MCS® 251 Architecture Overview

- **Binary Code Compatible with MCS 51® Architecture**
- **5 to 15 Times Increase in Performance Compared to MCS 251 Microcontroller at the Same Clock Speed**
- **3-Stage Pipeline CPU Architecture**
- **2 Clocks (1 State) per Instruction**
- **16-Bit Internal Code Bus**
  - **— 2 Bytes/State Code Fetch**
- **8-Bit ALU**
  - **— High Speed 8-Bit Source and 16-Bit Destination Bus**
- **40 Bytes General Purpose Register File**
  - **— Accessible as 16 8-Bit, 16 16-Bit or 10 32-Bit Registers**
  - **— With Accumulator Functionality and Data Indexing Capability**
- **24-Bit Linear Code and Data Addressing**
- **64KB Stack Space**
- **New Instructions and Addressing Modes**
  - **— 8, 16 and Limited 32-Bit Data Transfer, Arithmetic and Logical Instructions**
  - **— Supports Register, Immediate, Direct, Indirect, Displacement, Relative and Bit Addressing**
- **Support 64 Interrupt Sources**
  - **— 1 TRAP Instruction Interrupt (Highest Priority)**
  - **— 1 Non-Maskable Interrupt (2nd Highest Priority)**
  - **— 62 Maskable Interrupt Sources**
  - **— 4 Interrupt Priority Levels**
- **Complete Tools Support**
  - **— Assemblers and C Compilers**
  - **— In-Circuit Emulator**
  - **— OTP/EPROM Programmer**
  - **— Debuggers**

MCS 251 architecture is the next generation of Intel MCS 51 architecture that increases system performance by a factor of five using existing MCS 51 microcontroller code. By rewriting code using the MCS 251 architecture instructions, designers can increase performance up to 15 times.

The new MCS 251 architecture brings high performance, an increased memory mix and addressing, low power, low noise, efficient high level language support, enhanced instruction set, integrated features and functionality to the 8-bit embedded control market segment. All products in the family will be built around the new MCS 251 architecture core. They will have various peripherals, memories, input/ouput (I/O) ports, and a BIU (Bus Interface Unit). Most importantly, new proliferations will be binary code-compatible with existing 8051 components. Software investment is protected while providing an easy performance upgrade path. (See table 1 for features and benefits listing.)

The first product based on the new architecture will be 80C51 pin-compatible and a direct "plug-in" replacement. Anticipated availability of general samples is Q1 of 1995 with additional proliferations to follow later in the year.

Development tools for the new architecture will be available from some of the leading tools vendors. The vendors, including BSO Tasking; Data I/O Corporation; Keil Elektronik GmbH/Franklin Software Inc.; Metalink Corporation; Needham; Nohau Corporation; Production Languages Corporation (PLC); SMS Mikrocomputer-Systeme GmbH; and System General Corporation are planning to supply a full range of hardware and software development tools such as emulators, compilers, programmers and debuggers.

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Table 1. Features and Benefits

Features	Benefits
• 3-stage pipeline CPU architecture • 1 state (2 clocks) per machine cycle (vs 6 states (12 clocks) per machine cycle for MCS® 51 microcontroller) • 16-bit internal code bus	• High performance. 5 to 15 times increase in performance compared to MCS 51 microcontroller at the same clock speed • High instruction throughput at low clock speed reduces power consumption and RFI

• Enhanced MCS 51 instruction set with:
  • 16-bit and limited 32-bit data transfer, arithmetic and logic instructions
  • Register-to-register operations
  • Extended addressing modes
  • Improved control instructions
  • Bigger bit addressable space
	• Increased performance and programming flexibility.
	• Reduced code size.

• Binary code-compatible with MCS 51 microcontroller	• Protects software investment • Easy performance upgrade from MCS 51 microcontroller applications
• Register-based machine with 40 register bytes accessible as 16 8-bit registers, 16 16-bit registers, 10 32-bit registers or a combination of all. All registers are general-purpose with accumulator functionality and data indexing capability.	• Increased performance and programming flexibility • Increased efficiency for C code
• 24-bit linear addressing for up to 16 MB memory space	• Support bigger code and data memory requirement.
• 64 KB extended stack space and additional stack instructions	• Increased efficiency for C code

CPU Overview

The central processing unit (CPU) represents the heart of the MCS 251 architecture and consists of the ALU, instruction sequencer, program counter and the register file, connected by high-speed source and destination buses. The CPU performs all instructions as a series of 8-bit microcontroller operations. The CPU is implemented using typical pipelining techniques, and is built around a three-stage pipeline. The pipe stages are instruction fetch or decode, address generation or data fetch, and execution or write back. The three-stage pipeline implementation offers the best trade-off between performance and design complexity.

Memory Interface

The CPU interfaces with the peripherals, memories and other chip units via internal instruction and data buses. The MCS 251 architecture has an internal 16-bit wide instruction bus capable of sustained 2 bytes/state code fetches. It also has an 8-bit data bus capable of one byte/state data transfer rate.

The MCS 251 architecture has one contiguous 16MB address space that is used for both code and data. The 16MB address space will be partitioned for internal and external access, depending on the amount of on-chip memory.

Code memory can reside anywhere in the address space except for reserved areas. Further restrictions may prevent code execution from certain locations that may vary from product to product. The code memory resides outside the CPU and will be partitioned as internal and external memory, depending on the amount of on-chip code memory.

Data memory can reside anywhere in the address space except for reserved areas. The lower 32 bytes of the data memory space can be accessed as both data memory and as four banks of general-purpose registers. All MCS 251 controllers will have this memory as part of the CPU; the amount of additional on-chip data memory may vary from product to product.

To provide flexibility to designers during development and production, the MCS 251 microcontroller will have one-time programmable (OTP), ROM and CPU-only versions available. Flash memory versions will be available in the future.

The MCS 251 architecture also supports an extra 32 bytes of general-purpose registers which reside in the CPU as register file. This is in addition to the 4 banks of 8 registers found on the MCS 51 microcontroller architecture. The register file can be addressed in the following ways, depending upon the registers to be accessed: registers 0–15 can be addressed as either byte, word or double word (Dword) registers; registers 16–31 can be addressed as either word or Dword registers; and registers 56–63 can be addressed only as Dword registers. There are 16 possible byte registers, 16 possible word registers and 10 possible Dword registers depending on the combinations. (See Figure 1 for register file diagram.)

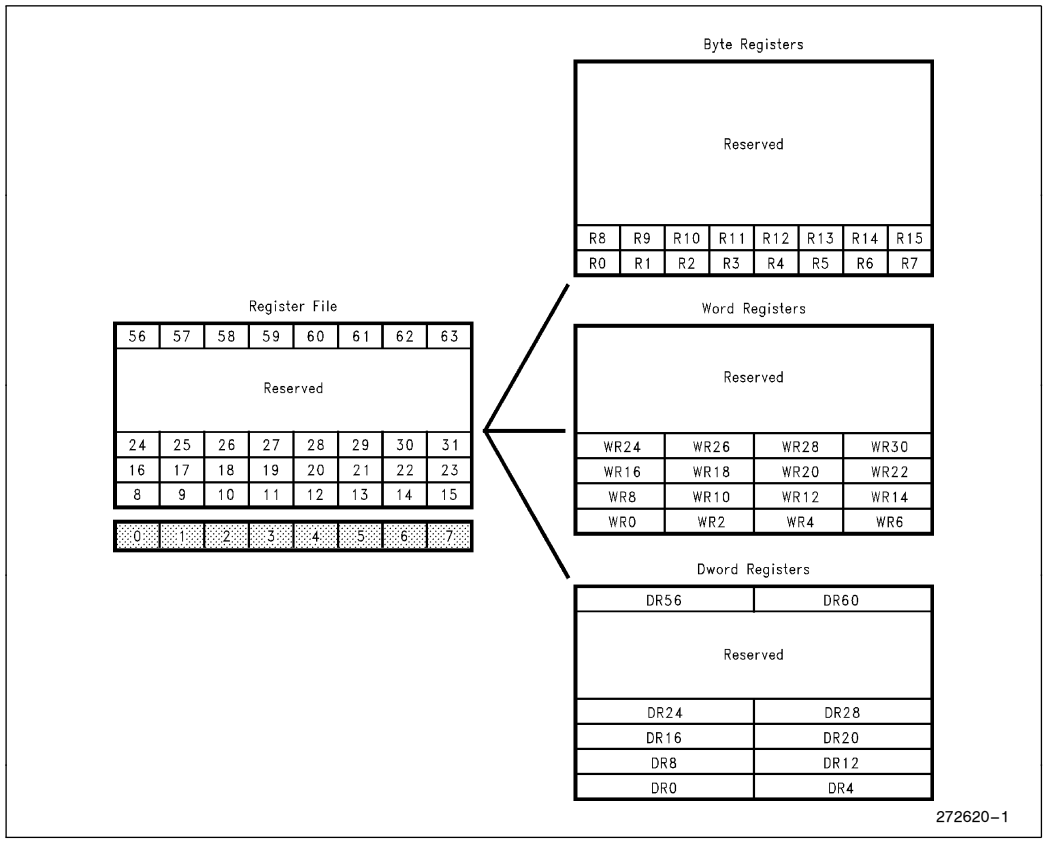

Figure 1. Register File Diagram

New Instruction Set

The MCS 251 architecture instruction set provides the user with newly-defined instructions that take advantage of the new architecture while maintaining all existing MCS 51 microcontroller instructions. Many of the MCS 251 microcontroller instructions can operate on either 8-, 16-, or limited 32-bit operands. This capability allows the MCS 251 architecture proliferations to be used more easily and efficiently with high-level programming languages such as "C."

The instruction set consists of data instructions, bit instructions and control instructions. Data instructions process 8-, 16-, and limited 32-bit data; bit instructions manipulate bits; and control instructions manage program flow. Each instruction type has a unique set of addressing modes; for example, not all data addressing modes apply to control instructions and vice-versa. The MCS 251 architecture supports the following addressing modes:

- Register addressing: The instruction specifies the register which contains the operand.
- Immediate addressing: The instruction contains the operand.
- Direct addressing: The instruction contains the operand address.
- Indirect addressing: The instruction specifies the register containing operand address.
- Displacement addressing: The sum of the register and a signed offset specified by the instruction is the operand address.
- Relative addressing: The instruction contains the relative offset from the next instruction to target address.
- Bit addressing: The instruction contains the bit address.

Interrupt Overview

The MCS 251 architecture supports one non-maskable interrupt, one TRAP (technical return analysis program) instruction interrupt and up to 62 maskable interrupt sources. The user can select each interrupt individually as well as control its priority level. The non-maskable interrupt is fixed in hardware to always have the second highest priority (after TRAP) and is always enabled. The exact number of interrupt sources, both internal and external, depends on the specific MCS 251 architecture proliferations.

Compatibility

The MCS 251 architecture is code-compatible with the MCS 51 architecture. And, all 51 microcontroller instructions are available on the 251. The 51 controllers have four separate address spaces: program memory, special function registers, and internal and external data memory. The 251 incorporates the program memory and the data memory address spaces into a 16MB unified address space. The mapping is completely transparent to the user and is taken care of by the assembler.

Future Outlook

General samples for first product based on the MCS 251 architecture core are anticipated in the first quarter of 1995. This product will be 80C51 pin-compatible and a direct plug-in replacement. Additional products based on the core will include additional peripherals targeted to specific market segments to meet customer needs.

MCS® 251 Architecture Block Diagram