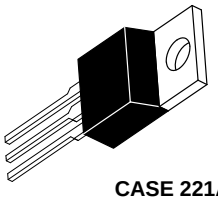
MCR218 Series

Thyristors
Silicon-Controlled Rectifiers

. . . designed primarily for half-wave ac control applications, such as motor controls, heating controls and power supplies; or wherever half-wave silicon gate-controlled, solid-state devices are needed.

- Glass-Passivated Junctions
- Blocking Voltage to 800 Volts
- TO-220 Construction — Low Thermal Resistance, High Heat Dissipation and Durability

SCRs
8 AMPERES RMS
50 thru 800 VOLTS



CASE 221A-04
(TO-220AB)
STYLE 3

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted.)

Rating		Symbol	Value	Unit
Peak Repetitive Forward and Reverse Voltage(1) (T_J = 25 to 125°C, Gate Open)	MCR218-2	V_{DRM} V_{RRM}	50	Volts
	MCR218-3		100	
	MCR218-4		200	
	MCR218-6		400	
	MCR218-8		600	
	MCR218-10		800	
Forward Current RMS (All Conduction Angles)		$I_{T(RMS)}$	8	Amps
Peak Forward Surge Current (1/2 Cycle, Sine Wave, 60 Hz)		I_{TSM}	80	Amps
Circuit Fusing Considerations (t = 8.3 ms)		I^2t	26	A^2s
Forward Peak Gate Power		P_{GM}	5	Watts
Forward Average Gate Power		$P_{G(AV)}$	0.5	Watt
Forward Peak Gate Current		I_{GM}	2	Amps
Operating Junction Temperature Range		T_J	–40 to +125	°C
Storage Temperature Range		T_{stg}	–40 to +150	°C

1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

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THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	2	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Peak Forward or Reverse Blocking Current (V_{AK} = Rated V_{DRM} or V_{RRM}, Gate Open) T_J = 25°C T_J = 125°C	I_{DRM}, I_{RRM}	— —	— —	10 2	μA mA
Peak On-State Voltage(1) (I_{TM} = 16 A Peak)	V_{TM}	—	1.5	1.8	Volts
Gate Trigger Current (Continuous dc) (V_D = 12 V, R_L = 100 Ohms)	I_{GT}	—	10	25	mA
Gate Trigger Voltage (Continuous dc) (V_D = 12 V, R_L = 100 Ohms) (Rated V_{DRM}, R_L = 1000 Ohms, T_J = 125°C)	V_{GT}	— 0.2	— —	1.5 —	Volts
Holding Current (Anode Voltage = 24 Vdc, Peak Initiating On-State Current = 0.5 A, 0.1 to 10 ms Pulse, Gate Trigger Source = 7 V, 20 Ohms)	I_H	—	16	30	mA
Critical Rate-of-Rise of Off-State Voltage (V_D = Rated V_{DRM}, Exponential Waveform, Gate Open, T_J = 125°C)	dv/dt	—	100	—	V/μs

1. Pulse Test: Pulse Width = 1 ms, Duty Cycle ≤ 2%.

FIGURE 1 — CURRENT DERATING

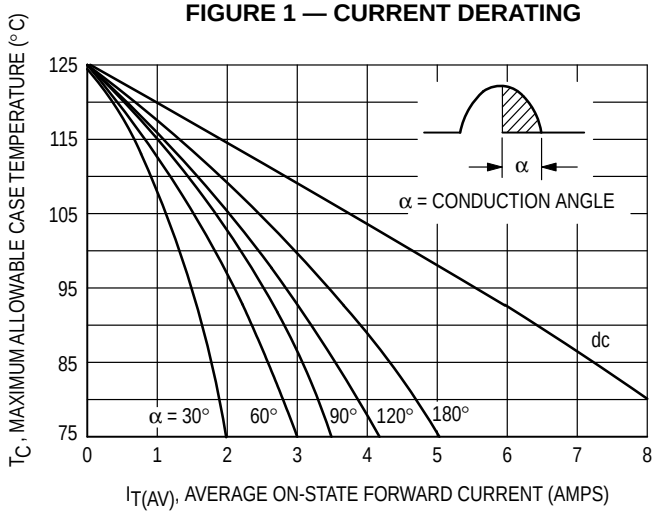


FIGURE 2 — ON-STATE POWER DISSIPATION

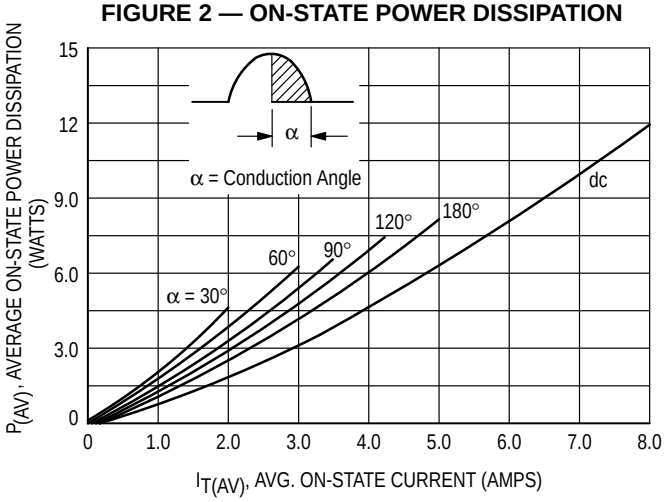


FIGURE 3 — NORMALIZED GATE TRIGGER CURRENT

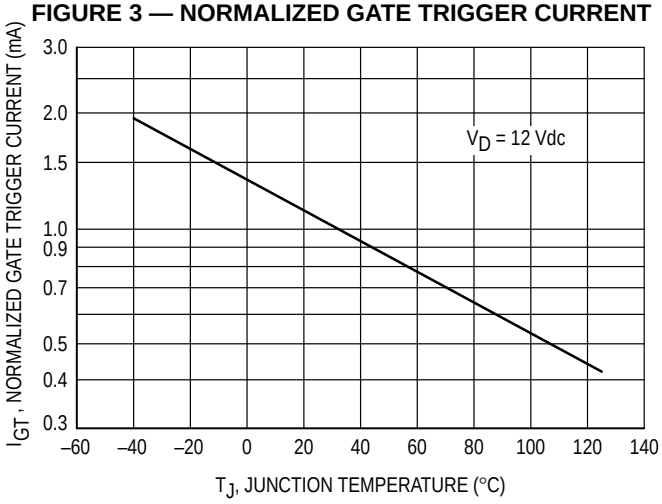


FIGURE 4 — NORMALIZED GATE TRIGGER VOLTAGE

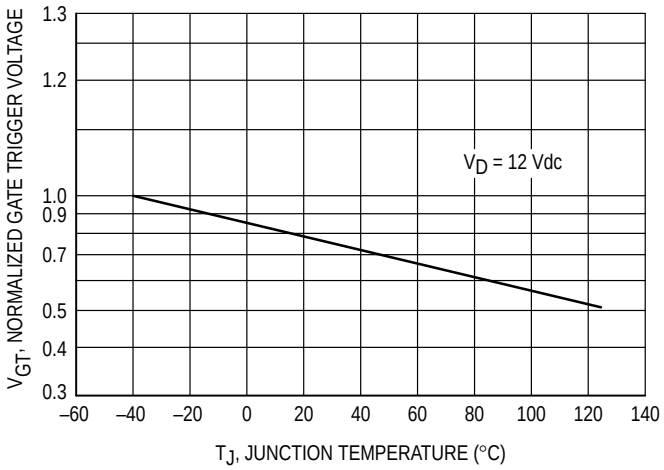
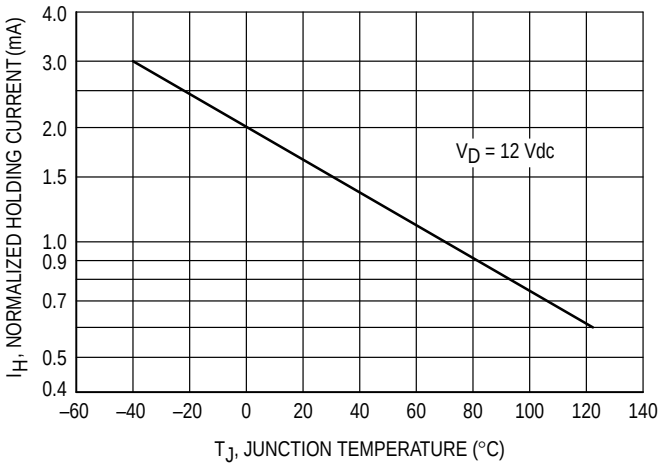
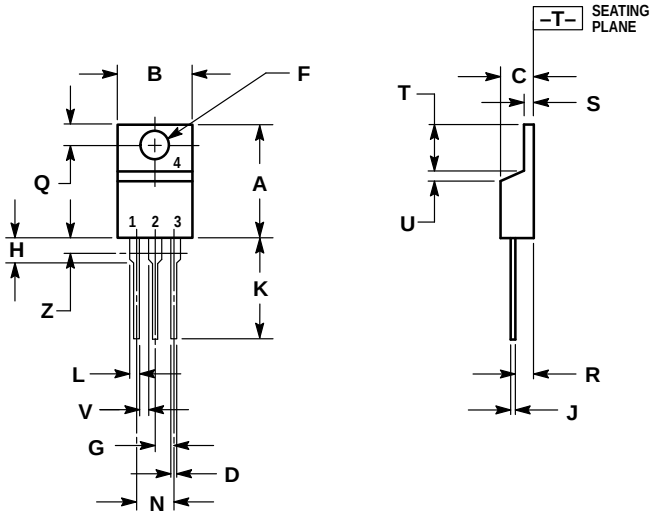


FIGURE 5 — NORMALIZED HOLDING CURRENT



PACKAGE DIMENSIONS



STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.022	0.36	0.55
K	0.500	0.562	12.70	14.27
L	0.045	0.055	1.15	1.39
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04

CASE 221A-04
(TO–220AB)

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