# MCP3204/3208

## 2.7V 4-Channel/8-Channel 12-Bit A/D Converters with SPI™ Serial Interface

### Features

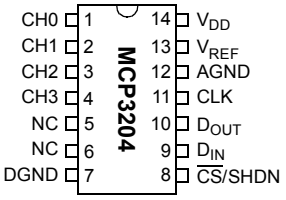
- 12-bit resolution
- ± 1 LSB max DNL
- ± 1 LSB max INL (MCP3204/3208-B)
- ± 2 LSB max INL (MCP3204/3208-C)
- 4 (MCP3204) or 8 (MCP3208) input channels
- Analog inputs programmable as single-ended or pseudo-differential pairs
- On-chip sample and hold
- SPI serial interface (modes 0,0 and 1,1)
- Single supply operation: 2.7V - 5.5V
- 100 ksps max. sampling rate at $V_{DD}$ = 5V
- 50 ksps max. sampling rate at $V_{DD}$ = 2.7V
- Low power CMOS technology:
  - 500 nA typical standby current, 2 µA max.
  - 400 µA max. active current at 5V
- Industrial temp range: -40°C to +85°C
- Available in PDIP, SOIC and TSSOP packages

### Applications

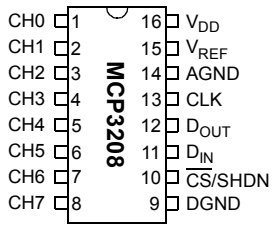
- Sensor Interface
- Process Control
- Data Acquisition
- Battery Operated Systems

### Package Types

**PDIP, SOIC, TSSOP**




**PDIP, SOIC**

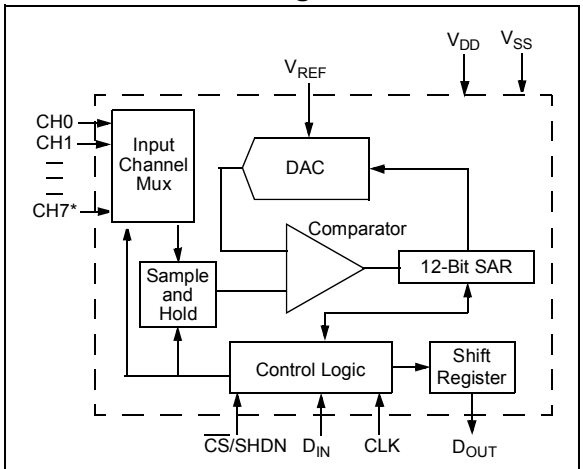



### Description

The Microchip Technology Inc. MCP3204/3208 devices are successive approximation 12-bit Analog-to-Digital (A/D) Converters with on-board sample and hold circuitry. The MCP3204 is programmable to provide two pseudo-differential input pairs or four single-ended inputs. The MCP3208 is programmable to provide four pseudo-differential input pairs or eight single-ended inputs. Differential Nonlinearity (DNL) is specified at ±1 LSB, while Integral Nonlinearity (INL) is offered in ±1 LSB (MCP3204/3208-B) and ±2 LSB (MCP3204/3208-C) versions.

Communication with the devices is accomplished using a simple serial interface compatible with the SPI protocol. The devices are capable of conversion rates of up to 100 ksps. The MCP3204/3208 devices operate over a broad voltage range (2.7V - 5.5V). Low current design permits operation with typical standby and active currents of only 500 nA and 320 µA, respectively. The MCP3204 is offered in 14-pin PDIP, 150 mil SOIC and TSSOP packages. The MCP3208 is offered in 16-pin PDIP and SOIC packages.

### Functional Block Diagram




*** Note:** Channels 5-7 available on MCP3208 Only

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings*

$V_{DD}$.....7.0V

All inputs and outputs w.r.t. $V_{SS}$ ..... -0.6V to $V_{DD}$ +0.6V

Storage temperature .....-65°C to +150°C

Ambient temp. with power applied .....-65°C to +125°C

Soldering temperature of leads (10 seconds) ..... +300°C

ESD protection on all pins.....> 4 kV

***Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

## PIN FUNCTION TABLE

| Name | Function |
|---|---|
| $V_{DD}$ | +2.7V to 5.5V Power Supply |
| DGND | Digital Ground |
| AGND | Analog Ground |
| CH0-CH7 | Analog Inputs |
| CLK | Serial Clock |
| $D_{IN}$ | Serial Data In |
| $D_{OUT}$ | Serial Data Out |
| $\overline{CS}$/SHDN | Chip Select/Shutdown Input |
| $V_{REF}$ | Reference Voltage Input |

### ELECTRICAL SPECIFICATIONS

**Electrical Characteristics:** Unless otherwise noted, all parameters apply at $V_{DD}$ = 5V, $V_{SS}$ = 0V, $V_{REF}$ = 5V, $T_{AMB}$ = -40°C to +85°C, $f_{SAMPLE}$ = 100 ksps and $f_{CLK}$ = 20*$f_{SAMPLE}$

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Conversion Rate** | | | | | | |
| Conversion Time | $t_{CONV}$ | — | — | 12 | clock cycles | |
| Analog Input Sample Time | $t_{SAMPLE}$ | | 1.5 | | clock cycles | |
| Throughput Rate | $f_{SAMPLE}$ | —<br>— | —<br>— | 100<br>50 | ksps<br>ksps | $V_{DD}$ = $V_{REF}$ = 5V<br>$V_{DD}$ = $V_{REF}$ = 2.7V |
| **DC Accuracy** | | | | | | |
| Resolution | | | 12 | | bits | |
| Integral Nonlinearity | INL | —<br>— | ±0.75<br>±1.0 | ±1<br>±2 | LSB | MCP3204/3208-B<br>MCP3204/3208-C |
| Differential Nonlinearity | DNL | — | ±0.5 | ±1 | LSB | No missing codes over-temperature |
| Offset Error | | — | ±1.25 | ±3 | LSB | |
| Gain Error | | — | ±1.25 | ±5 | LSB | |
| **Dynamic Performance** | | | | | | |
| Total Harmonic Distortion | | — | -82 | — | dB | $V_{IN}$ = 0.1V to 4.9V@1 kHz |
| Signal to Noise and Distortion (SINAD) | | — | 72 | — | dB | $V_{IN}$ = 0.1V to 4.9V@1 kHz |
| Spurious Free Dynamic Range | | — | 86 | — | dB | $V_{IN}$ = 0.1V to 4.9V@1 kHz |
| **Reference Input** | | | | | | |
| Voltage Range | | 0.25 | — | $V_{DD}$ | V | **Note 2** |
| Current Drain | | —<br>— | 100<br>0.001 | 150<br>3.0 | µA<br>µA | <br>$\overline{CS}$ = $V_{DD}$ = 5V |

**Note 1:** This parameter is established by characterization and not 100% tested.

**2:** See graphs that relate linearity performance to $V_{REF}$ levels.

**3:** Because the sample cap will eventually lose charge, effective clock rates below 10 kHz can affect linearity performance, particularly at elevated temperatures. See Section 6.2, “Maintaining Minimum Clock Speed”, for more information.

## ELECTRICAL SPECIFICATIONS (CONTINUED)

**Electrical Characteristics:** Unless otherwise noted, all parameters apply at $V_{DD}$ = 5V, $V_{SS}$ = 0V, $V_{REF}$ = 5V, $T_{AMB}$ = -40°C to +85°C, $f_{SAMPLE}$ = 100 ksps and $f_{CLK}$ = 20*$f_{SAMPLE}$

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Analog Inputs** | | | | | | |
| Input Voltage Range for CH0-CH7 in Single-Ended Mode | | $V_{SS}$ | — | $V_{REF}$ | V | |
| Input Voltage Range for IN+ in pseudo-differential Mode | | IN- | — | $V_{REF}$+IN- | | |
| Input Voltage Range for IN- in pseudo-differential Mode | | $V_{SS}$-100 | — | $V_{SS}$+100 | mV | |
| Leakage Current | | — | 0.001 | ±1 | µA | |
| Switch Resistance | | — | 1000 | — | Ω | See Figure 4-1 |
| Sample Capacitor | | — | 20 | — | pF | See Figure 4-1 |
| **Digital Input/Output** | | | | | | |
| Data Coding Format | | Straight Binary | | | | |
| High Level Input Voltage | $V_{IH}$ | 0.7 $V_{DD}$ | — | — | V | |
| Low Level Input Voltage | $V_{IL}$ | — | — | 0.3 $V_{DD}$ | V | |
| High Level Output Voltage | $V_{OH}$ | 4.1 | — | — | V | $I_{OH}$ = -1 mA, $V_{DD}$ = 4.5V |
| Low Level Output Voltage | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 1 mA, $V_{DD}$ = 4.5V |
| Input Leakage Current | $I_{LI}$ | -10 | — | 10 | µA | $V_{IN}$ = $V_{SS}$ or $V_{DD}$ |
| Output Leakage Current | $I_{LO}$ | -10 | — | 10 | µA | $V_{OUT}$ = $V_{SS}$ or $V_{DD}$ |
| Pin Capacitance (All Inputs/Outputs) | $C_{IN}$,$C_{OUT}$ | — | — | 10 | pF | $V_{DD}$ = 5.0V (**Note 1**)<br>$T_{AMB}$ = 25°C, f = 1 MHz |
| **Timing Parameters** | | | | | | |
| Clock Frequency | $f_{CLK}$ | —<br>— | —<br>— | 2.0<br>1.0 | MHz<br>MHz | $V_{DD}$ = 5V (**Note 3**)<br>$V_{DD}$ = 2.7V (**Note 3**) |
| Clock High Time | $t_{HI}$ | 250 | — | — | ns | |
| Clock Low Time | $t_{LO}$ | 250 | — | — | ns | |
| $\overline{CS}$ Fall To First Rising CLK Edge | $t_{SUCS}$ | 100 | — | — | ns | |
| Data Input Setup Time | $t_{SU}$ | — | — | 50 | ns | |
| Data Input Hold Time | $t_{HD}$ | — | — | 50 | ns | |
| CLK Fall To Output Data Valid | $t_{DO}$ | — | — | 200 | ns | See Figures 1-2 and 1-3 |
| CLK Fall To Output Enable | $t_{EN}$ | — | — | 200 | ns | See Figures 1-2 and 1-3 |
| $\overline{CS}$ Rise To Output Disable | $t_{DIS}$ | — | — | 100 | ns | See Figures 1-2 and 1-3 |
| $\overline{CS}$ Disable Time | $t_{CSH}$ | 500 | — | — | ns | |
| $D_{OUT}$ Rise Time | $t_R$ | — | — | 100 | ns | See Figures 1-2 and 1-3 (**Note 1**) |
| $D_{OUT}$ Fall Time | $t_F$ | — | — | 100 | ns | See Figures 1-2 and 1-3 (**Note 1**) |
| **Power Requirements** | | | | | | |
| Operating Voltage | $V_{DD}$ | 2.7 | — | 5.5 | V | |
| Operating Current | $I_{DD}$ | —<br>— | 320<br>225 | 400<br>— | µA | $V_{DD}$=$V_{REF}$ = 5V, $D_{OUT}$ unloaded<br>$V_{DD}$=$V_{REF}$ = 2.7V, $D_{OUT}$ unloaded |
| Standby Current | $I_{DDS}$ | — | 0.5 | 2.0 | µA | $\overline{CS}$ = $V_{DD}$ = 5.0V |

**Note 1:** This parameter is established by characterization and not 100% tested.

**2:** See graphs that relate linearity performance to $V_{REF}$ levels.

**3:** Because the sample cap will eventually lose charge, effective clock rates below 10 kHz can affect linearity performance, particularly at elevated temperatures. See Section 6.2, “Maintaining Minimum Clock Speed”, for more information.

## ELECTRICAL SPECIFICATIONS (CONTINUED)

**Electrical Characteristics:** Unless otherwise noted, all parameters apply at $V_{DD}$ = 5V, $V_{SS}$ = 0V, $V_{REF}$ = 5V, $T_{AMB}$ = -40°C to +85°C,$f_{SAMPLE}$ = 100 ksps and $f_{CLK}$ = 20*$f_{SAMPLE}$

| Parameters | Sym | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| **Temperature Ranges** | | | | | | |
| Specified Temperature Range | $T_A$ | -40 | — | +85 | °C | |
| Operating Temperature Range | $T_A$ | -40 | — | +85 | °C | |
| Storage Temperature Range | $T_A$ | -65 | — | +150 | °C | |
| **Thermal Package Resistance** | | | | | | |
| Thermal Resistance, 14L-PDIP | $\theta_{JA}$ | — | 70 | — | °C/W | |
| Thermal Resistance, 14L-SOIC | $\theta_{JA}$ | — | 108 | — | °C/W | |
| Thermal Resistance, 14L-TSSOP | $\theta_{JA}$ | — | 100 | — | °C/W | |
| Thermal Resistance, 16L-PDIP | $\theta_{JA}$ | — | 70 | — | °C/W | |
| Thermal Resistance, 16L-SOIC | $\theta_{JA}$ | — | 90 | — | °C/W | |

**Note 1:** This parameter is established by characterization and not 100% tested.

**2:** See graphs that relate linearity performance to $V_{REF}$ levels.

**3:** Because the sample cap will eventually lose charge, effective clock rates below 10 kHz can affect linearity performance, particularly at elevated temperatures. See Section 6.2, “Maintaining Minimum Clock Speed”, for more information.

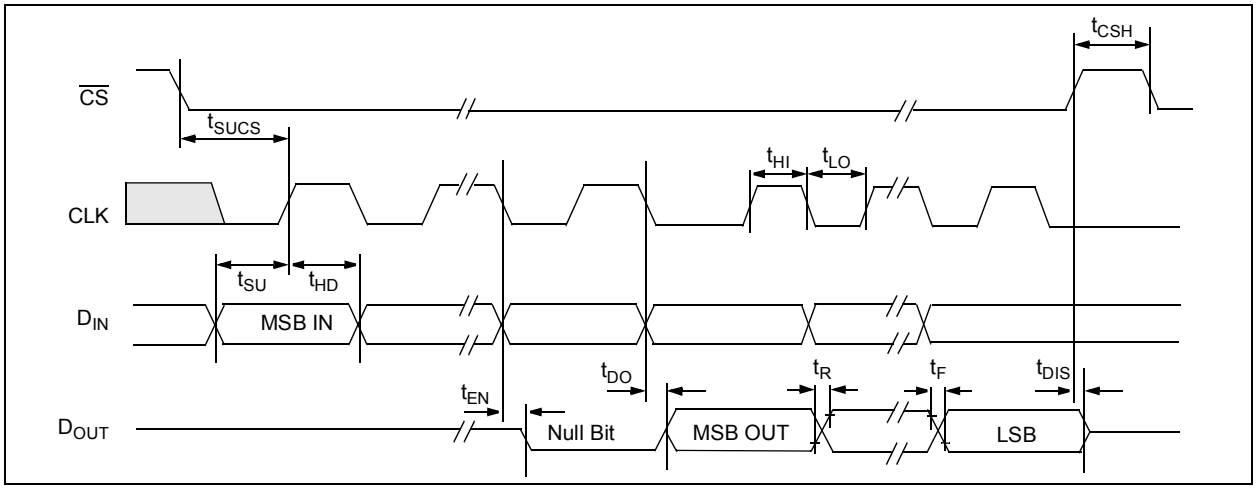



***FIGURE 1-1:*** *Serial Interface Timing.*

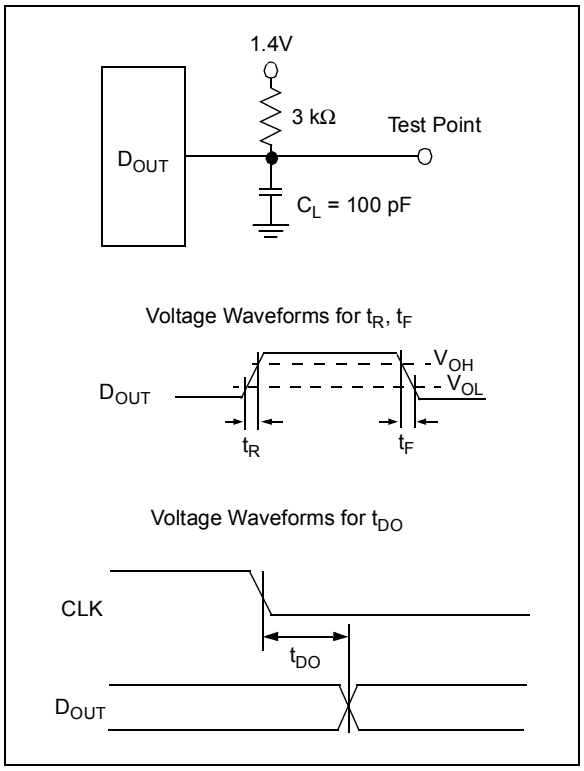
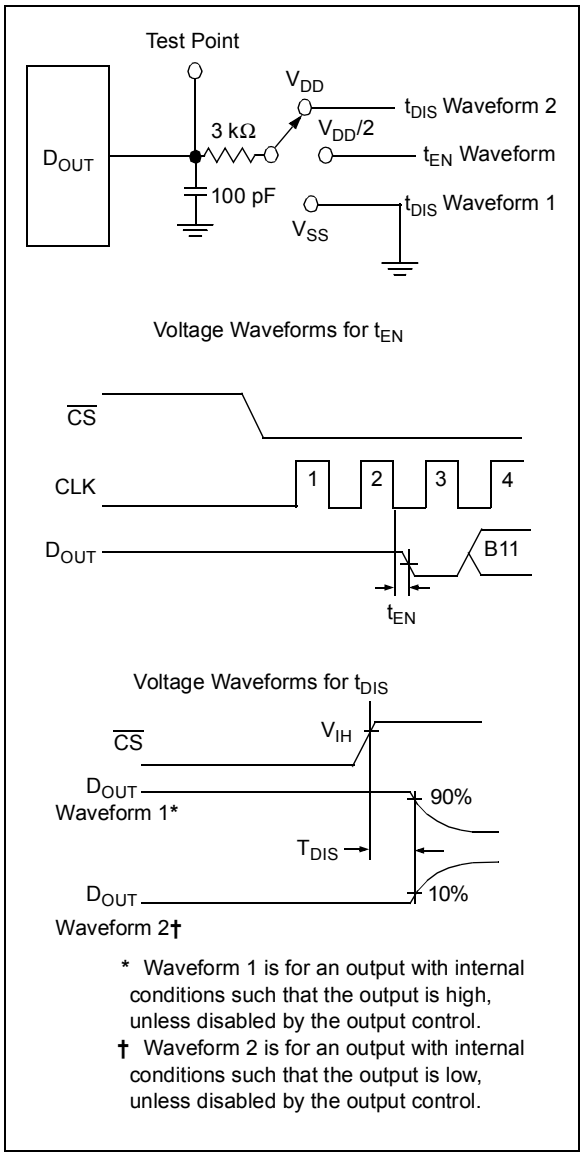



***FIGURE 1-2:*** *Load Circuit for $t_R$, $t_F$, $t_{DO}$.*




* Waveform 1 is for an output with internal conditions such that the output is high, unless disabled by the output control.

† Waveform 2 is for an output with internal conditions such that the output is low, unless disabled by the output control.

***FIGURE 1-3:*** *Load circuit for $t_{DIS}$ and $t_{EN}$.*

## 2.0 TYPICAL PERFORMANCE CHARACTERISTICS

| **Note:** | The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range. |
|---|---|

**Note:** Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 20 * f_{SAMPLE}$, $T_A = 25°C$.

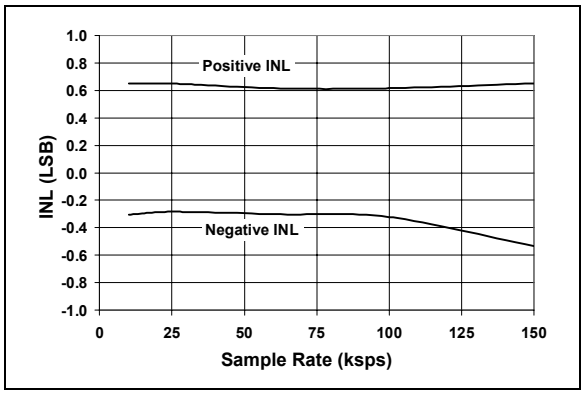



***FIGURE 2-1:*** *Integral Nonlinearity (INL) vs. Sample Rate.*

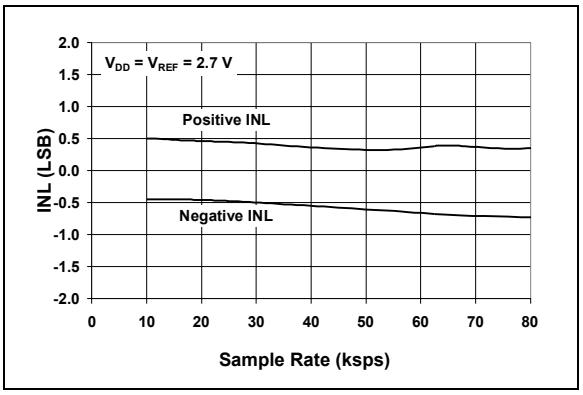



***FIGURE 2-4:*** *Integral Nonlinearity (INL) vs. Sample Rate ($V_{DD}$ = 2.7V).*

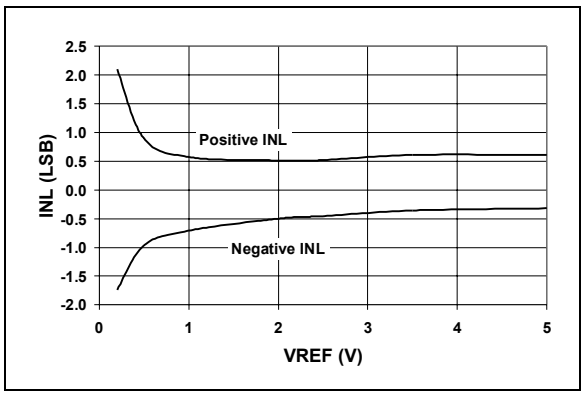



***FIGURE 2-2:*** *Integral Nonlinearity (INL) vs. $V_{REF}$*

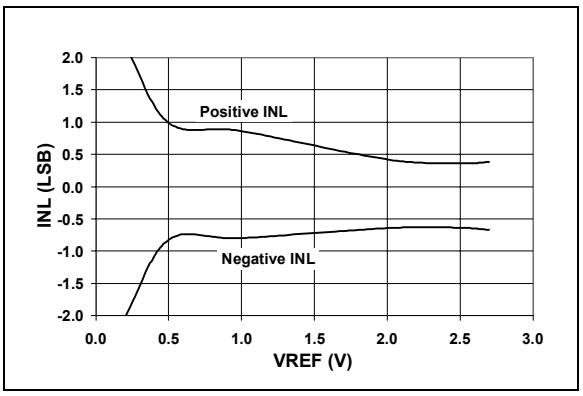



***FIGURE 2-5:*** *Integral Nonlinearity (INL) vs. $V_{REF}$ ($V_{DD}$ = 2.7V).*

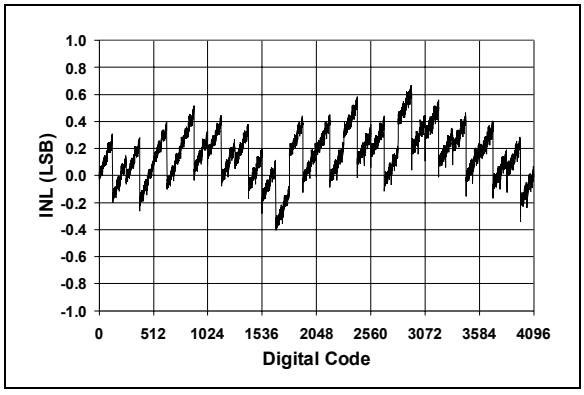



***FIGURE 2-3:*** *Integral Nonlinearity (INL) vs. Code (Representative Part).*

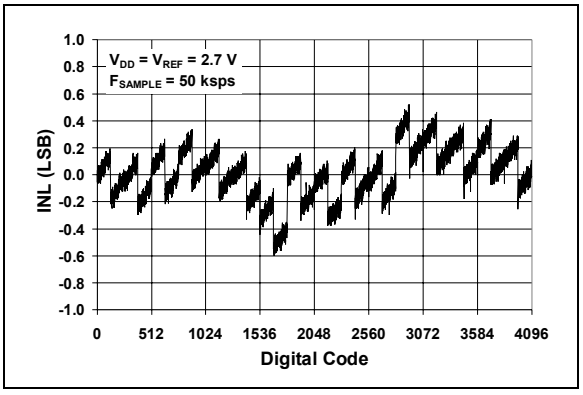



***FIGURE 2-6:*** *Integral Nonlinearity (INL) vs. Code (Representative Part, $V_{DD}$ = 2.7V).*

**Note:** Unless otherwise indicated, $V_{DD} = V_{REF} = 5$ V, $V_{SS} = 0$ V, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 20 * f_{SAMPLE}$, $T_A = 25°C$.

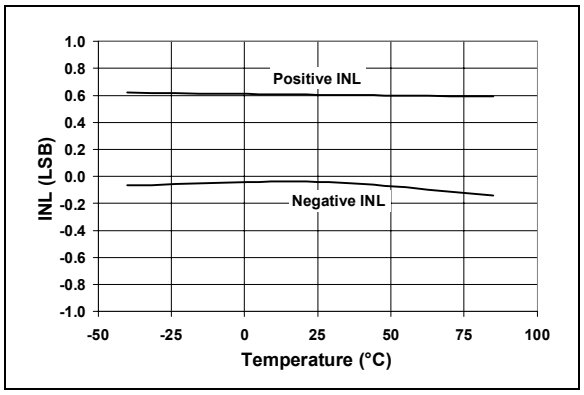



***FIGURE 2-7:*** *Integral Nonlinearity (INL) vs. Temperature.*

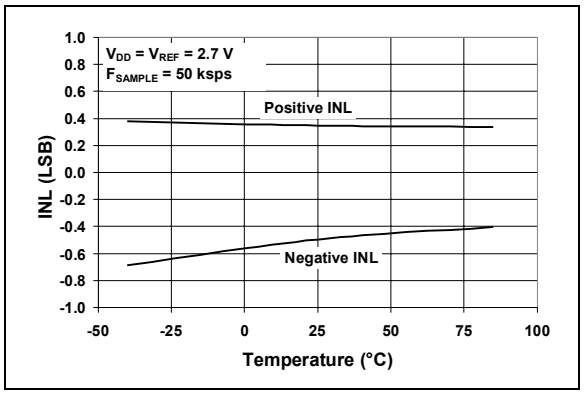



***FIGURE 2-10:*** *Integral Nonlinearity (INL) vs. Temperature ($V_{DD}$ = 2.7V).*

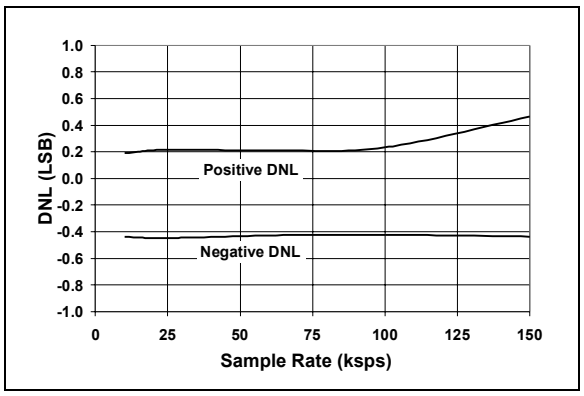



***FIGURE 2-8:*** *Differential Nonlinearity (DNL) vs. Sample Rate.*

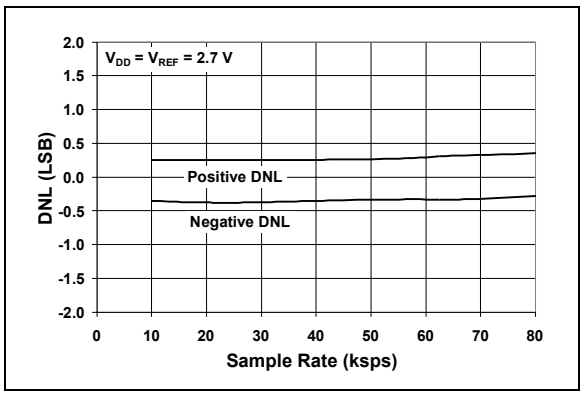



***FIGURE 2-11:*** *Differential Nonlinearity (DNL) vs. Sample Rate ($V_{DD}$ = 2.7V).*

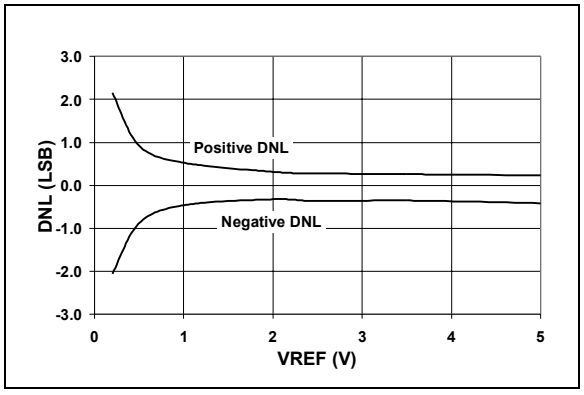



***FIGURE 2-9:*** *Differential Nonlinearity (DNL) vs. $V_{REF}$*

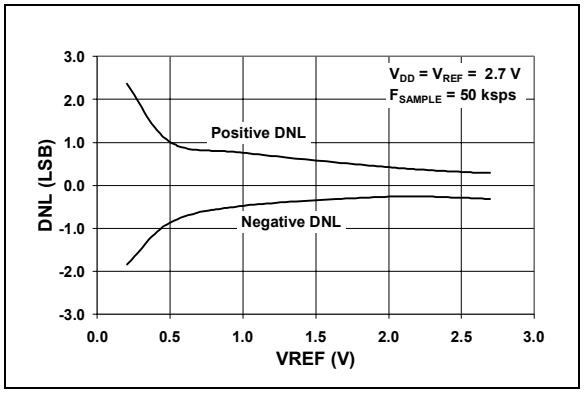



***FIGURE 2-12:*** *Differential Nonlinearity (DNL) vs. $V_{REF}$ ($V_{DD}$ = 2.7V).*

**Note:** Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 20* f_{SAMPLE}$, $T_A = 25°C$.

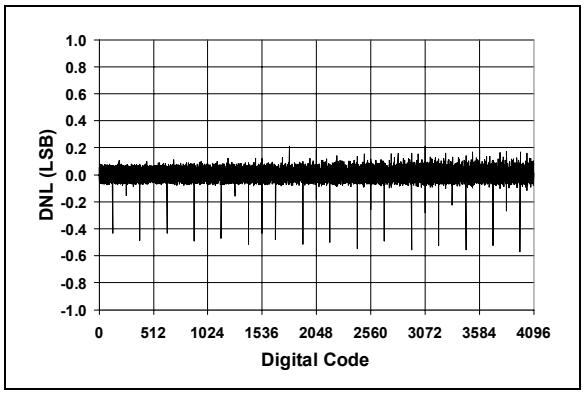



***FIGURE 2-13:*** *Differential Nonlinearity (DNL) vs. Code (Representative Part).*

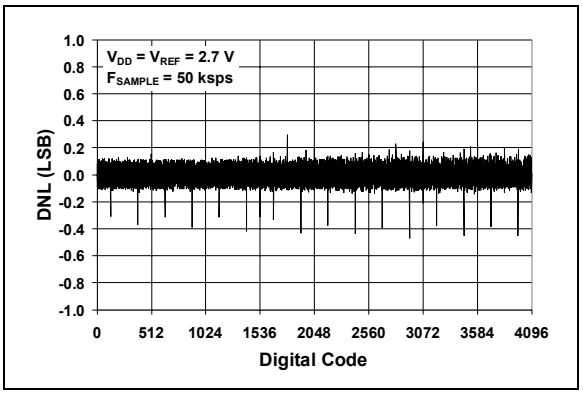



***FIGURE 2-16:*** *Differential Nonlinearity (DNL) vs. Code (Representative Part, $V_{DD}$ = 2.7V).*

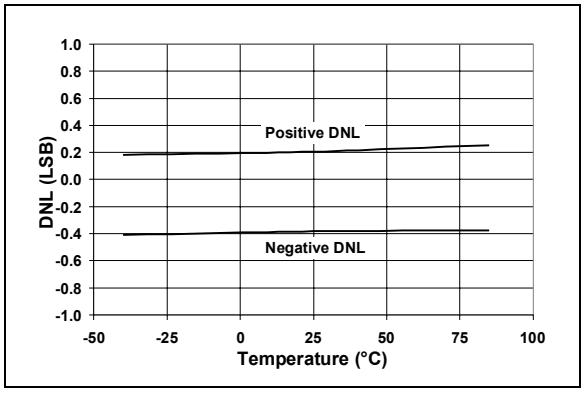



***FIGURE 2-14:*** *Differential Nonlinearity (DNL) vs. Temperature.*

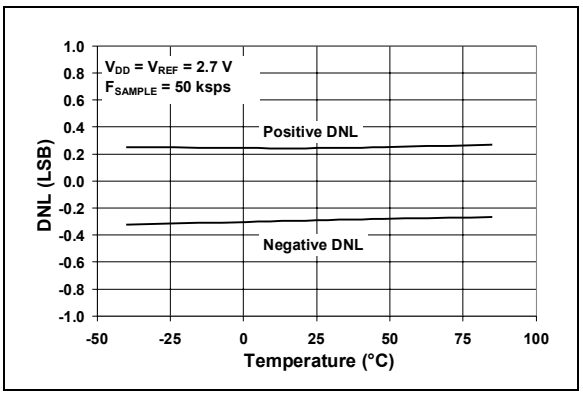



***FIGURE 2-17:*** *Differential Nonlinearity (DNL) vs. Temperature ($V_{DD}$ = 2.7V).*

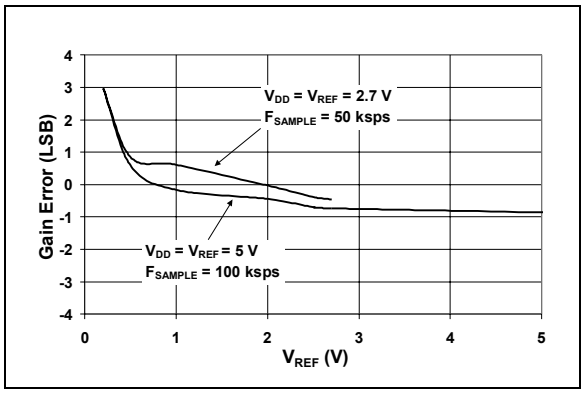



***FIGURE 2-15:*** *Gain Error vs. $V_{REF}$*

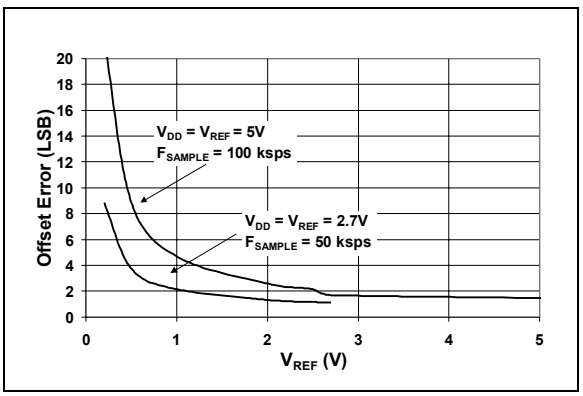



***FIGURE 2-18:*** *Offset Error vs. $V_{REF}$*

**Note:** Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 20^* f_{SAMPLE}$, $T_A = 25°C$.

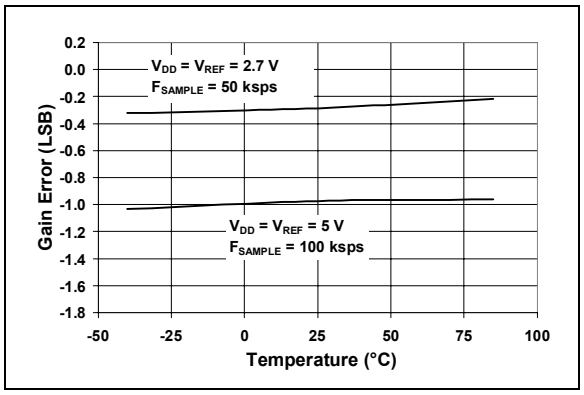



***FIGURE 2-19:*** *Gain Error vs. Temperature.*

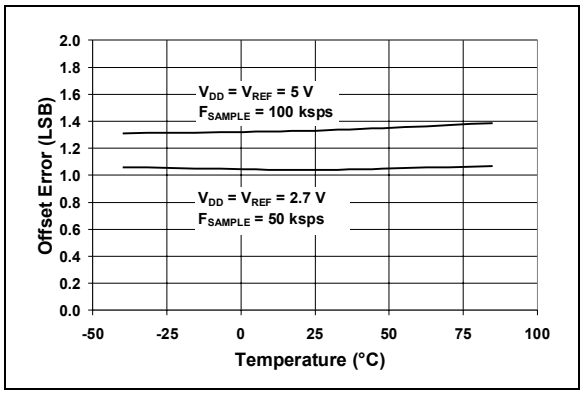



***FIGURE 2-22:*** *Offset Error vs. Temperature.*

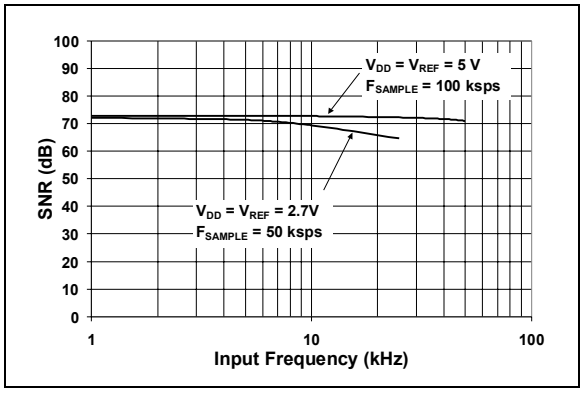



***FIGURE 2-20:*** *Signal to Noise (SNR) vs. Input Frequency.*

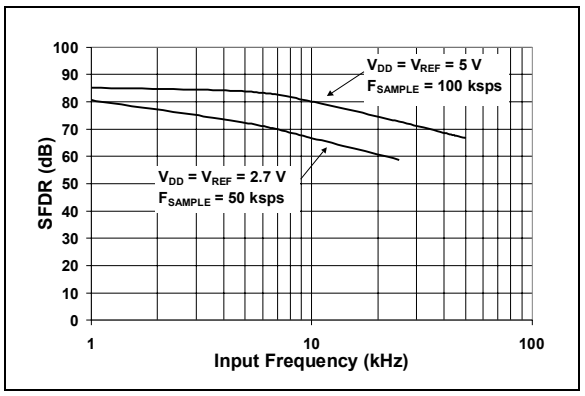



***FIGURE 2-23:*** *Signal to Noise and Distortion (SINAD) vs. Input Frequency.*

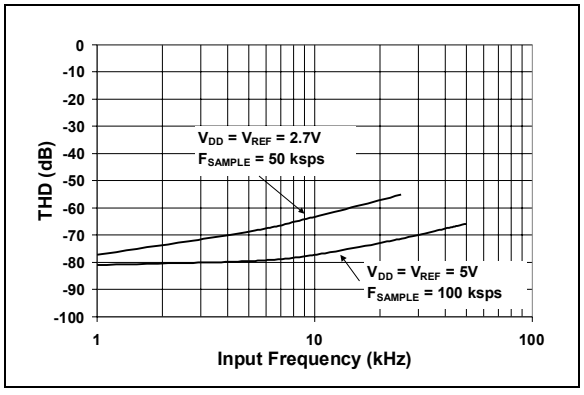



***FIGURE 2-21:*** *Total Harmonic Distortion (THD) vs. Input Frequency.*

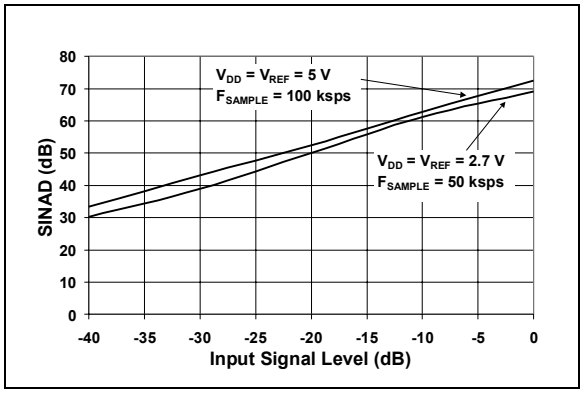



***FIGURE 2-24:*** *Signal to Noise and Distortion (SINAD) vs. Input Signal Level.*

**Note:** Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 20^* f_{SAMPLE}$, $T_A = 25°C$.

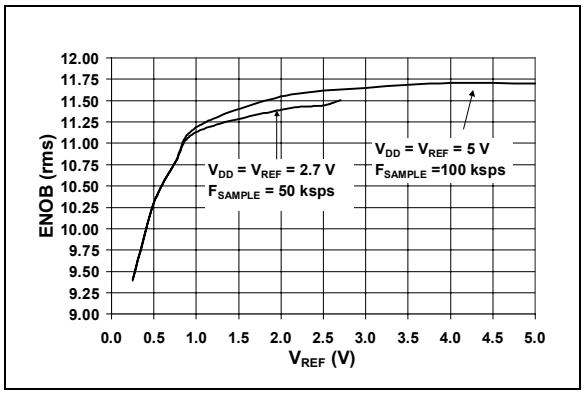



***FIGURE 2-25:*** *Effective Number of Bits (ENOB) vs. $V_{REF}$*

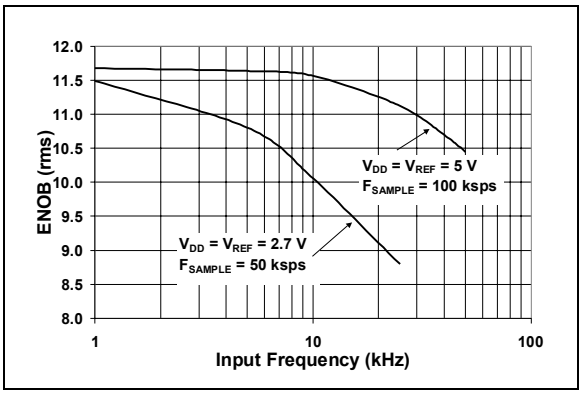



***FIGURE 2-28:*** *Effective Number of Bits (ENOB) vs. Input Frequency.*

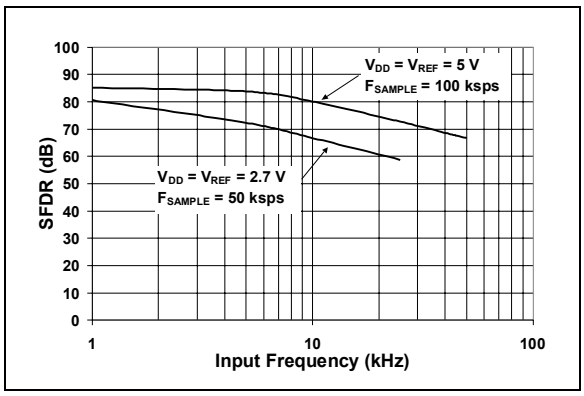



***FIGURE 2-26:*** *Spurious Free Dynamic Range (SFDR) vs. Input Frequency.*

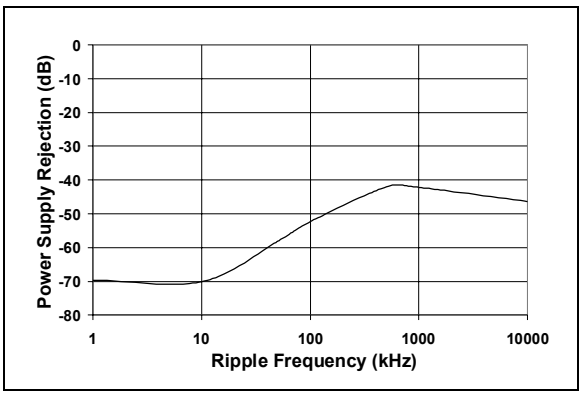



***FIGURE 2-29:*** *Power Supply Rejection (PSR) vs. Ripple Frequency.*

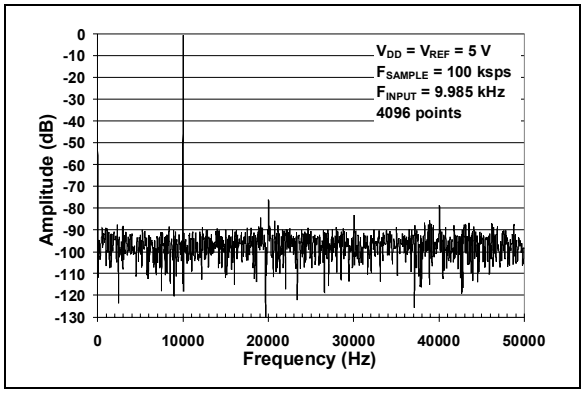



***FIGURE 2-27:*** *Frequency Spectrum of 10 kHz input (Representative Part).*

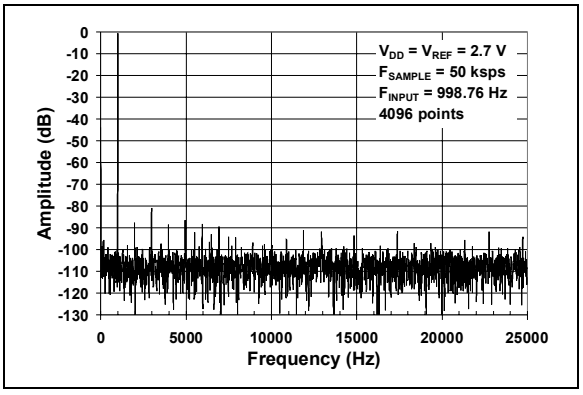



***FIGURE 2-30:*** *Frequency Spectrum of 1 kHz input (Representative Part, $V_{DD} = 2.7V$).*

**Note:** Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 20^* f_{SAMPLE}$, $T_A = 25°C$.

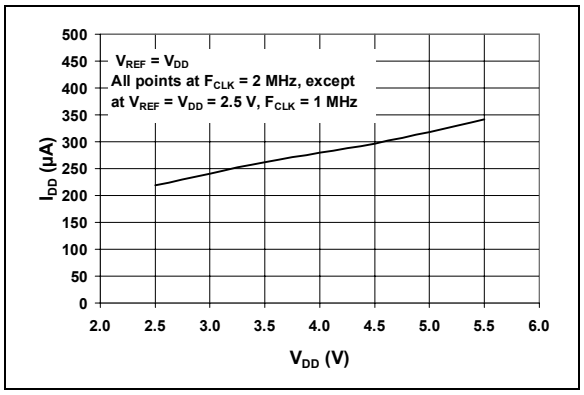



***FIGURE 2-31:*** *$I_{DD}$ vs. $V_{DD}$.*

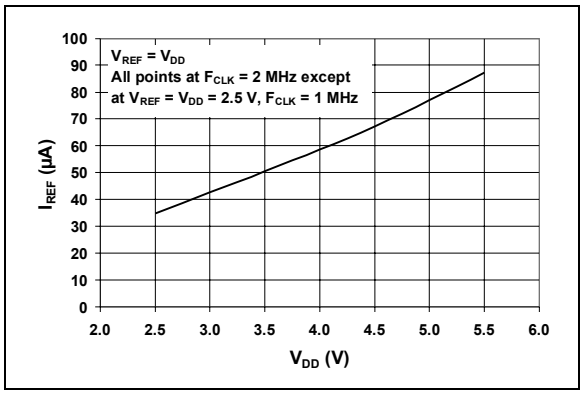



***FIGURE 2-34:*** *$I_{REF}$ vs. $V_{DD}$.*

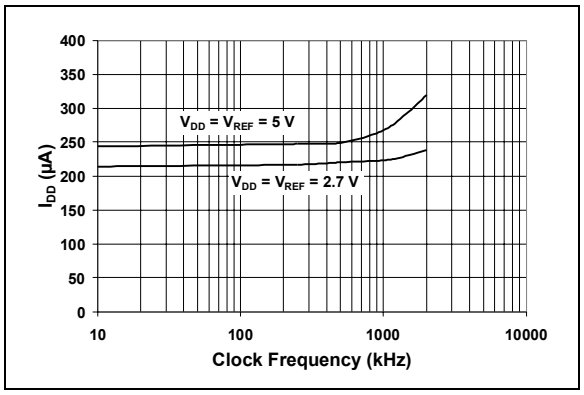



***FIGURE 2-32:*** *$I_{DD}$ vs. Clock Frequency.*

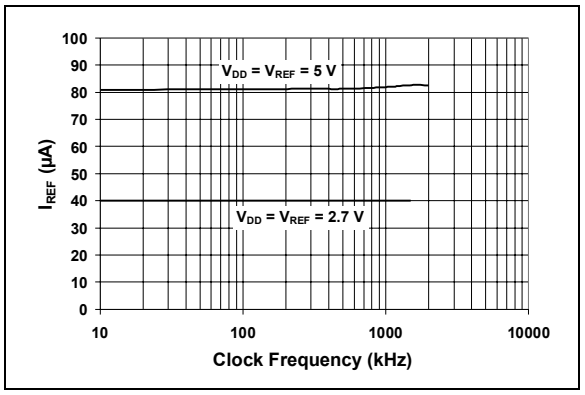



***FIGURE 2-35:*** *$I_{REF}$ vs. Clock Frequency.*

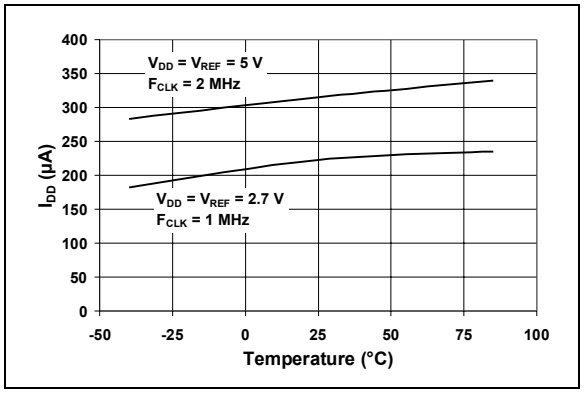



***FIGURE 2-33:*** *$I_{DD}$ vs. Temperature.*

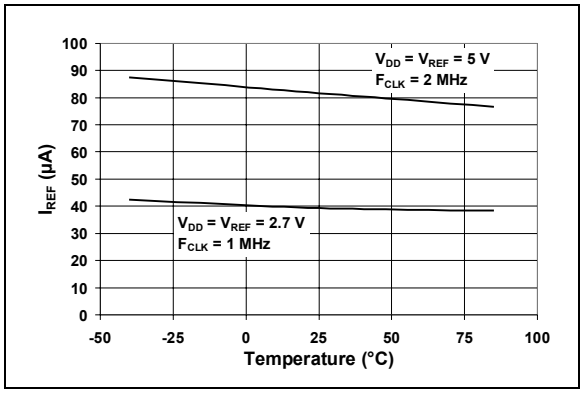



***FIGURE 2-36:*** *$I_{REF}$ vs. Temperature.*

**Note:** Unless otherwise indicated, $V_{DD} = V_{REF} = 5V$, $V_{SS} = 0V$, $f_{SAMPLE} = 100$ ksps, $f_{CLK} = 20^* f_{SAMPLE}$, $T_A = 25°C$.

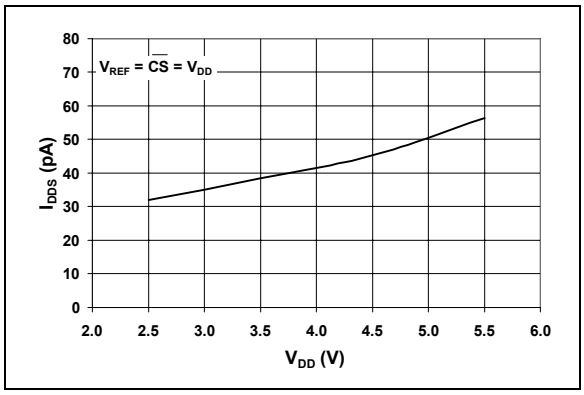



***FIGURE 2-37:*** *$I_{DDS}$ vs. $V_{DD}$.*

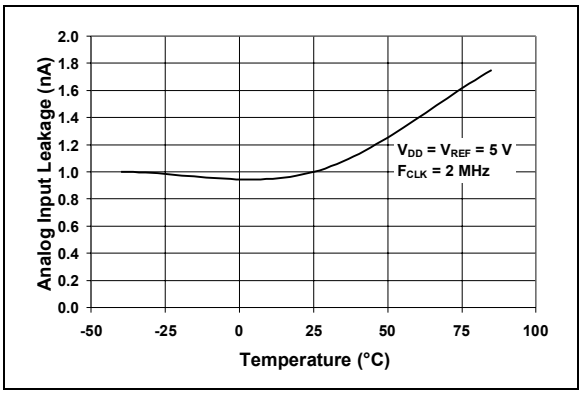



***FIGURE 2-39:*** *Analog Input Leakage Current vs. Temperature.*

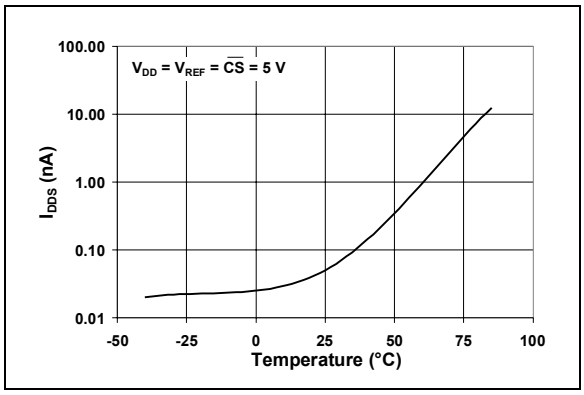



***FIGURE 2-38:*** *$I_{DDS}$ vs. Temperature.*

## 3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

**TABLE 3-1: PIN FUNCTION TABLE**

| Name | Function |
|---|---|
| $V_{DD}$ | +2.7V to 5.5V Power Supply |
| DGND | Digital Ground |
| AGND | Analog Ground |
| CH0-CH7 | Analog Inputs |
| CLK | Serial Clock |
| $D_{IN}$ | Serial Data In |
| $D_{OUT}$ | Serial Data Out |
| $\overline{CS}$/SHDN | Chip Select/Shutdown Input |
| $V_{REF}$ | Reference Voltage Input |

### 3.1 DGND

Digital ground connection to internal digital circuitry.

### 3.2 AGND

Analog ground connection to internal analog circuitry.

### 3.3 CH0 - CH7

Analog inputs for channels 0 - 7 for the multiplexed inputs. Each pair of channels can be programmed to be used as two independent channels in single-ended mode or as a single pseudo-differential input, where one channel is IN+ and one channel is IN. See Section 4.1, “Analog Inputs”, and Section 5.0, “Serial Communications”, for information on programming the channel configuration.

### 3.4 Serial Clock (CLK)

The SPI clock pin is used to initiate a conversion and clock out each bit of the conversion as it takes place. See Section 6.2, “Maintaining Minimum Clock Speed”, for constraints on clock speed.

### 3.5 Serial Data Input ($D_{IN}$)

The SPI port serial data input pin is used to load channel configuration data into the device.

### 3.6 Serial Data Output ($D_{OUT}$)

The SPI serial data output pin is used to shift out the results of the A/D conversion. Data will always change on the falling edge of each clock as the conversion takes place.

### 3.7 Chip Select/Shutdown ($\overline{CS}$/SHDN)

The $\overline{CS}$/SHDN pin is used to initiate communication with the device when pulled low and will end a conversion and put the device in low power standby when pulled high. The $\overline{CS}$/SHDN pin must be pulled high between conversions.

## 4.0 DEVICE OPERATION

The MCP3204/3208 A/D converters employ a conventional SAR architecture. With this architecture, a sample is acquired on an internal sample/hold capacitor for 1.5 clock cycles starting on the fourth rising edge of the serial clock after the start bit has been received. Following this sample time, the device uses the collected charge on the internal sample/hold capacitor to produce a serial 12-bit digital output code. Conversion rates of 100 ksps are possible on the MCP3204/3208. See Section 6.2, “Maintaining Minimum Clock Speed”, for information on minimum clock rates. Communication with the device is accomplished using a 4-wire SPI-compatible interface.

### 4.1 Analog Inputs

The MCP3204/3208 devices offer the choice of using the analog input channels configured as single-ended inputs or pseudo-differential pairs. The MCP3204 can be configured to provide two pseudo-differential input pairs or four single-ended inputs, while the MCP3208 can be configured to provide four pseudo-differential input pairs or eight single-ended inputs. Configuration is done as part of the serial command before each conversion begins. When used in the pseudo-differential mode, each channel pair (i.e., CH0 and CH1, CH2 and CH3 etc.) is programmed to be the IN+ and IN- inputs as part of the command string transmitted to the device. The IN+ input can range from IN- to ($V_{REF}$ + IN-). The IN- input is limited to ±100 mV from the $V_{SS}$ rail. The IN- input can be used to cancel small signal common-mode noise which is present on both the IN+ and IN- inputs.

When operating in the pseudo-differential mode, if the voltage level of IN+ is equal to or less than IN-, the resultant code will be 000h. If the voltage at IN+ is equal to or greater than {[$V_{REF}$ + (IN-)] - 1 LSB}, then the output code will be FFFh. If the voltage level at IN- is more than 1 LSB below $V_{SS}$, the voltage level at the IN+ input will have to go below $V_{SS}$ to see the 000h output code. Conversely, if IN- is more than 1 LSB above $V_{SS}$, then the FFFh code will not be seen unless the IN+ input level goes above $V_{REF}$ level.

For the A/D converter to meet specification, the charge holding capacitor ($C_{SAMPLE}$) must be given enough time to acquire a 12-bit accurate voltage level during the 1.5 clock cycle sampling period. The analog input model is shown in Figure 4-1.

This diagram illustrates that the source impedance ($R_S$) adds to the internal sampling switch ($R_{SS}$) impedance, directly effecting the time that is required to charge the capacitor (Csample). Consequently, larger source impedances increase the offset, gain and integral linearity errors of the conversion (see Figure 4-2).

## 4.2 Reference Input

For each device in the family, the reference input ($V_{REF}$) determines the analog input voltage range. As the reference input is reduced, the LSB size is reduced accordingly. The theoretical digital output code produced by the A/D converter is a function of the analog input signal and the reference input, as shown below.

**EQUATION**

$$Digital\ Output\ Code = \frac{4096 \times V_{IN}}{V_{REF}}$$

$V_{IN}$ = analog input voltage
$V_{REF}$ = reference voltage

When using an external voltage reference device, the system designer should always refer to the manufacturer's recommendations for circuit layout. Any instability in the operation of the reference device will have a direct effect on the operation of the A/D converter.

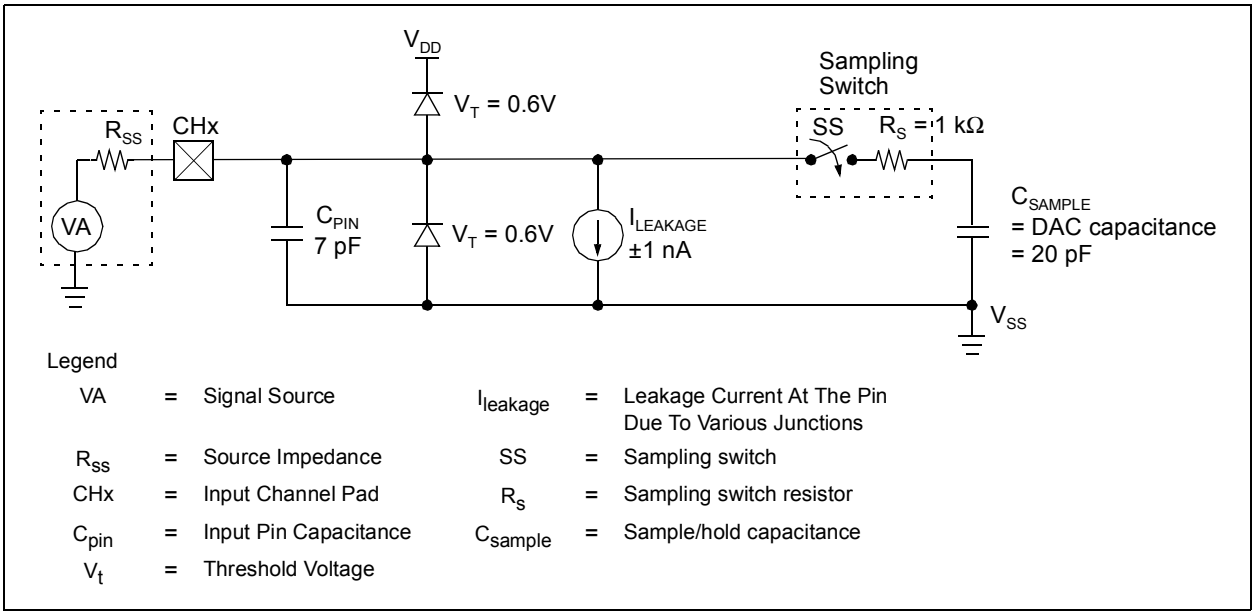



***FIGURE 4-1:*** *Analog Input Model.*

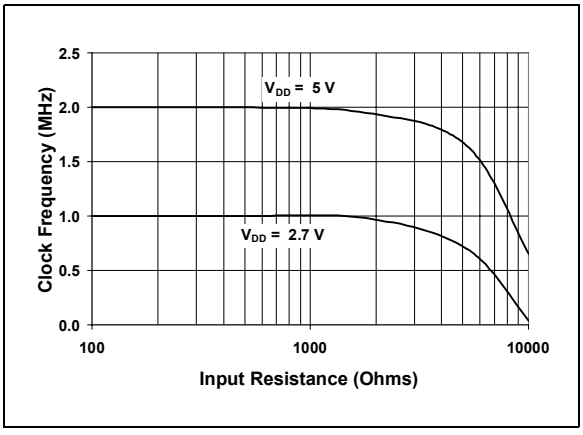



***FIGURE 4-2:*** *Maximum Clock Frequency vs. Input resistance ($R_S$) to maintain less than a 0.1 LSB deviation in INL from nominal conditions.*

## 5.0 SERIAL COMMUNICATIONS

Communication with the MCP3204/3208 devices is accomplished using a standard SPI-compatible serial interface. Initiating communication with either device is done by bringing the $\overline{CS}$ line low (see Figure 5-1). If the device was powered up with the $\overline{CS}$ pin low, it must be brought high and back low to initiate communication. The first clock received with $\overline{CS}$ low and $D_{IN}$ high will constitute a start bit. The SGL/$\overline{DIFF}$ bit follows the start bit and will determine if the conversion will be done using single-ended or differential input mode. The next three bits (D0, D1 and D2) are used to select the input channel configuration. Table 5-1 and Table 5-2 show the configuration bits for the MCP3204 and MCP3208, respectively. The device will begin to sample the analog input on the fourth rising edge of the clock after the start bit has been received. The sample period will end on the falling edge of the fifth clock following the start bit.

Once the D0 bit is input, one more clock is required to complete the sample and hold period ($D_{IN}$ is a "don't care" for this clock). On the falling edge of the next clock, the device will output a low null bit. The next 12 clocks will output the result of the conversion with MSB first, as shown in Figure 5-1. Data is always output from the device on the falling edge of the clock. If all 12 data bits have been transmitted and the device continues to receive clocks while the $\overline{CS}$ is held low, the device will output the conversion result LSB first, as shown in Figure 5-2. If more clocks are provided to the device while $\overline{CS}$ is still low (after the LSB first data has been transmitted), the device will clock out zeros indefinitely.

If necessary, it is possible to bring $\overline{CS}$ low and clock in leading zeros on the $D_{IN}$ line before the start bit. This is often done when dealing with microcontroller-based SPI ports that must send 8 bits at a time. Refer to Section 6.1 for more details on using the MCP3204/3208 devices with hardware SPI ports.

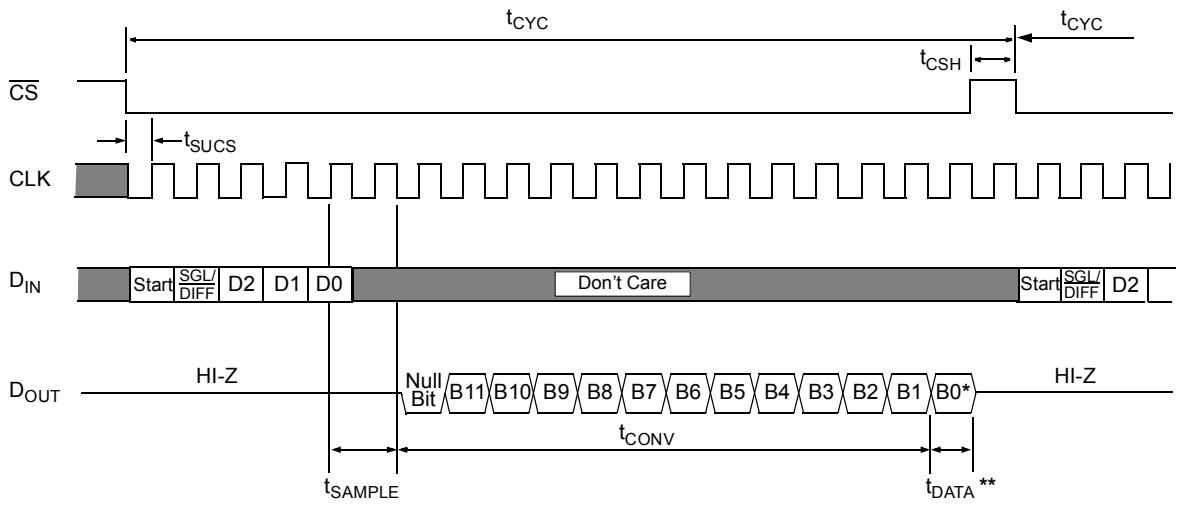
**TABLE 5-1: CONFIGURATION BITS FOR THE MCP3204**

| Control Bit Selections | | | | Input Configuration | Channel Selection |
|---|---|---|---|---|---|
| Single/Diff | D2* | D1 | D0 | | |
| 1 | X | 0 | 0 | single-ended | CH0 |
| 1 | X | 0 | 1 | single-ended | CH1 |
| 1 | X | 1 | 0 | single-ended | CH2 |
| 1 | X | 1 | 1 | single-ended | CH3 |
| 0 | X | 0 | 0 | differential | CH0 = IN+ CH1 = IN- |
| 0 | X | 0 | 1 | differential | CH0 = IN- CH1 = IN+ |
| 0 | X | 1 | 0 | differential | CH2 = IN+ CH3 = IN- |
| 0 | X | 1 | 1 | differential | CH2 = IN- CH3 = IN+ |

* D2 is a "don't care" for MCP3204

**TABLE 5-2: CONFIGURATION BITS FOR THE MCP3208**

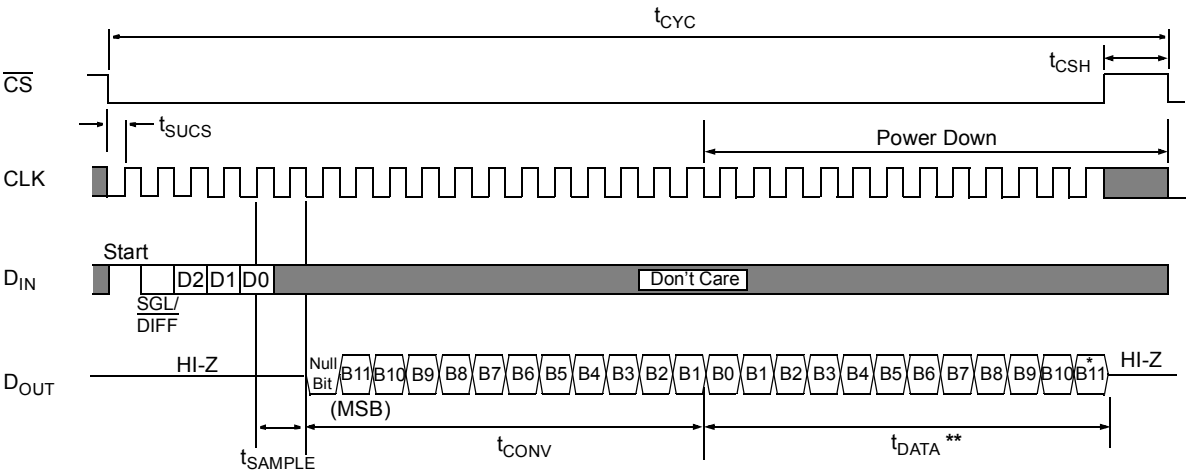
| Control Bit Selections | | | | Input Configuration | Channel Selection |
|---|---|---|---|---|---|
| Single /Diff | D2 | D1 | D0 | | |
| 1 | 0 | 0 | 0 | single-ended | CH0 |
| 1 | 0 | 0 | 1 | single-ended | CH1 |
| 1 | 0 | 1 | 0 | single-ended | CH2 |
| 1 | 0 | 1 | 1 | single-ended | CH3 |
| 1 | 1 | 0 | 0 | single-ended | CH4 |
| 1 | 1 | 0 | 1 | single-ended | CH5 |
| 1 | 1 | 1 | 0 | single-ended | CH6 |
| 1 | 1 | 1 | 1 | single-ended | CH7 |
| 0 | 0 | 0 | 0 | differential | CH0 = IN+ CH1 = IN- |
| 0 | 0 | 0 | 1 | differential | CH0 = IN- CH1 = IN+ |
| 0 | 0 | 1 | 0 | differential | CH2 = IN+ CH3 = IN- |
| 0 | 0 | 1 | 1 | differential | CH2 = IN- CH3 = IN+ |
| 0 | 1 | 0 | 0 | differential | CH4 = IN+ CH5 = IN- |
| 0 | 1 | 0 | 1 | differential | CH4 = IN- CH5 = IN+ |
| 0 | 1 | 1 | 0 | differential | CH6 = IN+ CH7 = IN- |
| 0 | 1 | 1 | 1 | differential | CH6 = IN- CH7 = IN+ |




* After completing the data transfer, if further clocks are applied with $\overline{CS}$ low, the A/D converter will output LSB first data, followed by zeros indefinitely (see Figure 5-2 below).

** $t_{DATA}$: during this time, the bias current and the comparator power down while the reference input becomes a high impedance node, leaving the CLK running to clock out the LSB-first data or zeros.

***FIGURE 5-1:*** *Communication with the MCP3204 or MCP3208.*




* After completing the data transfer, if further clocks are applied with $\overline{CS}$ low, the A/D converter will output zeros indefinitely.

** $t_{DATA}$: During this time, the bias circuit and the comparator power down while the reference input becomes a high impedance node, leaving the CLK running to clock out LSB first data or zeroes.

***FIGURE 5-2:*** *Communication with MCP3204 or MCP3208 in LSB First Format.*

# 6.0 APPLICATIONS INFORMATION

## 6.1 Using the MCP3204/3208 with Microcontroller (MCU) SPI Ports

With most microcontroller SPI ports, it is required to send groups of eight bits. It is also required that the microcontroller SPI port be configured to clock out data on the falling edge of clock and latch data in on the rising edge. Because communication with the MCP3204/3208 devices may not need multiples of eight clocks, it will be necessary to provide more clocks than are required. This is usually done by sending 'leading zeros' before the start bit. As an example, Figure 6-1 and Figure 6-2 illustrate how the MCP3204/3208 can be interfaced to a MCU with a hardware SPI port. Figure 6-1 depicts the operation shown in SPI Mode 0,0, which requires that the SCLK from the MCU idles in the 'low' state, while Figure 6-2 shows the similar case of SPI Mode 1,1, where the clock idles in the 'high' state.

As is shown in Figure 6-1, the first byte transmitted to the A/D converter contains five leading zeros before the start bit. Arranging the leading zeros this way allows the output 12 bits to fall in positions easily manipulated by the MCU. The MSB is clocked out of the A/D converter on the falling edge of clock number 12. Once the second eight clocks have been sent to the device, the MCU's receive buffer will contain three unknown bits (the output is at high impedance for the first two clocks), the null bit and the highest order four bits of the conversion. Once the third byte has been sent to the device, the receive register will contain the lowest order eight bits of the conversion results. Employing this method ensures simpler manipulation of the converted data.

Figure 6-2 shows the same thing in SPI Mode 1,1, which requires that the clock idles in the high state. As with mode 0,0, the A/D converter outputs data on the falling edge of the clock and the MCU latches data from the A/D converter in on the rising edge of the clock.

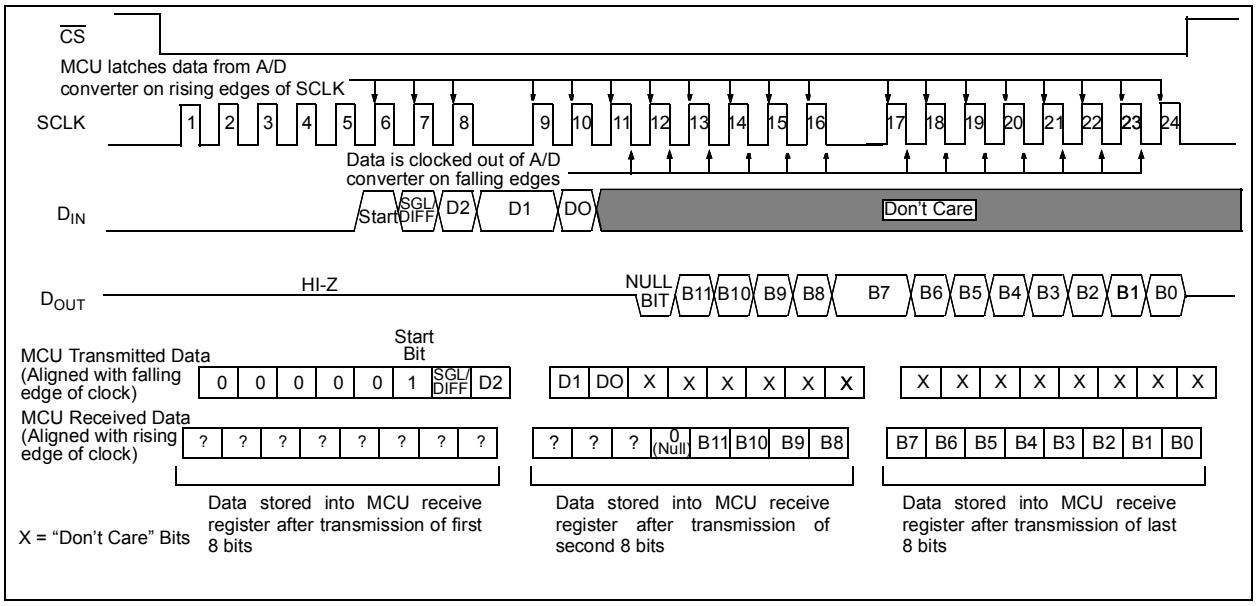



***FIGURE 6-1:*** *SPI Communication using 8-bit segments (Mode 0,0: SCLK idles low).*

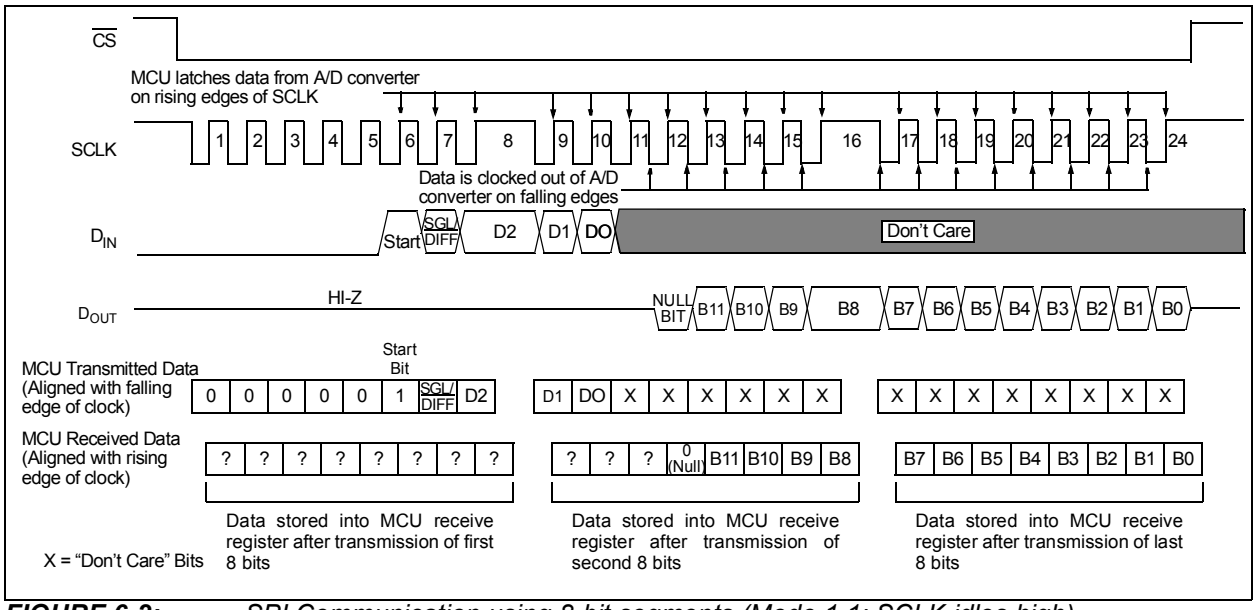



***FIGURE 6-2:*** *SPI Communication using 8-bit segments (Mode 1,1: SCLK idles high).*

## 6.2 Maintaining Minimum Clock Speed

When the MCP3204/3208 initiates the sample period, charge is stored on the sample capacitor. When the sample period is complete, the device converts one bit for each clock that is received. It is important for the user to note that a slow clock rate will allow charge to bleed off the sample capacitor while the conversion is taking place. At 85°C (worst case condition), the part will maintain proper charge on the sample capacitor for at least 1.2 ms after the sample period has ended. This means that the time between the end of the sample period and the time that all 12 data bits have been clocked out must not exceed 1.2 ms (effective clock frequency of 10 kHz). Failure to meet this criterion may introduce linearity errors into the conversion outside the rated specifications. It should be noted that during the entire conversion cycle, the A/D converter does not require a constant clock speed or duty cycle, as long as all timing specifications are met.

## 6.3 Buffering/Filtering the Analog Inputs

If the signal source for the A/D converter is not a low impedance source, it will have to be buffered or inaccurate conversion results may occur (see Figure 4-2). It is also recommended that a filter be used to eliminate any signals that may be aliased back into the conversion results, as is illustrated in Figure 6-3, where an op amp is used to drive the analog input of the MCP3204/3208. This amplifier provides a low impedance source for the converter input, and a low pass filter, which eliminates unwanted high frequency noise.

Low pass (anti-aliasing) filters can be designed using Microchip's free interactive FilterLab™ software. FilterLab will calculate capacitor and resistor values, as well as determine the number of poles that are required for the application. For more information on filtering signals, see AN699, *"Anti-Aliasing Analog Filters for Data Acquisition Systems"*.

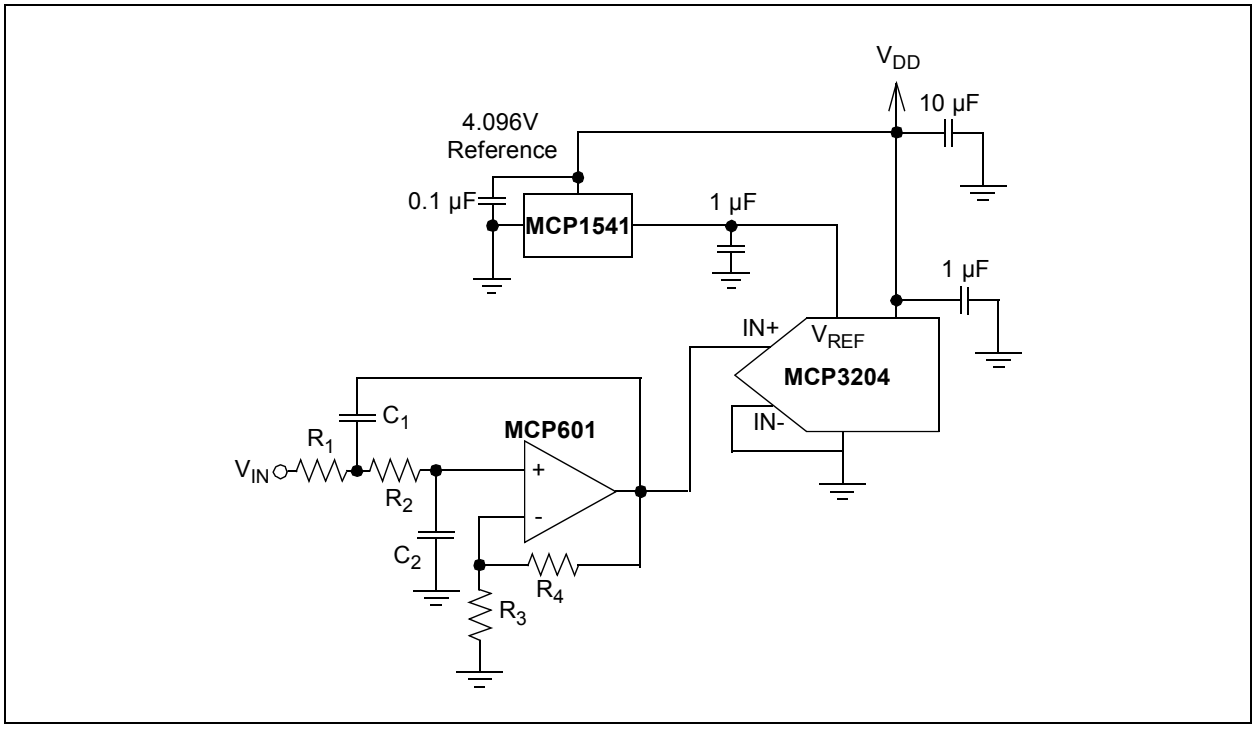



***FIGURE 6-3:*** *The MCP601 Operational Amplifier is used to implement a second order anti-aliasing filter for the signal being converted by the MCP3204.*

## 6.4 Layout Considerations

When laying out a printed circuit board for use with analog components, care should be taken to reduce noise wherever possible. A bypass capacitor should always be used with this device, placed as close as possible to the device pin. A bypass capacitor value of 1 µF is recommended.

Digital and analog traces should be separated as much as possible on the board, with no traces running underneath the device or the bypass capacitor. Extra precautions should be taken to keep traces with high frequency signals (such as clock lines) as far as possible from analog traces.

Use of an analog ground plane is recommended in order to keep the ground potential the same for all devices on the board. Providing $V_{DD}$ connections to devices in a "star" configuration can also reduce noise by eliminating return current paths and associated errors (see Figure 6-4). For more information on layout tips when using A/D converters, refer to AN688, *"Layout Tips for 12-Bit A/D converter Applications"*.

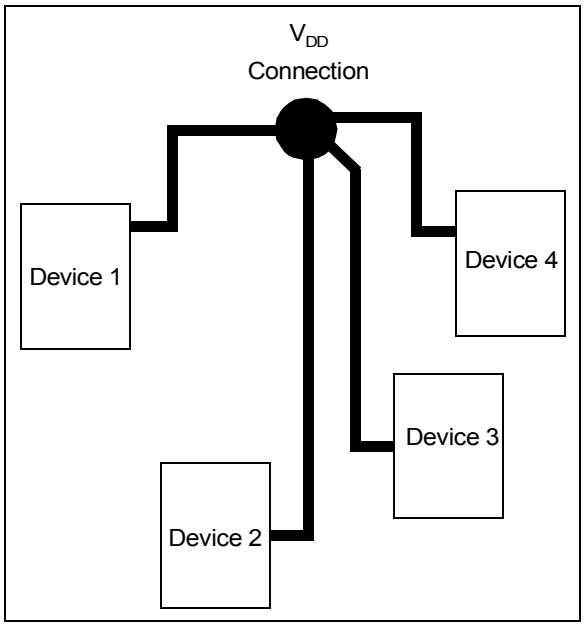



***FIGURE 6-4:*** *$V_{DD}$ traces arranged in a 'Star' configuration in order to reduce errors caused by current return paths.*

## 6.5 Utilizing the Digital and Analog Ground Pins

The MCP3204/3208 devices provide both digital and analog ground connections to provide another means of noise reduction. As shown in Figure 6-5, the analog and digital circuitry is separated internal to the device. This reduces noise from the digital portion of the device being coupled into the analog portion of the device. The two grounds are connected internally through the substrate, which has a resistance of 5 -10Ω.

If no ground plane is utilized, then both grounds must be connected to $V_{SS}$ on the board. If a ground plane is available, both digital and analog ground pins should be connected to the analog ground plane. If both an analog and a digital ground plane are available, both the digital and the analog ground pins should be connected to the analog ground plane. Following these steps will reduce the amount of digital noise from the rest of the board being coupled into the A/D converter.

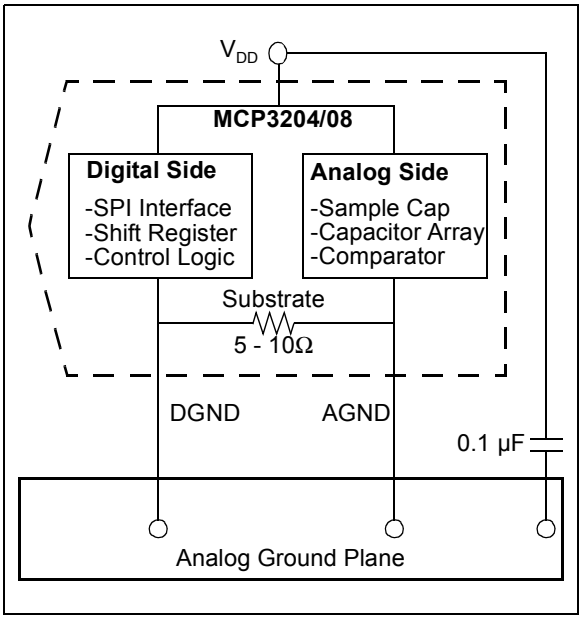
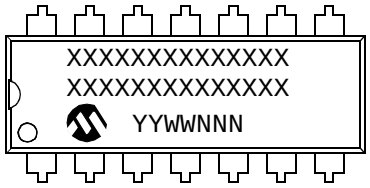



***FIGURE 6-5:*** *Separation of Analog and Digital Ground Pins.*

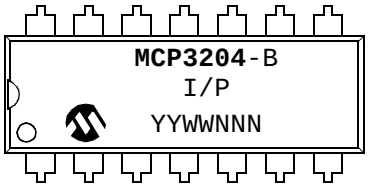
## 7.0 PACKAGING INFORMATION

### 7.1 Package Marking Information

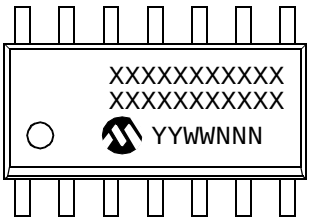
14-Lead PDIP (300 mil)



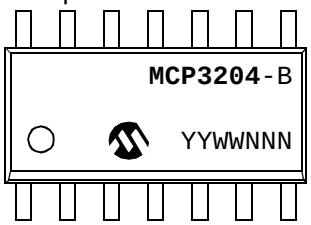

Example:



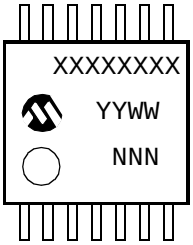

14-Lead SOIC (150 mil)



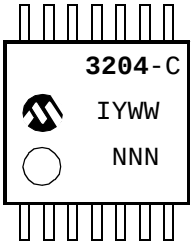

Example:




14-Lead TSSOP (4.4mm) *




Example:




* Please contact Microchip Factory for B-Grade TSSOP devices

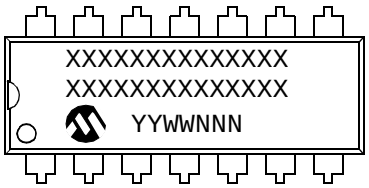
| | | |
|---|---|---|
| **Legend:** | XX...X | Customer specific information* |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |

**Note**: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

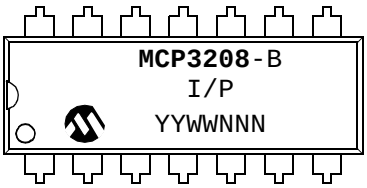
* Standard marking consists of Microchip part number, year code, week code, traceability code (facility code, mask rev#, and assembly code). For marking beyond this, certain price adders apply. Please check with your Microchip Sales Office.

**Package Marking Information (Continued)**

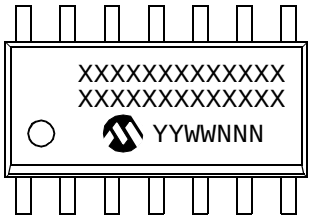
16-Lead PDIP (300 mil) (**MCP3304**)



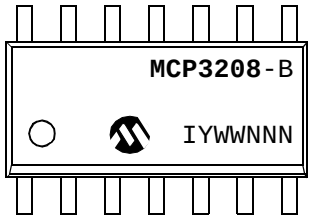

Example:



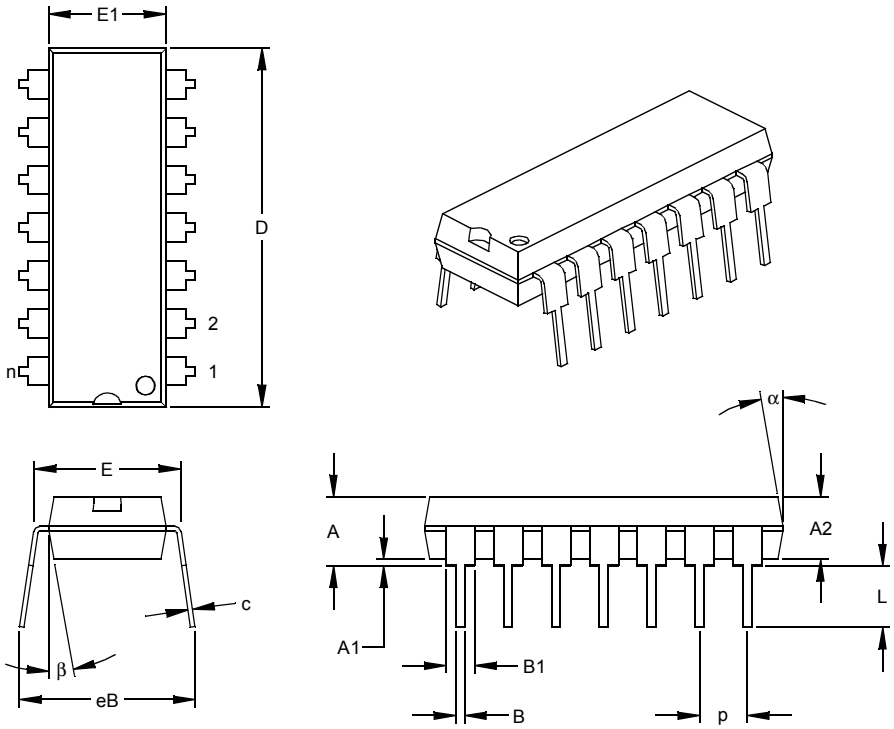

16-Lead SOIC (150 mil) (**MCP3304**)




Example:



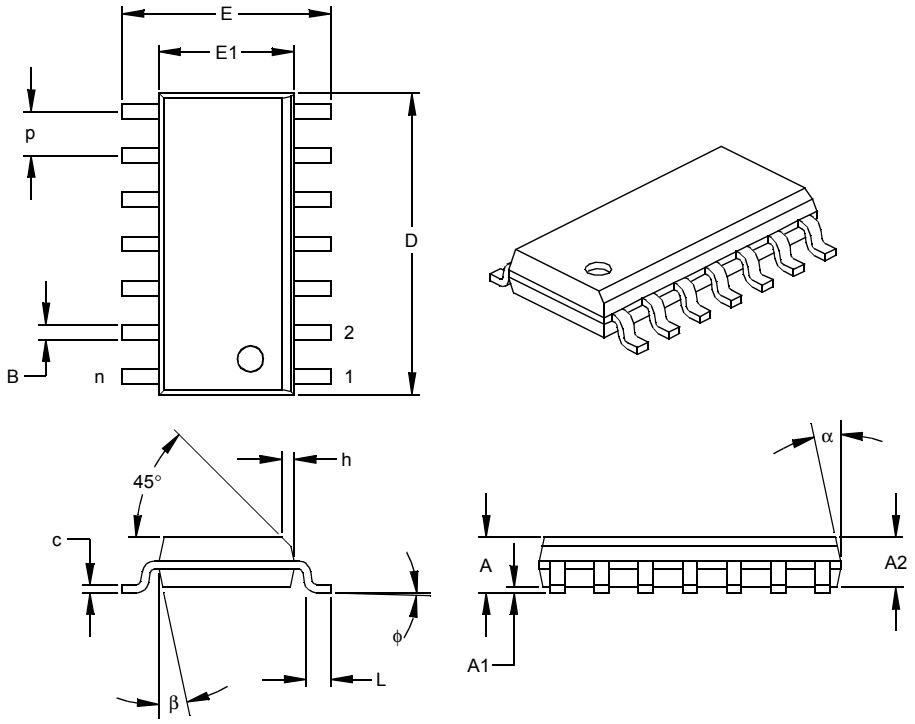
**14-Lead Plastic Dual In-line (P) – 300 mil (PDIP)**




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 14 | | | 14 | |
| Pitch | p | | .100 | | | 2.54 | |
| Top to Seating Plane | A | .140 | .155 | .170 | 3.56 | 3.94 | 4.32 |
| Molded Package Thickness | A2 | .115 | .130 | .145 | 2.92 | 3.30 | 3.68 |
| Base to Seating Plane | A1 | .015 | | | 0.38 | | |
| Shoulder to Shoulder Width | E | .300 | .313 | .325 | 7.62 | 7.94 | 8.26 |
| Molded Package Width | E1 | .240 | .250 | .260 | 6.10 | 6.35 | 6.60 |
| Overall Length | D | .740 | .750 | .760 | 18.80 | 19.05 | 19.30 |
| Tip to Seating Plane | L | .125 | .130 | .135 | 3.18 | 3.30 | 3.43 |
| Lead Thickness | c | .008 | .012 | .015 | 0.20 | 0.29 | 0.38 |
| Upper Lead Width | B1 | .045 | .058 | .070 | 1.14 | 1.46 | 1.78 |
| Lower Lead Width | B | .014 | .018 | .022 | 0.36 | 0.46 | 0.56 |
| Overall Row Spacing § | eB | .310 | .370 | .430 | 7.87 | 9.40 | 10.92 |
| Mold Draft Angle Top | α | 5 | 10 | 15 | 5 | 10 | 15 |
| Mold Draft Angle Bottom | β | 5 | 10 | 15 | 5 | 10 | 15 |

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-005

**14-Lead Plastic Small Outline (SL) – Narrow, 150 mil (SOIC)**

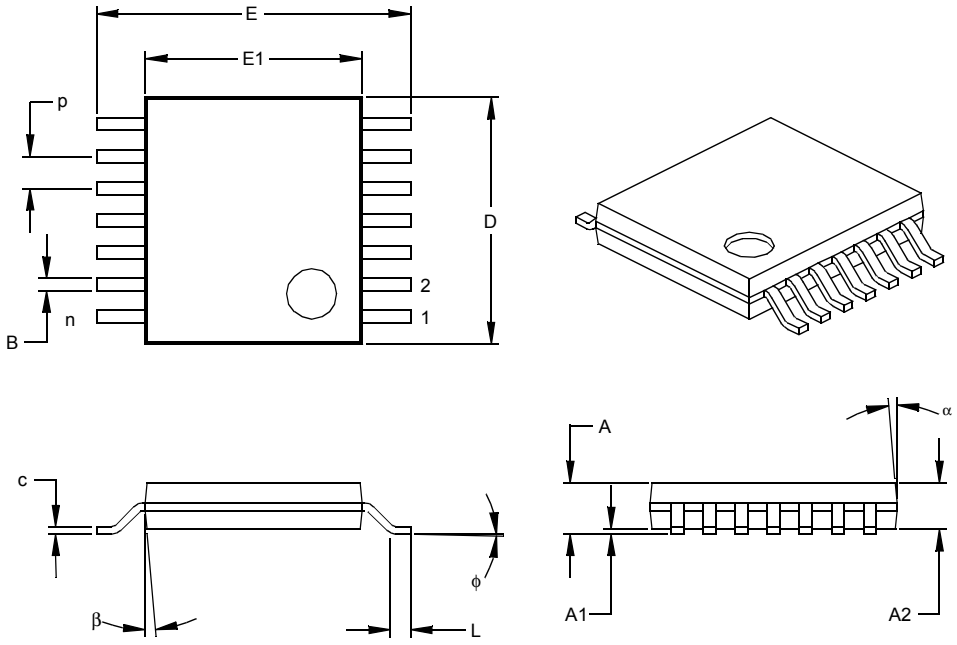



| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 14 | | | 14 | |
| Pitch | p | | .050 | | | 1.27 | |
| Overall Height | A | .053 | .061 | .069 | 1.35 | 1.55 | 1.75 |
| Molded Package Thickness | A2 | .052 | .056 | .061 | 1.32 | 1.42 | 1.55 |
| Standoff § | A1 | .004 | .007 | .010 | 0.10 | 0.18 | 0.25 |
| Overall Width | E | .228 | .236 | .244 | 5.79 | 5.99 | 6.20 |
| Molded Package Width | E1 | .150 | .154 | .157 | 3.81 | 3.90 | 3.99 |
| Overall Length | D | .337 | .342 | .347 | 8.56 | 8.69 | 8.81 |
| Chamfer Distance | h | .010 | .015 | .020 | 0.25 | 0.38 | 0.51 |
| Foot Length | L | .016 | .033 | .050 | 0.41 | 0.84 | 1.27 |
| Foot Angle | φ | 0 | 4 | 8 | 0 | 4 | 8 |
| Lead Thickness | c | .008 | .009 | .010 | 0.20 | 0.23 | 0.25 |
| Lead Width | B | .014 | .017 | .020 | 0.36 | 0.42 | 0.51 |
| Mold Draft Angle Top | α | 0 | 12 | 15 | 0 | 12 | 15 |
| Mold Draft Angle Bottom | β | 0 | 12 | 15 | 0 | 12 | 15 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-065

**14-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm (TSSOP)**

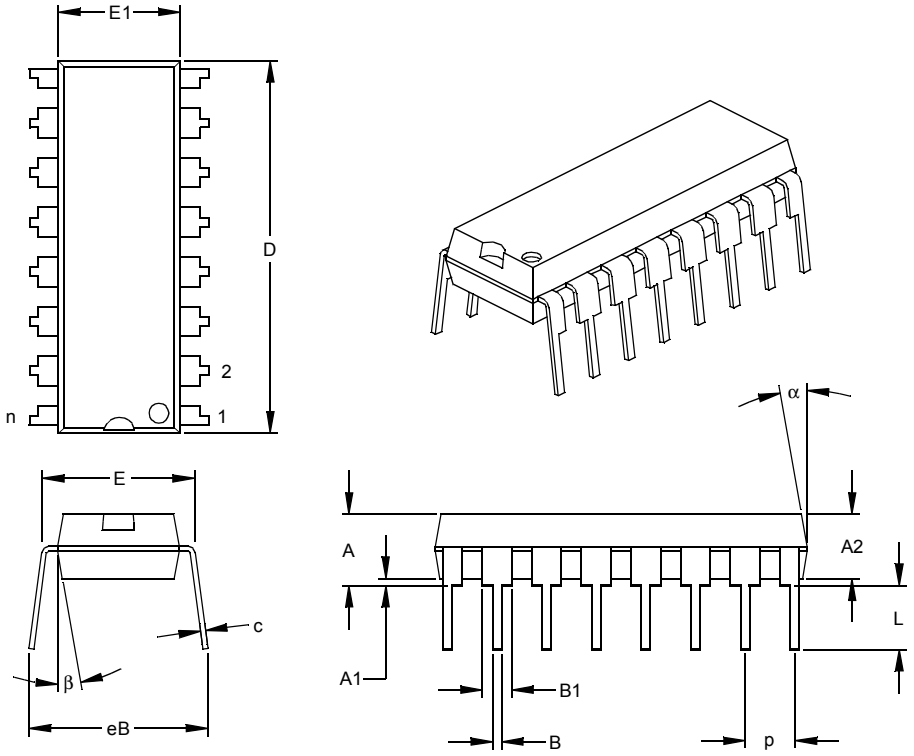



| Units | | INCHES | | | MILLIMETERS* | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 14 | | | 14 | |
| Pitch | p | | .026 | | | 0.65 | |
| Overall Height | A | | | .043 | | | 1.10 |
| Molded Package Thickness | A2 | .033 | .035 | .037 | 0.85 | 0.90 | 0.95 |
| Standoff § | A1 | .002 | .004 | .006 | 0.05 | 0.10 | 0.15 |
| Overall Width | E | .246 | .251 | .256 | 6.25 | 6.38 | 6.50 |
| Molded Package Width | E1 | .169 | .173 | .177 | 4.30 | 4.40 | 4.50 |
| Molded Package Length | D | .193 | .197 | .201 | 4.90 | 5.00 | 5.10 |
| Foot Length | L | .020 | .024 | .028 | 0.50 | 0.60 | 0.70 |
| Foot Angle | φ | 0 | 4 | 8 | 0 | 4 | 8 |
| Lead Thickness | c | .004 | .006 | .008 | 0.09 | 0.15 | 0.20 |
| Lead Width | B1 | .007 | .010 | .012 | 0.19 | 0.25 | 0.30 |
| Mold Draft Angle Top | α | 0 | 5 | 10 | 0 | 5 | 10 |
| Mold Draft Angle Bottom | β | 0 | 5 | 10 | 0 | 5 | 10 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005” (0.127mm) per side.
JEDEC Equivalent: MO-153
Drawing No. C04-087

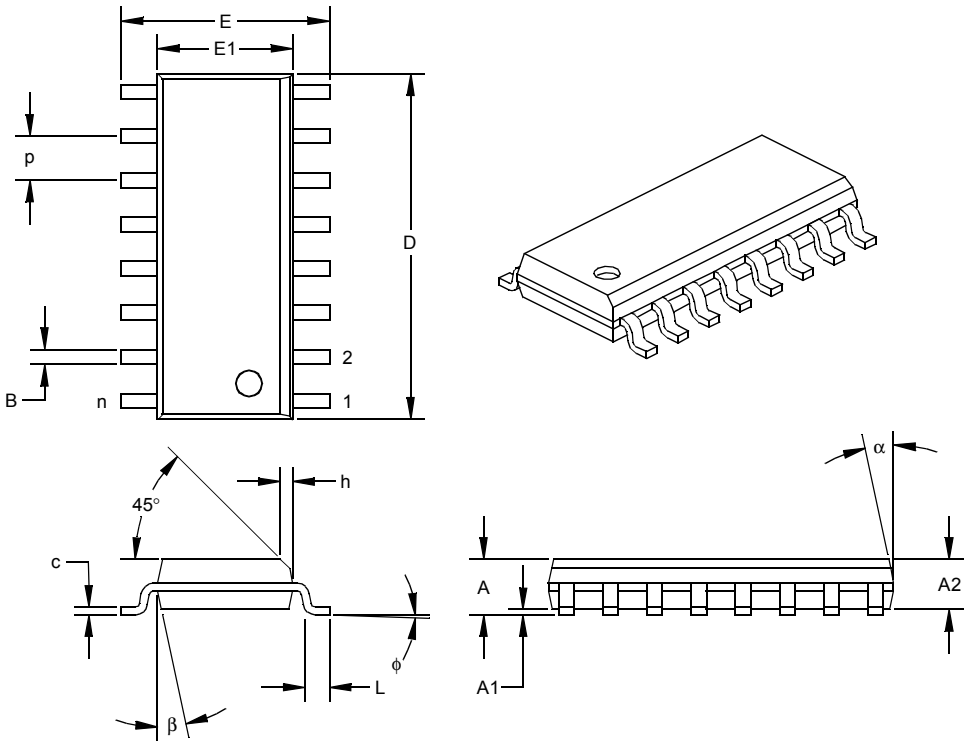
### 16-Lead Plastic Dual In-line (P) – 300 mil (PDIP)




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 16 | | | 16 | |
| Pitch | p | | .100 | | | 2.54 | |
| Top to Seating Plane | A | .140 | .155 | .170 | 3.56 | 3.94 | 4.32 |
| Molded Package Thickness | A2 | .115 | .130 | .145 | 2.92 | 3.30 | 3.68 |
| Base to Seating Plane | A1 | .015 | | | 0.38 | | |
| Shoulder to Shoulder Width | E | .300 | .313 | .325 | 7.62 | 7.94 | 8.26 |
| Molded Package Width | E1 | .240 | .250 | .260 | 6.10 | 6.35 | 6.60 |
| Overall Length | D | .740 | .750 | .760 | 18.80 | 19.05 | 19.30 |
| Tip to Seating Plane | L | .125 | .130 | .135 | 3.18 | 3.30 | 3.43 |
| Lead Thickness | c | .008 | .012 | .015 | 0.20 | 0.29 | 0.38 |
| Upper Lead Width | B1 | .045 | .058 | .070 | 1.14 | 1.46 | 1.78 |
| Lower Lead Width | B | .014 | .018 | .022 | .036 | 0.46 | 0.56 |
| Overall Row Spacing § | eB | .310 | .370 | .430 | 7.87 | 9.40 | 10.92 |
| Mold Draft Angle Top | α | 5 | 10 | 15 | 5 | 10 | 15 |
| Mold Draft Angle Bottom | β | 5 | 10 | 15 | 5 | 10 | 15 |

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-001
Drawing No. C04-017

**16-Lead Plastic Small Outline (SL) – Narrow 150 mil (SOIC)**




| Units | | INCHES* | | | MILLIMETERS | | |
|---|---|---|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX | MIN | NOM | MAX |
| Number of Pins | n | | 16 | | | 16 | |
| Pitch | p | | .050 | | | 1.27 | |
| Overall Height | A | .053 | .061 | .069 | 1.35 | 1.55 | 1.75 |
| Molded Package Thickness | A2 | .052 | .057 | .061 | 1.32 | 1.44 | 1.55 |
| Standoff § | A1 | .004 | .007 | .010 | 0.10 | 0.18 | 0.25 |
| Overall Width | E | .228 | .237 | .244 | 5.79 | 6.02 | 6.20 |
| Molded Package Width | E1 | .150 | .154 | .157 | 3.81 | 3.90 | 3.99 |
| Overall Length | D | .386 | .390 | .394 | 9.80 | 9.91 | 10.01 |
| Chamfer Distance | h | .010 | .015 | .020 | 0.25 | 0.38 | 0.51 |
| Foot Length | L | .016 | .033 | .050 | 0.41 | 0.84 | 1.27 |
| Foot Angle | φ | 0 | 4 | 8 | 0 | 4 | 8 |
| Lead Thickness | c | .008 | .009 | .010 | 0.20 | 0.23 | 0.25 |
| Lead Width | B | .013 | .017 | .020 | 0.33 | 0.42 | 0.51 |
| Mold Draft Angle Top | α | 0 | 12 | 15 | 0 | 12 | 15 |
| Mold Draft Angle Bottom | β | 0 | 12 | 15 | 0 | 12 | 15 |

* Controlling Parameter
§ Significant Characteristic

Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MS-012
Drawing No. C04-108

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The file transfer site is available by using an FTP service to connect to:

**ftp://ftp.microchip.com**

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092002

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4. What additions to the document do you think would enhance the structure and subject?

5. What deletions from the document could be made without affecting the overall usefulness?

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7. How would you improve this document?

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| PART NO. | X | X | /XX |
|---|---|---|---|
| Device | Grade | Temperature Range | Package |

| | | |
|---|---|---|
| Device: | MCP3204: | 4-Channel 12-Bit Serial A/D Converter |
| | MCP3204T: | 4-Channel 12-Bit Serial A/D Converter (Tape and Reel) |
| | MCP3208: | 8-Channel 12-Bit Serial A/D Converter |
| | MCP3208T: | 8-Channel 12-Bit Serial A/D Converter (Tape and Reel) |
| Grade: | B = | ±1 LSB INL |
| | C = | ±2 LSB INL |
| Temperature Range: | I = | -40°C to +85°C |
| Package: | P = | Plastic DIP (300 mil Body), 14-lead, 16-lead |
| | SL = | Plastic SOIC (150 mil Body), 14-lead, 16-lead |
| | ST = | Plastic TSSOP (4.4mm), 14-lead |

**Examples:**

a) MCP3204-BI/P: ±1 LSB INL, Industrial Temperature, PDIP package.

b) MCP3204-BI/SL: ±1 LSB INL, Industrial Temperature, SOIC package.

c) MCP3204-CI/ST: ±2 LSB INL, Industrial Temperature, TSSOP package.

a) MCP3208-BI/P: ±1 LSB INL, Industrial Temperature, PDIP package.

b) MCP3208-BI/SL: ±1 LSB INL, Industrial Temperature, SOIC package.

c) MCP3208-CI/ST: ±2 LSB INL, Industrial Temperature, TSSOP package.

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