MCP250XX

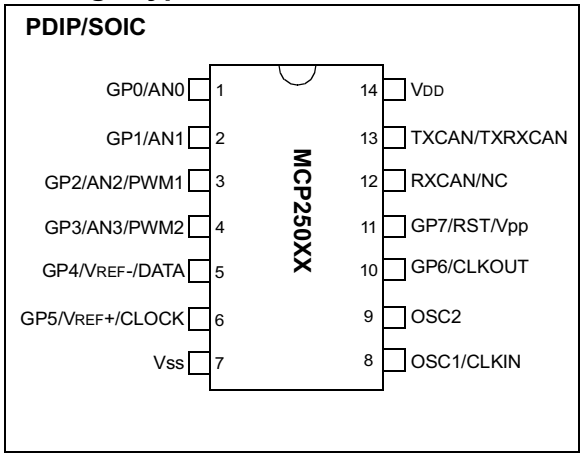
Programming Specifications

This document includes the programming specifications for the following devices:

- MCP25020
- MCP25025
- MCP25050
- MCP25055

Package Types:

PDIP/SOIC



1.0 OVERVIEW

This specification describes the requirements to program a device. Programming is accomplished through a serial interface. A serial interface reduces the number of device pins that must be controlled and eases the application requirements for the device to be programmed while in the users system. This capability increases design flexibility, and is referred to as In-Circuit Serial Programming™ (ICSP™).

1.1 Hardware Requirements

The MCP250XX requires two programmable power supplies, one for VDD (2.0V to 6.0V recommended) and one for VPP (12V to 14V). Both supplies should have a minimum resolution of 0.25V.

1.2 Programming Mode

The programming mode for the MCP250XX allows programming of user program memory and the configuration word.

2.0 MCP250XX MEMORY

The MCP250XX has two memory spaces. The first is the User EPROM Memory. This memory stores the default configuration values for the device. The second memory space is the configuration memory. This contains the values for the device oscillator and reset pin configurations.

2.1 User EPROM Memory Map

The User EPROM memory space extends from 0x00 to 0x45. Table 2-1 shows this program memory map.

This User EPROM memory is offset within the device memory map. When programming the device, an offset to the addresses in Table 2-1 is required.

Note 1: An offset of 0x10 is required to be added to the addresses shown in the User Program Memory Map (Table 2-1) when programming these locations. Therefore, there should be 16 Increment Address commands before programming the contents of the User EPROM Memory.

2: Do not program outside the specified user EPROM memory range or improper operation may occur.

2.2 Configuration Memory

Configuration memory is accessed with the Load Configuration command. Once in configuration memory, the only way to access the User EPROM Memory is to reset the device and re-enter Programming mode, as described in Section 3.1. Only the lower 3-bits should be programmed. The remaining 11-bits are reserved and should be programmed as a '1'. Programming these bits as a '1' will ensure that the factory value is not modified. When verifying this location, only verify against the lower 3-bits (the bits that were programmed).

TABLE 2-1: USER EPROM MEMORY MAP

Address (1)	Location Name	Address (1)	Location Name
00h	IOINTEN	23h	TXID0EID0
01h	IOINTPO	24h	TXID1SIDH
02h	GPLAT	25h	TXID1SIDL
03h	— (2)	26h	TXID1EID8
04h	OPTREG1	27h	TXID1EID0
05h	T1CON	28h	TXID2SIDH
06h	T2CON	29h	TXID2SIDL
07h	PR1	2Ah	TXID2EID8
08h	PR2	2Bh	TXID2EID0
09h	PWM1DCH	2Ch	ADCMP3H
0Ah	PWM2DCH	2Dh	ADCMP3L
0Bh	CNF1	2Eh	ADCMP2H
0Ch	CNF2	2Fh	ADCMP2L
0Dh	CNF3	30h	ADCMP1H
0Eh	ADCON0	31h	ADCMP1L
0Fh	ADCON1	32h	ADCMP0H
10h	STCON	33h	ADCMP0L
11h	OPTREG2	34h	GPDDR
12h	— (3)	35h	USER0
13h	— (3)	36h	USER1
14h	RXMSIDH	37h	USER2
15h	RXMSIDL	38h	USER3
16h	RXMEID8	39h	USER4
17h	RXMEID0	3Ah	USER5
18h	RXF0SIDH	3Bh	USER6
19h	RXF0SIDL	3Ch	USER7
1Ah	RXF0EID8	3Dh	USER8
1Bh	RXF0EID0	3Eh	USER9
1Ch	RXF1SIDH	3Fh	USERA
1Dh	RXF1SIDL	40h	USERB
1Eh	RXF1EID8	41h	USERC
1Fh	RXF1EID0	42h	USERD
20h	TXID0SIDH	43h	USERE
21h	TXID0SIDL	44h	USERF
22h	TXID0EID8	45h	CHKSUM

Note 1: An offset of 0x10 is required.

2: Reserved, Program this location as 0x34FF.

3: Unimplemented, Program this location as 0x34FF.

3.0 PROGRAMMING MODE ENTRY

A specific hardware sequence is required to force the device from the normal operating mode into Programming programming mode. After entering into the Programming mode, the 2-wire serial interface can be used to send the commands to the MCP250XX. These commands are discussed in Section 4.0.

3.1 Programming Entry Sequence

The Programming mode is entered by raising the $\overline{RST}$ pin from V_{IL} (Parameter PD8) to V_{IHH} (Parameter PD4). Then while holding the CLOCK and DATA pins (GP5 and GP4) low, raising V_{DD}.

Once in this mode, the User EPROM memory and the configuration memory can be accessed (read and programmed). The interface is serial and the CLOCK pin (GP5) is a Schmitt Trigger input in this mode.

The sequence that forces the device into the Programming mode also puts all other logic into the reset state (the $\overline{RST}$ pin was initially at V_{IL}). This means that all I/O are in the reset state (High impedance inputs).

Note 1: Do not power any I/O pins before V_{DD} is applied.

Figure 7-2 shows the waveform for entry into Programming mode.

3.2 Programming Operation

The CLOCK pin (GP5) is used as a clock input pin. The DATA pin (GP4) is used for entering command bits and data input/output during serial communication.

To input a command, the CLOCK pin (GP5) is cycled six times. Each command bit is latched on the falling edge of the clock with the least significant bit (LSb) of the command being input first. The data on the DATA pin (GP4) is required to have a minimum setup and hold time (see Parameter P3 and Parameter P4) with respect to the falling edge of the clock. Commands that have data associated with them (read and load) are specified to have a minimum delay between the command and the data (Parameter P6).

After this delay, the clock pin is cycled 16 times with the first cycle being a start bit and the last cycle being a stop bit. The data is input/output LSb first. During a read operation the LSb will be transmitted onto the DATA pin (GP4) on the rising edge of the second cycle, and during a load operation the LSb will be latched on the falling edge of the second cycle.

All commands and data words are transmitted LSb first. The DATA pin value is latched on the falling edge of the CLOCK pin. A minimum time between the command and the data word (or another command) is required. This separation time is shown in Parameter P6 of the Electrical Specification.

The commands that are available are listed in Table 4-1. The waveforms for these commands are shown in Figure 7-3 through Figure 7-8.

4.0 PROGRAMMING COMMANDS

There are six commands that the MCP250XX will execute when in Programming mode. These commands are shown in Table 4-1. Three of the commands have data that are required. The Load commands supply data to the MCP250XX, and the Read command retrieve data from the MCP250XX.

When the device enters into Programming mode, the address pointer is pointing to 0x00. The User Program Memory has an offset of 0x10. So before starting to program a desired location in the User Program Memory Map, the Increment Address command must be executed 16 times.

TABLE 4-1: PROGRAMMING COMMANDS

Command	Mapping (MSb ... LSb)	Data
Load Configuration	0 0 0 0 0 0	0, data(14), 0
Load Data	0 0 0 0 1 0	0,1,1,0,1,0,0,data(8),0
Read Data	0 0 0 1 0 0	0, data(14), 0
Increment Address	0 0 0 1 1 0	—
Begin Programming	0 0 1 0 0 0	—
End Programming	0 0 1 1 1 0	—

4.1 Load Configuration

After receiving this command, the address pointer points to the Configuration memory space. To address the MCP250xx Configuration word the Increment command must be given seven times (see Figure 4-2). Then by applying 16 clock cycles to the CLOCK pin, a 14-bit “data word” will be loaded into the Transfer Latch (ready to be programmed into the configuration word, see Register 5-1). Only the lower 3-bits of the “data word” should be programmed. The remaining 11-bits of the “data word” are reserved and should be programmed as a ‘1’. Programming these bits as a ‘1’ will ensure that the factory value is not modified. When verifying this location, only verify against the lower 3-bits (the bits that were programmed).

After the Load Configuration command is supplied, the only way to have the address pointer return to pointing at the User Program Memory is to exit the Programming mode. This is accomplished by taking the voltage on the $\overline{RST}$ pin to a low level (V_{IL}, Parameter PD8) and the re-entering into Programming mode (see Section 3.1).

Figure 7-3 shows the waveform for the Load Configuration command and Table 7-3 specifies the timing parameters that must be meet.

4.2 Load Data

After receiving this command, the chip will load in a 14-bit “data word” into the Transfer latch when 16 clock cycles are applied to the CLOCK pin.

Figure 7-4 shows the waveform for the Load Data command and Table 7-4 specifies the timing parameters that must be meet.

4.3 Read Data

After receiving this command (the first 6 bits), the device data word at the memory address currently accessed is loaded into the Transfer latch. Then as the Data is transmitted, the DATA (GP4) pin is automatically configured into an output on the second rising clock edge, and reverts back to an input (hi-impedance) after the 16th rising edge.

Figure 7-5 shows the waveform for the Read Data command and Table 7-5 specifies the timing parameters that must be meet.

This command is useful in the verify sequence of the programming algorithm. This is used to verify that if the value that was programmed at this location has been “well programmed”. That is, that the memory cell was able to retain the value previously written. A memory verification should be done at the minimum and maximum voltage that the device will experience within the application.

4.4 Increment Address

The address pointer is incremented when this command is received.

Figure 7-6 shows the waveform for the Increment Address command and Table 7-6 specifies the timing parameters that must be meet.

4.5 Begin Programming

Programming of the appropriate memory (User Program Memory or Configuration Memory) will begin after this command is received and decoded. This programming pulse will continue until an End Programming command is received. Each programming pulse should meet a minimum time duration (Parameter P11 in Electrical Specification's Table 7-7).

Note:	A load command (load configuration or load data) must be given before every Begin Programming command.

Programming should be performed with a series of programming pulses (Parameter P11). A programming pulse is defined as the time between the Begin Programming command and the End Programming command.

Figure 7-7 shows the waveform for the Begin Programming command and Table 7-7 specifies the timing parameters that must be met.

Example 4-1 shows a typical command sequence that would be used in the over programming of a device.

EXAMPLE 4-1: Command Sequence

Step	Command	Comment
1	Load Command	; Data or Configuration
2	Begin Programming	; Pulse #1 ; Wait required delay
3	End Programming	
4	Load Command	; Data or Configuration
5	Begin Programming	; Pulse #2 ; Wait required delay
6	End Programming	
:	:	; Repeat Load/Begin/ ; End Programming ; sequence as needed

4.6 End Programming

After receiving this command, the chip stops programming the memory (configuration program memory or user program memory) that it was programming at the time.

Figure 7-8 shows the waveform for the End Programming command and Table 7-8 specifies the timing parameters that must be met.

4.7 Programming Algorithm Requires Variable VDD

The algorithm calls for program verification at VDDmin as well as VDDmax. Verification at VDDmin guarantees good "erase margin". Verification at VDDmax guarantees good "program margin".

The actual programming must be done with VDD in the VDDP range (Parameter PD1).

VDDP = VDD range required during programming.

VDDV = VDD range required during verification.

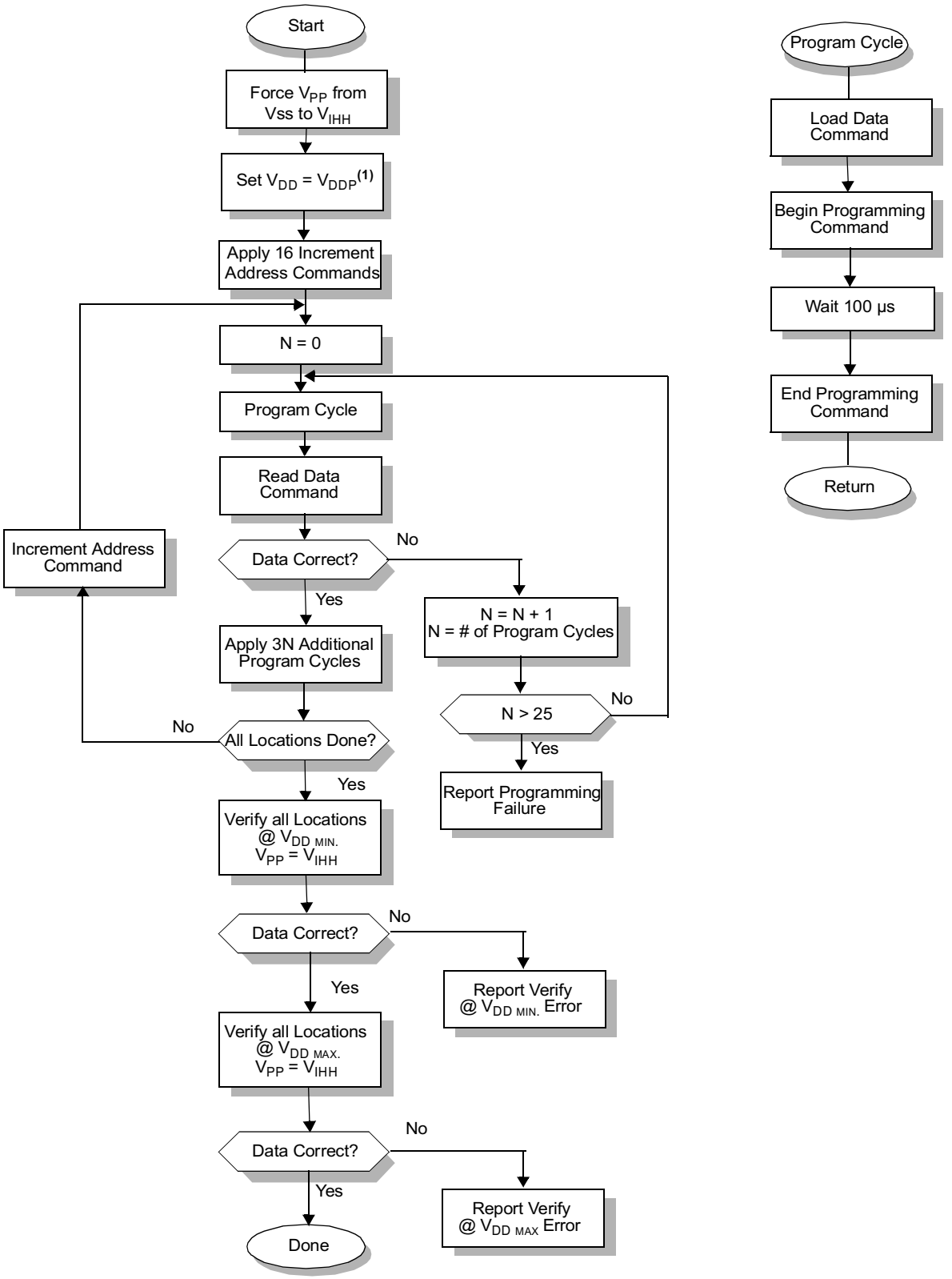
VDDMIN = Minimum operating VDD specification for the device.

VDDMAX = Maximum operating VDD specification for the device.

Programmers must verify the MCP250XX at its specified VDDMAX and VDDMIN levels. Since Microchip may introduce future versions of the MCP250XX with a broader VDD range, it is best that these levels are user selectable (defaults are ok).

Note:	Any programmer not meeting these requirements may only be classified as "prototype" or "development" programmer but not a "production" quality programmer.

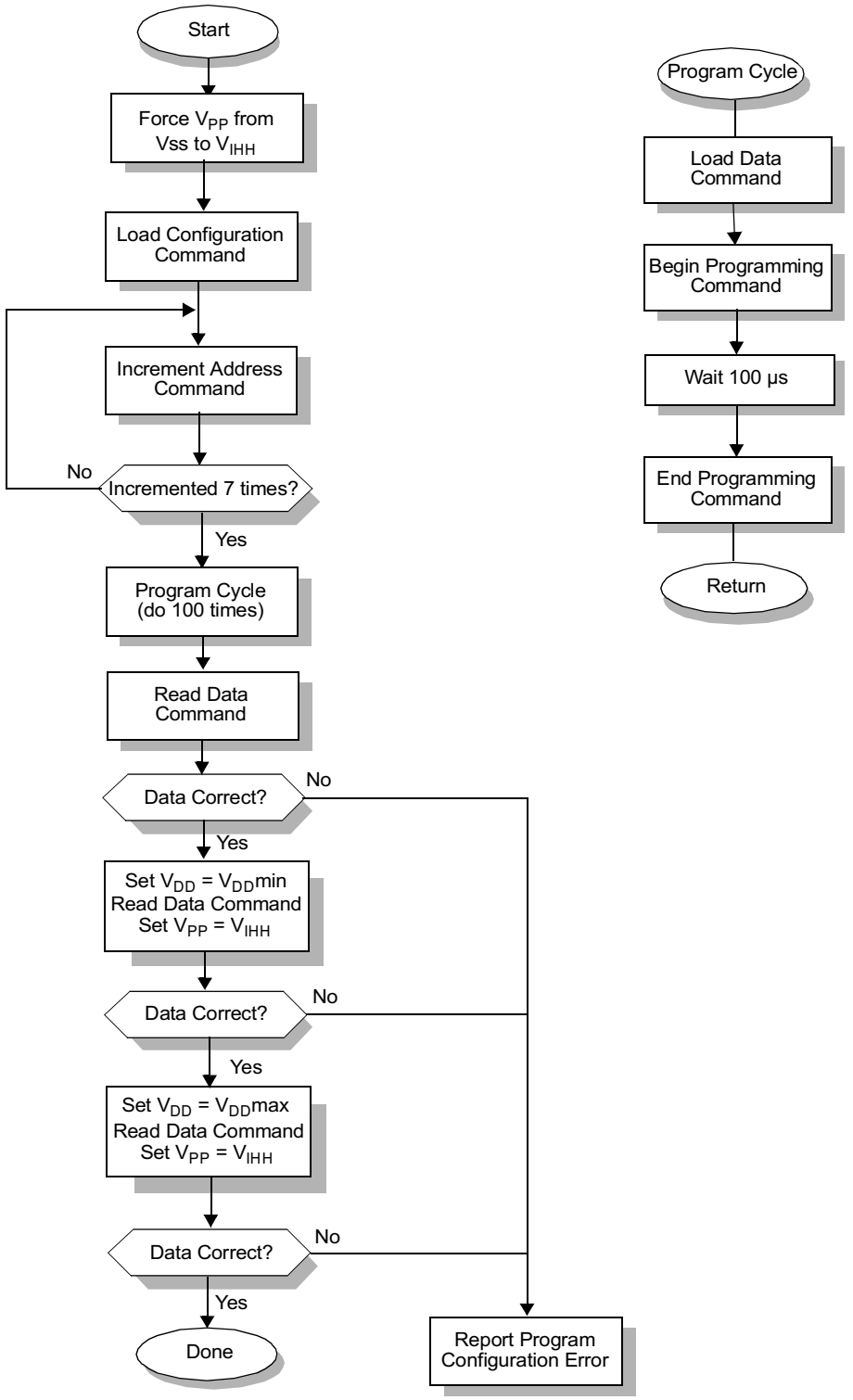
FIGURE 4-1: PROGRAM FLOW CHART - MCP250XX PROGRAM MEMORY



Note 1: $V_{DDP} = V_{DD}$ range for programming (typically 4.75V - 5.25V).

2: $V_{DD\ MIN.}$ = Minimum V_{DD} for device operation.
$V_{DD\ MAX.}$ = Maximum V_{DD} for device operation.

FIGURE 4-2: PROGRAM FLOW CHART - MCP250XX CONFIGURATION WORD



Note 1: V_{DDP} = V_{DD} range for programming (typically 4.75V - 5.25V).

2: $V_{DD\ MIN.}$ = Minimum V_{DD} for device operation.
$V_{DD\ MAX.}$ = Maximum V_{DD} for device operation.

5.0 CONFIGURATION WORD

The MCP250XX family members have several configuration bits. These bits can be programmed (reads '0') or left unprogrammed (reads '1') to select various device configurations. Register 5-1 provides an overview of configuration bits.

Only the lower 3-bits should be programmed. The remaining 11-bits are reserved and should be programmed as a '1'. Programming these bits as a '1' will ensure that the factory value is not modified.

REGISTER 5-1: CONFIGURATION REGISTER

R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R-x	R/P-1	R/P-1	R/P-1
—	—	—	—	—	—	—	—	—	—	—	RSTEN	FOSC1	FOSC0
bit 13													bit 0

bit 13-3 **Reserved:** Read as 'x', Program as '1'.

bit 2 **RSTEN:** Reset on GP7 Enable bit
1 = $\overline{\text{RST}}$ function is enabled on the GP7 I/O pin
0 = GP7 is a general purpose I/O pin

bit 1-0 **FOSC1:FOSC0:** Oscillator Selection bits
11 = HS oscillator
10 = Reserved
01 = XT oscillator
00 = LP oscillator

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'
- n = Value when device is unprogrammed		x = Unknown state

6.0 MEMORY VERIFICATION

The User EPROM memory and configuration word is checksummed. This enhances the validation that the correct user's values are programmed into the devices memory.

6.1 Checksum CALCULATIONS

Checksum is calculated by reading the contents of the MCP250XX User EPROM memory locations and adding the values up. The entire User EPROM memory is read (00h - 44h). Any carry bits exceeding 16-bits are ignored. Checksum computation for each member of the MCP250XX devices is shown in Table 6-1.

The checksum is calculated by summing the user memory and taking the 2s complement. The result is the truncated lower eight bits.

The Table 6-1 describes how to calculate the checksum.

TABLE 6-1: CHECKSUM COMPUTATION

Device	Checksum (1)	Value	
		Unprogrammed	When: Addr. 0x000 = 0xE6 Addr. 0x044 = 0xE6
MCP250XX	~ [SUM(0x000:0x045)] + 1	0x45	0x77
MCP2502x	~ [SUM(0x000:0x045)] + 1	0x2C	0x5E

Legend: SUM[a:b] = [Sum of locations a through b inclusive]

Note 1: Checksum = 2s comlement of the sum of all the individual expressions, trucated to 8-bits.
~ = 1s complement

7.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

7.1 DC Characteristics

FIGURE 7-1: PROGRAMMING DC CHARACTERISTICS WAVEFORMS

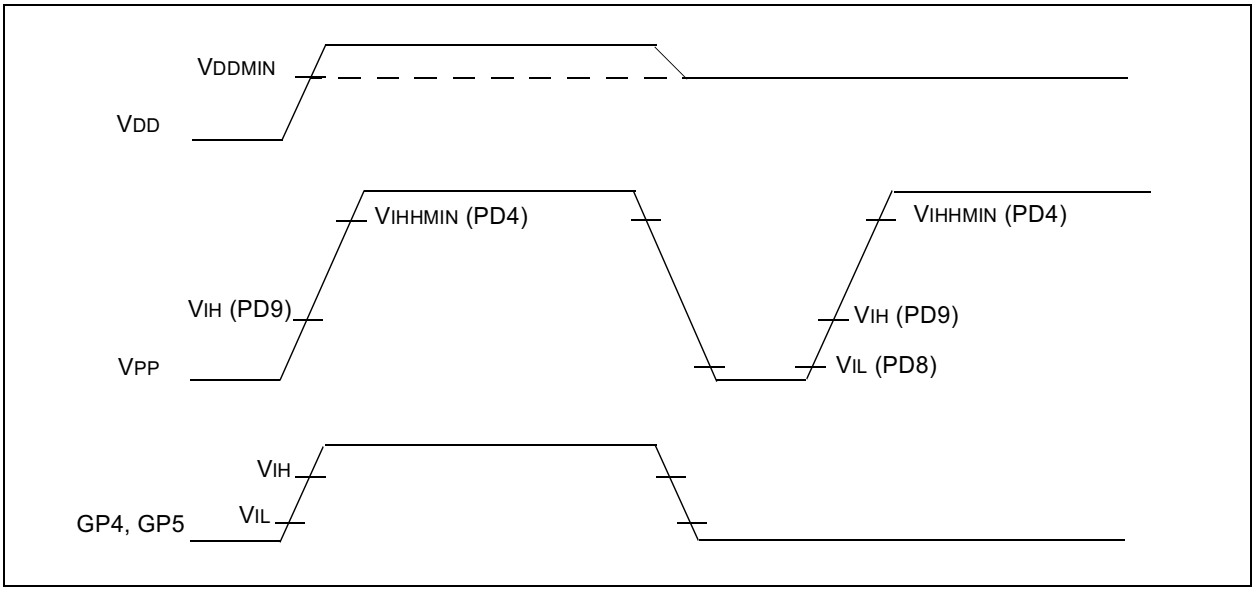


TABLE 7-1: DC CHARACTERISTICS FOR PROGRAMMING MODE (PROGRAM/VERIFY)

Standard Operating Conditions:
Operating Temperature: +10°C ≤ TA ≤ +40°C, unless otherwise stated, (25°C is recommended)
Operating Voltage: 4.5V ≤ VDD ≤ 5.5V, unless otherwise stated.

Parameter No.	Sym.	Characteristic		Min.	Typ.	Max.	Units	Conditions
PD1	VDDP	Supply voltage during programming		4.75	5.0	5.25	V	
PD2	IDDP	Supply current (from VDD) during programming		—	—	20	mA	
PD3	VDDV	Supply voltage during verify		VDDmin	—	VDDmax	V	**Note 1**
PD4	VIHH	Voltage on $\overline{MCLR}$/VPP during programming/verify		12.75	—	13.25	V	
PD6	IPP	Programming supply current (from VPP)		—	—	50	mA	
PD8	VIL	Voltage input low level	DATA (GP4)	VSS	—	0.2 VDD	V	Schmitt Trigger input
			CLOCK (GP5)	VSS	—	0.2 VDD	V	Schmitt Trigger input
			RESET	VSS	—	0.2 VDD	V	
PD9	VIH	Voltage input high level	DATA (GP4)	0.8 VDD	—	VDD	V	Schmitt Trigger input
			CLOCK (GP5)	0.8 VDD	—	VDD	V	Schmitt Trigger input
			RESET	0.8 VDD	—	VDD	V	

Note 1: Program must be verified at the minimum and maximum VDD limits of the device.

7.2 Timing (AC) Characteristics

FIGURE 7-2: PROGRAMMING MODE ENTRY WAVEFORM

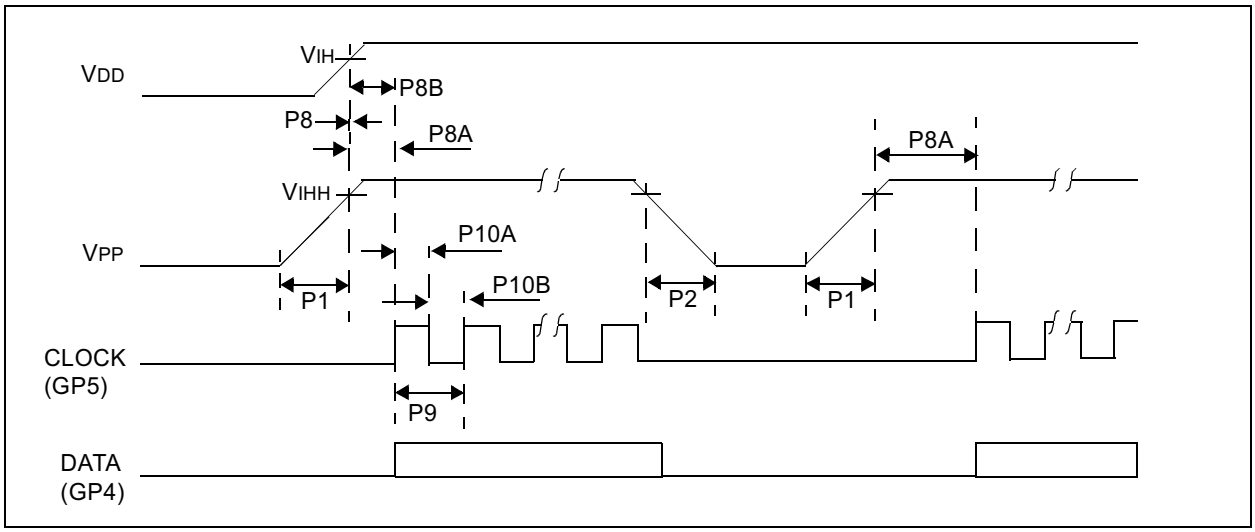


TABLE 7-2: PROGRAMMING MODE ENTRY TIMING

Parameter No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
P1	TR	RST/VPP rise time (VSS to VIHH)	0.15	—	1.0	µs	
P2	TF	$\overline{\text{RST}}$ Fall time	0.5	—	1.0	µs	
P8	THLD0	Hold time after VPP = VIHH to VDD valid	0	—	—	ns	
P8A	TPPDP	Hold time after VPP = VIHH to CLOCK ↑	2	—	—	µs	
P8B	THLD0	Hold time after VDD valid to CLOCK ↑	2	—	—	µs	
P9	TCLOCK	CLOCK pin Period (in Time)	250	—	—	ns	
P9A	FCLOCK	CLOCK pin Period (in Frequency)	—	—	4	MHz	
P10A	TCLKH	CLOCK pin High time	100	—	—	ns	
P10B	TCLKL	CLOCK pin Low time	100	—	—	ns	

Note 1: Program must be verified at the minimum and maximum VDD limits of the device.

FIGURE 7-3: LOAD CONFIGURATION COMMAND WAVEFORM

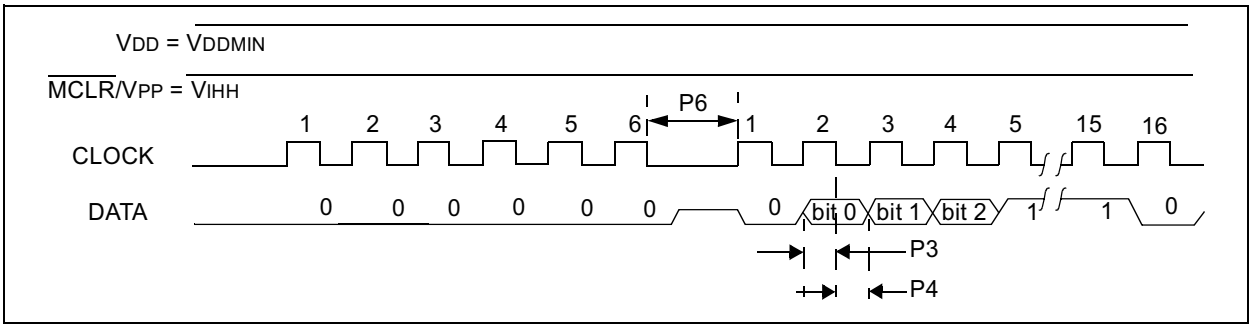


TABLE 7-3: LOAD CONFIGURATION COMMAND TIMING

Parameter No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
P3	TSET1	Data in setup time before clock ↓	100	—	—	ns	
P4	THLD1	Data in hold time after clock ↓	100	—	—	ns	
P6	TDLY2	Delay between clock ↓ to clock ↑ of next command or data	1.0	—	—	µs	

Note 1: Program must be verified at the minimum and maximum VDD limits of the device.

FIGURE 7-4: LOAD DATA COMMAND WAVEFORM

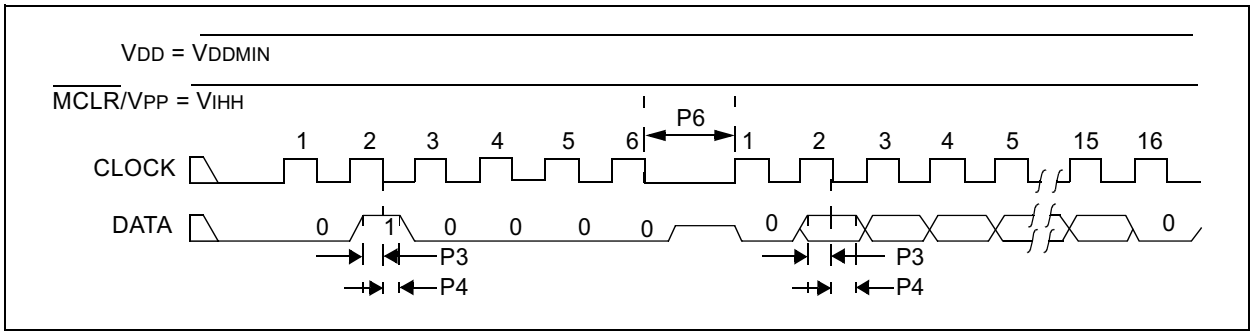


TABLE 7-4: LOAD DATA COMMAND TIMING

Parameter No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
P3	TSET1	Data in setup time before clock ↓	100	—	—	ns	
P4	THLD1	Data in hold time after clock ↓	100	—	—	ns	
P6	TDLY2	Delay between clock ↓ to clock ↑ of next command or data	1.0	—	—	µs	

Note 1: Program must be verified at the minimum and maximum VDD limits of the device.

FIGURE 7-5: READ DATA COMMAND WAVEFORM

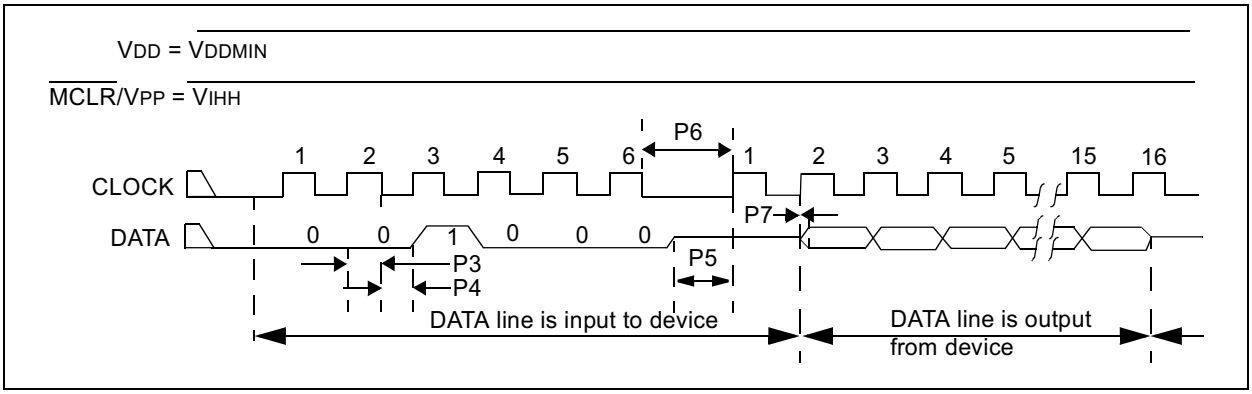


TABLE 7-5: READ DATA COMMAND TIMING

Parameter No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
P3	TSET1	Data in setup time before clock ↓	100	—	—	ns	
P4	THLD1	Data in hold time after clock ↓	100	—	—	ns	
P5	TDLY1	Data input not driven to next clock input (delay required between command/data or command/command)	0.9	—	—	µs	
P6	TDLY2	Delay between clock ↓ to clock ↑ of next command or data	1.0	—	—	µs	
P7	TDLY3	Clock ↑ to data out valid (during read data)	—	—	200	ns	

Note 1: Program must be verified at the minimum and maximum VDD limits of the device.

FIGURE 7-6: INCREMENT ADDRESS COMMAND WAVEFORM

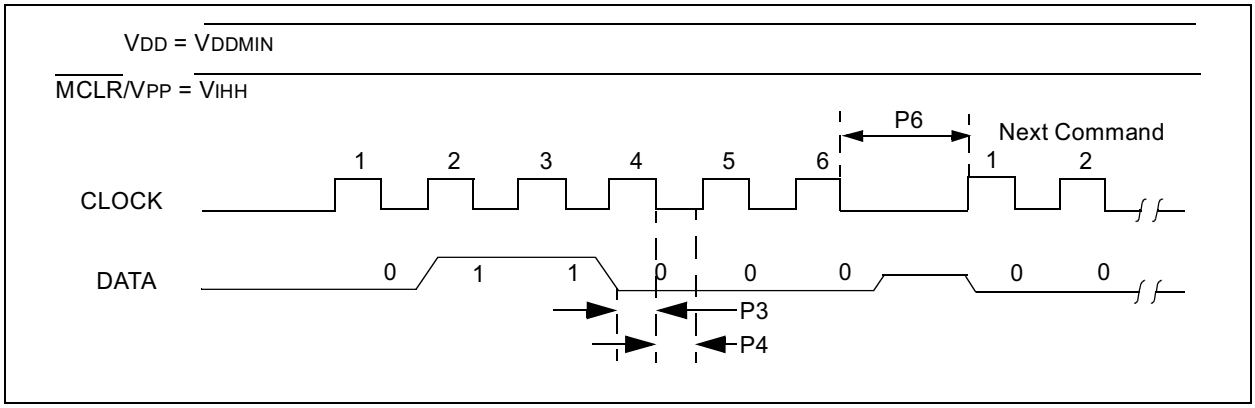


TABLE 7-6: INCREMENT ADDRESS TIMING

Parameter No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
P3	TSET1	Data in setup time before clock ↓	100	—	—	ns	
P4	THLD1	Data in hold time after clock ↓	100	—	—	ns	
P6	TDLY2	Delay between clock ↓ to clock ↑ of next command or data	1.0	—	—	µs	

Note 1: Program must be verified at the minimum and maximum VDD limits of the device.

FIGURE 7-7: BEGIN PROGRAMMING COMMAND WAVEFORM

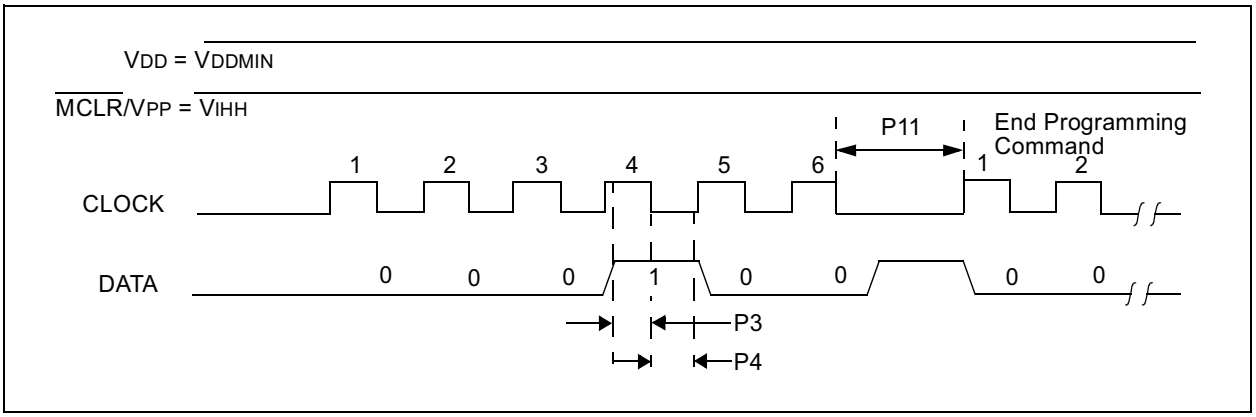


TABLE 7-7: BEGIN PROGRAMMING COMMAND TIMING

Parameter No.	Symbol	Characteristic		Min.	Typ.	Max.	Units	Conditions
P3	TSET1	Data in setup time before clock ↓		100	—	—	ns	
P4	THLD1	Data in hold time after clock ↓		100	—	—	ns	
P11		Programming Pulse Width	User Memory	90	100	110	µs	
			Configuration Memory	90	100	110	µs	

Note 1: Program must be verified at the minimum and maximum VDD limits of the device.

FIGURE 7-8: END PROGRAMMING COMMAND WAVEFORM

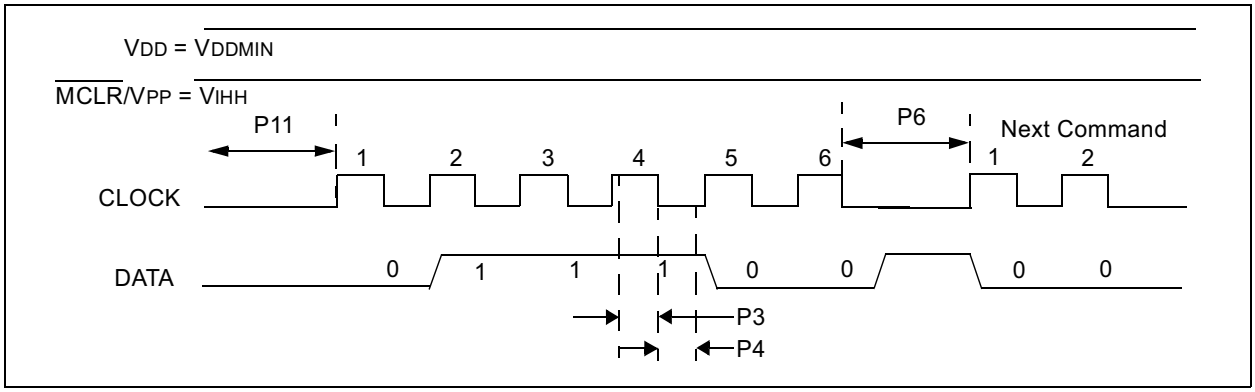


TABLE 7-8: END PROGRAMMING COMMAND TIMING

Parameter No.	Symbol	Characteristic		Min.	Typ.	Max.	Units	Conditions
P3	TSET1	Data in setup time before clock ↓		100	—	—	ns	
P4	THLD1	Data in hold time after clock ↓		100	—	—	ns	
P6	TDLY2	Delay between clock ↓ to clock ↑ of next command or data		1.0	—	—	µs	
P11		Programming Pulse Width (1)	User Memory	90	100	110	µs	
			Configuration Memory	90	100	110	µs	

Note 1: Only required if the previous command was the Begin Programming Command.
2: Program must be verified at the minimum and maximum VDD limits of the device.

NOTES:

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