MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

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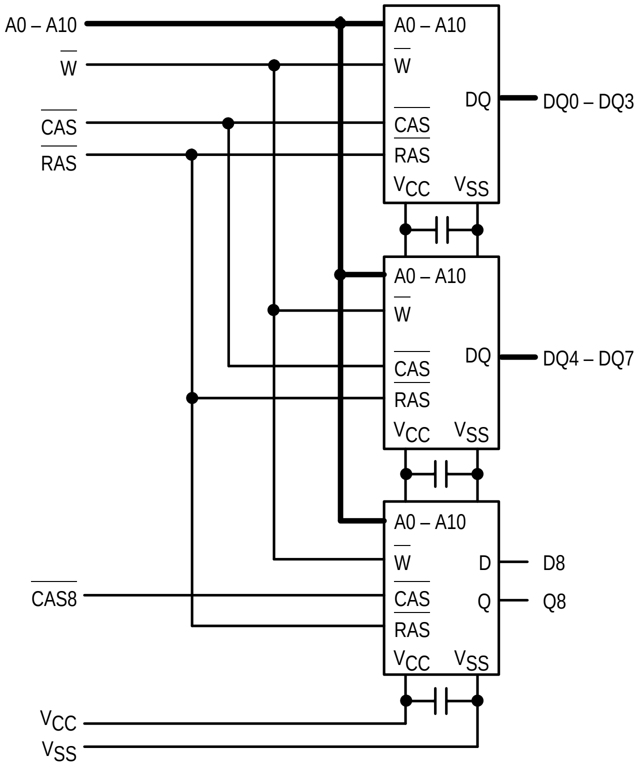
MCM94430

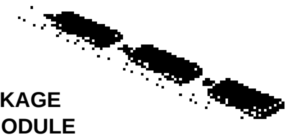
4M x 9 Bit Dynamic RAM Module

The MCM94430 is a 36M dynamic random access memory (DRAM) module organized as 4,194,304 x 9 bits. The module is a 30–lead single–in–line memory module (SIMM) consisting of two MCM517400B and one MCM54100A DRAMs housed in a J–lead small outline packages (SOJ) mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted adjacent to each DRAM. The MCM517400B is a CMOS high–speed dynamic random access memory organized as 4,194,304 four–bit words and fabricated with CMOS silicon–gate process technology.

- Three–State Data Output
- Early–Write Common I/O Capability
- Fast Page Mode Capability
- TTL–Compatible Inputs and Outputs
- RAS–Only Refresh
- CAS Before RAS Refresh
- Hidden Refresh
- 2048 Cycle Refresh: 32 ms
- Consists of Two 4M x 4, One 4Mx1 DRAMs, and Three 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM94430–60 = 60 ns (Max)
  MCM94430–70 = 70 ns (Max)
- Low Active Power Dissipation: MCM94430–60 = 1.87 W (Max)
  MCM94430–70 = 1.63 W (Max)
- Low Standby Power Dissipation: TTL Levels = 33 mW (Max)
  CMOS Levels = 28 mW (Max)
- CAS Control for Eight Common I/O Lines
- CAS Control for Separate I/O Pair

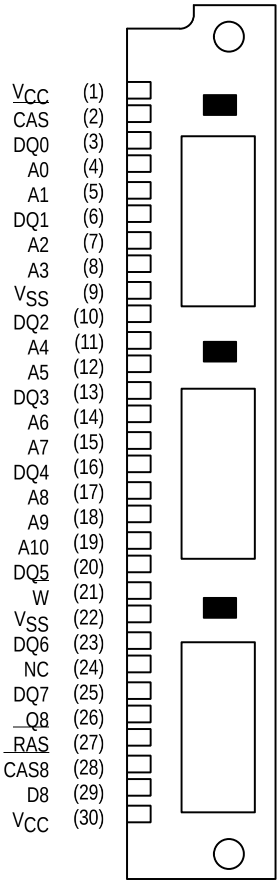
FUNCTIONAL BLOCK DIAGRAM





S PACKAGE
SIMM MODULE
CASE 839A–01

TOP VIEW



PIN NAMES

A0 – A10	Address Inputs
DQ0 – DQ7	Data Input/Output
D8	Data Input
Q8	Data Output
CAS	Column Address Strobe
RAS	Row Address Strobe
W	Read/Write Input
CAS8	Column Address Strobe
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

10/95

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to + 7	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	2.5	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	V_{CC} + 0.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 0.5*	—	0.8	V

* –2.0 V at pulse width ≤ 20 ns

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM94430–60, t_{RC} = 110 ns MCM94430–70, t_{RC} = 130 ns	I_{CC1}	— —	340 290	mA	1
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	6	mA	
V_{CC} Power Supply Current During $\overline{RAS}$ Only Refresh Cycles MCM94430–60, t_{RC} = 110 ns MCM94430–70, t_{RC} = 130 ns	I_{CC3}	 — —	 340 290	mA	1
V_{CC} Power Supply Current During Fast Page Mode Cycle	I_{CC4}	—	180	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	—	3	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM94430–60, t_{RC} = 110 ns MCM94430–70, t_{RC} = 130 ns	I_{CC6}	 — —	 340 290	mA	1
Input Leakage Current ($V_{SS} \leq V_{in} \leq V_{CC}$)	$I_{lkg(I)}$	– 30	30	µA	
Output Leakage Current ($\overline{CAS}$ at Logic 1, $V_{SS} \leq V_{in} \leq V_{CC}$)	$I_{lkg(O)}$	– 20	20	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Parameter		Symbol	Max	Unit
Input Capacitance	A0 – A10, $\overline{W}$, $\overline{CAS}$, $\overline{RAS}$ D8, CAS8	C_{in}	25 17	pF
Input/Output Capacitance	DQ0 – DQ7	$C_{I/O}$	17	pF
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	Q8	C_{out}	17	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\,\Delta t/\Delta V$.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM94430–60		MCM94430–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	45	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RELQV}	t_{RAC}	—	60	—	70	ns	6, 7
Access Time from $\overline{\text{CAS}}$	t_{CELQV}	t_{CAC}	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	ns	6, 9
Access Time from Precharge $\overline{\text{CAS}}$	t_{CEHQV}	t_{CPA}	—	40	—	40	ns	6
$\overline{\text{CAS}}$ to Output in Low–Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn–Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{REHREL}	t_{RP}	45	—	50	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	ns	
$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	200 k	70	200 k	ns	
$\overline{\text{RAS}}$ Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	ns	
$\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time	t_{CEHREH}	t_{RHCP}	40	—	40	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CELCEH}	t_{CAS}	20	10 k	20	10 k	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	ns	11
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	ns	12
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power–up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

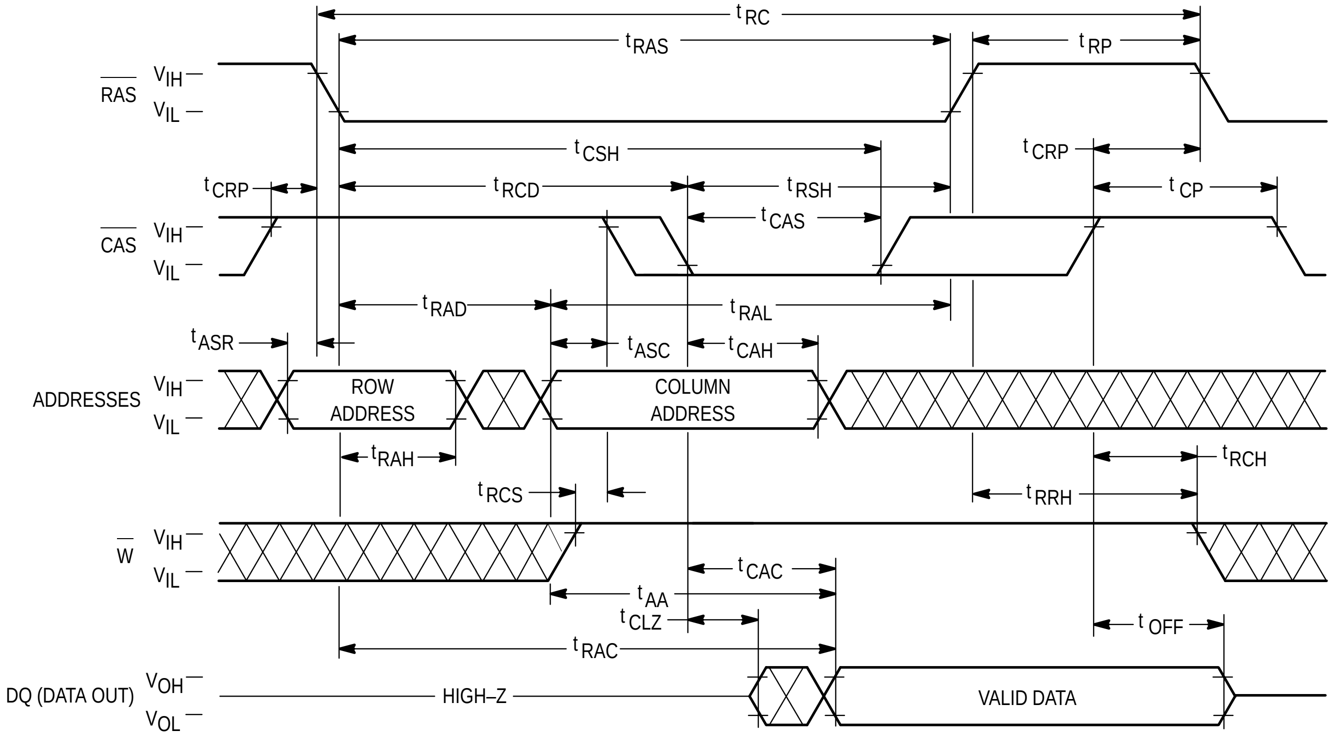
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM94430–60		MCM94430–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Read Command Hold Time Referenced to CAS	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to RAS	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to CAS	t_{CELWH}	t_{WCH}	10	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	ns	
Write Command to RAS Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	ns	
Write Command to CAS Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	ns	14
Refresh Period	t_{RVRV}	t_{RFSH}	—	16	—	16	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15
CAS Setup Time for CAS Before RAS Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	ns	
CAS Hold Time for CAS Before RAS Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	ns	
RAS Precharge to CAS Active Time	t_{REHCEL}	t_{RPC}	5	—	5	—	ns	
CAS Precharge Time for CAS Before RAS Counter Time	t_{CEHCEL}	t_{CPT}	30	—	40	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	ns	
Write to RAS Precharge Time (CAS Before RAS Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	ns	
Write to RAS Hold Time (CAS Before RAS Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	ns	

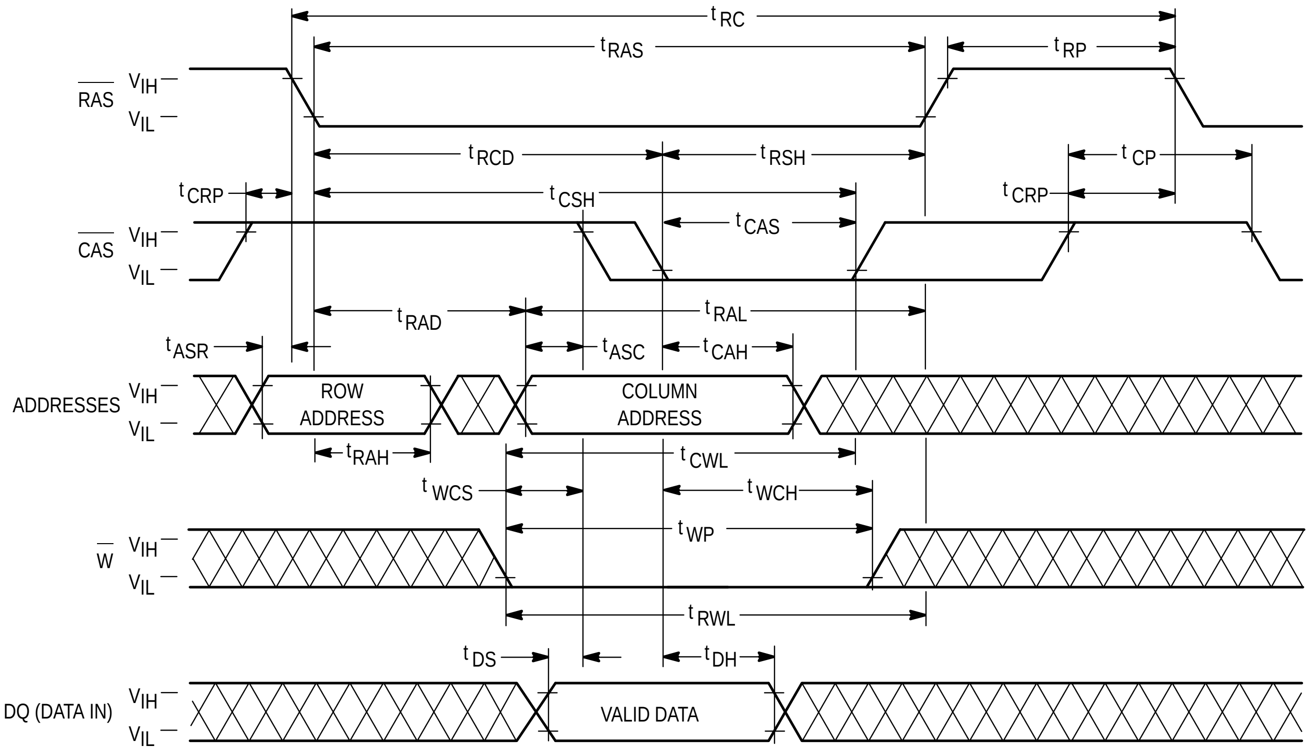
NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to CAS leading edge in early write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.

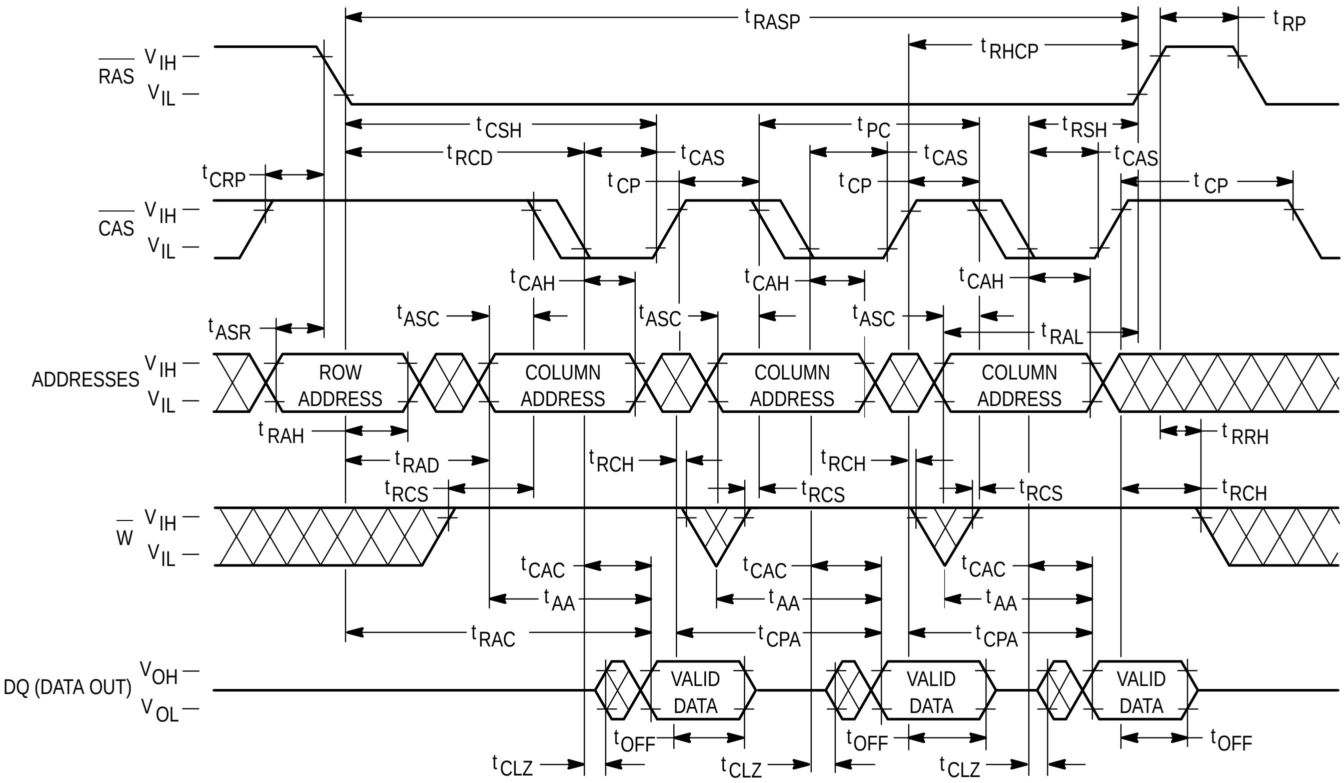
READ CYCLE



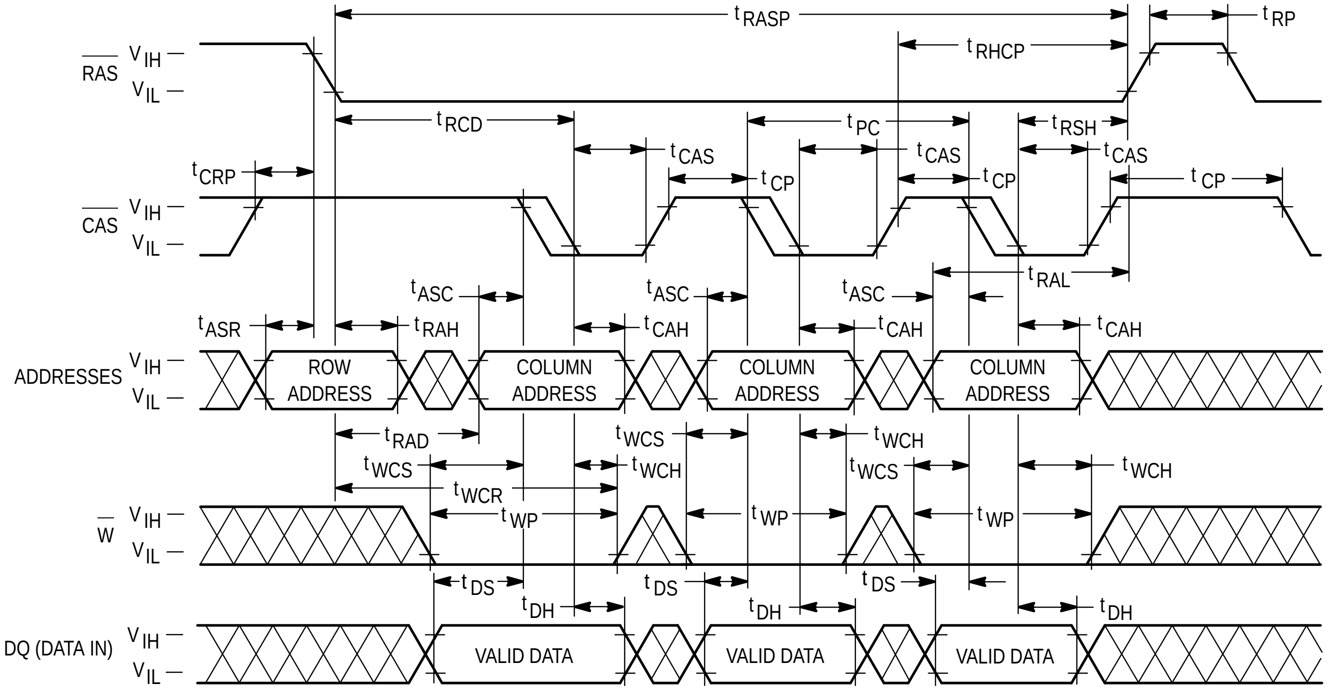
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE

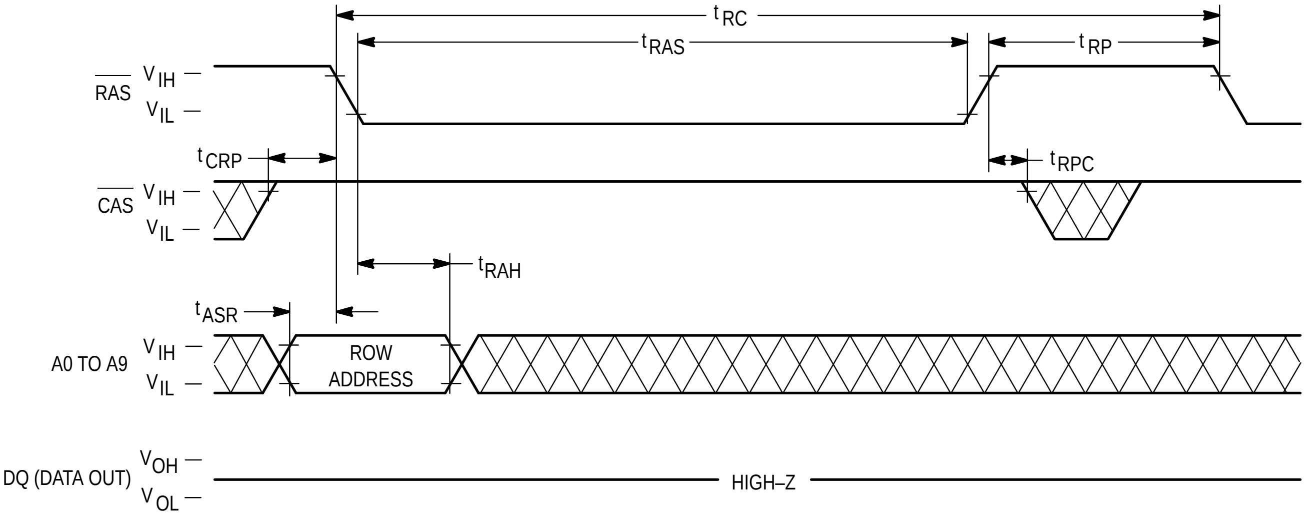


FAST PAGE MODE EARLY WRITE CYCLE



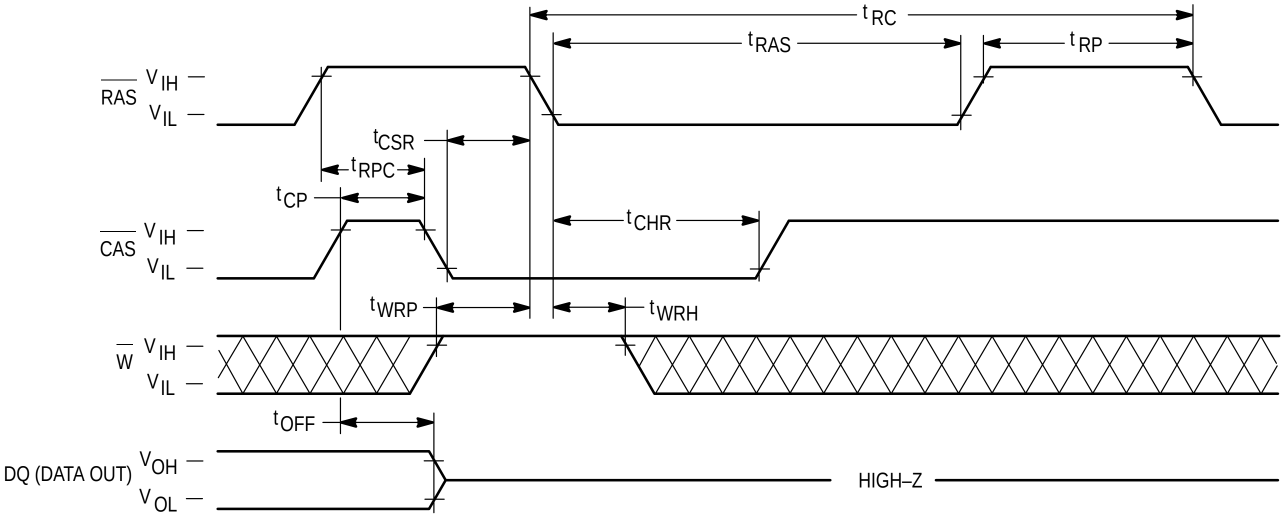
RAS ONLY REFRESH CYCLE

(W is Don't Care)

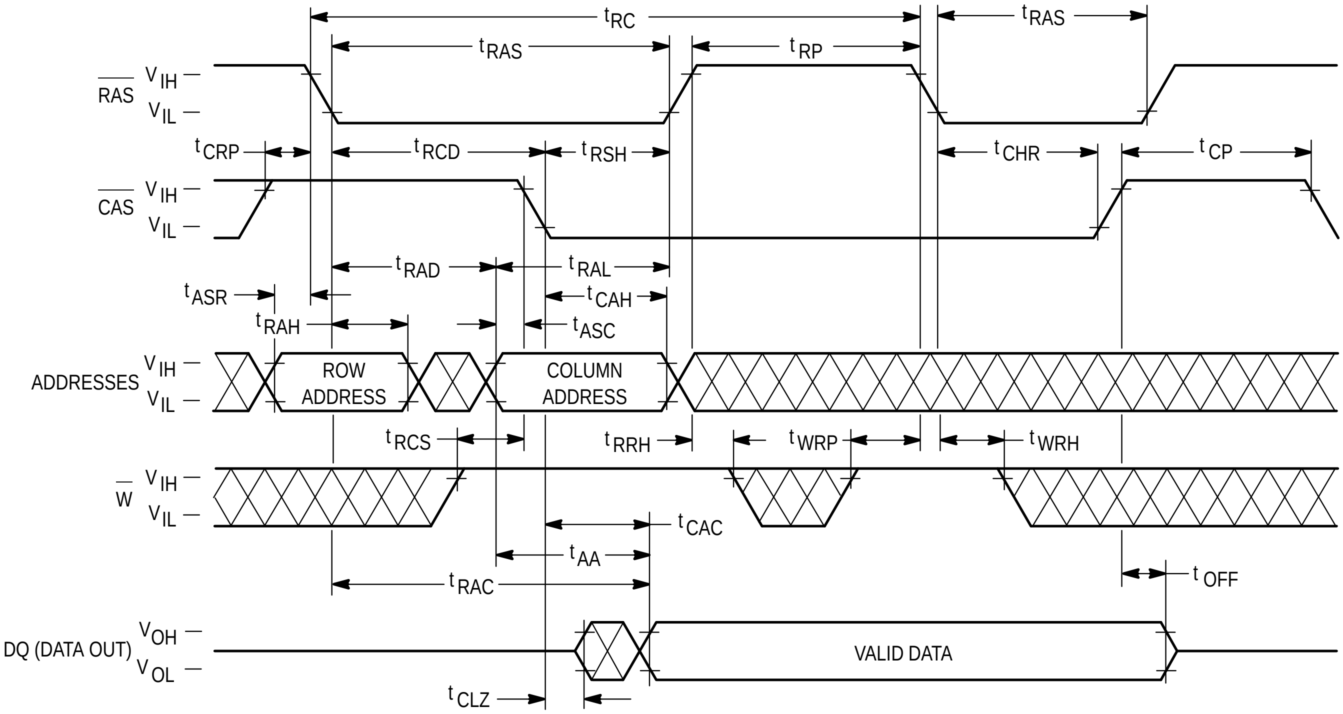


CAS BEFORE RAS REFRESH CYCLE

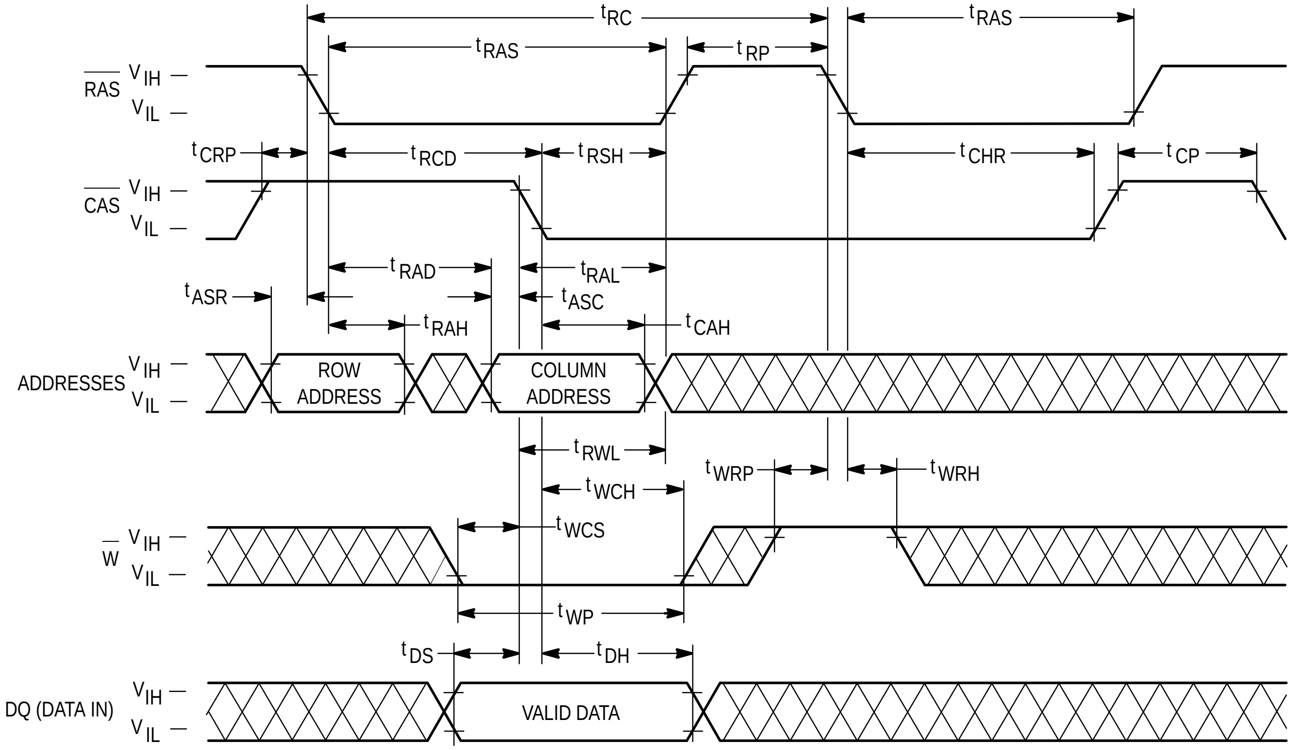
(A0 – A10 are Don't Care)



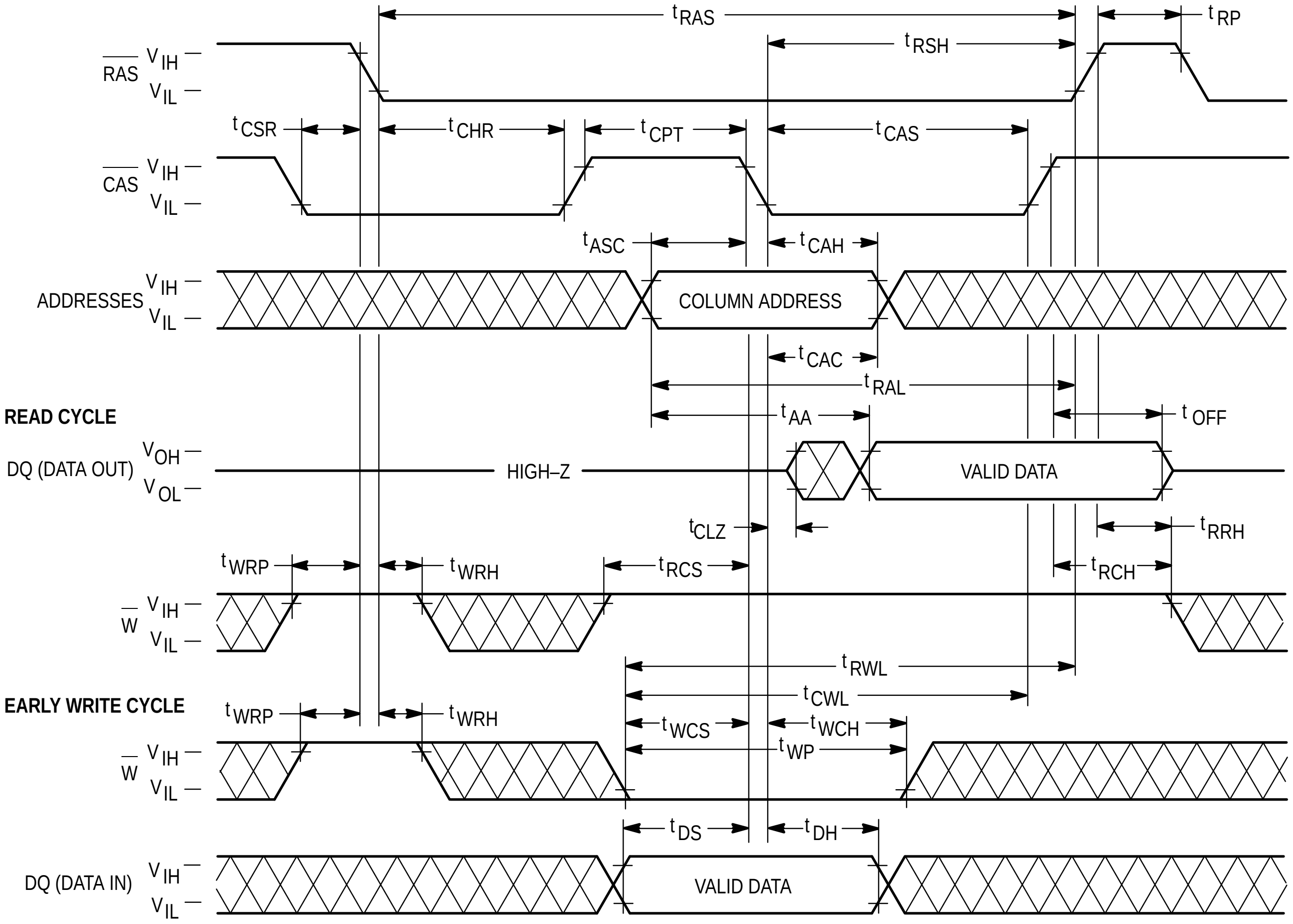
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power–up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe (RAS) and column address strobe (CAS), into two separate 11–bit address fields. A total of twenty–two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 word locations in the device. RAS active transition is followed by CAS active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between RAS and CAS active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external CAS signal is ignored until an internal RAS signal is available. This gate feature on the external CAS clock enables the internal CAS line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the CAS clock.

There are three other variations in addressing the module: **RAS only refresh cycle, CAS before RAS refresh cycle,** and **page mode**.

READ CYCLE

The DRAM may be read with either a normal random read cycle or a page mode read cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with RAS and CAS active transitions latching the desired bit location. The write (W) input level must be high (V_{IH}), t_{RCS} (minimum) before the CAS active transition, to enable read mode.

Both the RAS and CAS clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window; however, CAS must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from RAS active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the CAS clock active transition (t_{CAC}).

The RAS and CAS clocks must remain active for a minimum time of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. W must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after RAS or CAS inactive transition, respectively, to maintain the data at that bit location. Once RAS transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. DQ is valid, but not latched, as long as the CAS clock is active. When the CAS clock transitions to inactive, the output will switch to High–Z (three–state).

WRITE CYCLE

The user can write to the DRAM with either an early write or page mode early write cycle. Early write mode is discussed here, while page mode write operation is covered elsewhere.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of W to active (V_{IL}). Early write mode is distinguished by the active transition of W, with respect to CAS. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by W active transition at minimum time t_{WCS} before CAS active transition. Data in (DQ) is referenced to CAS in an early write cycle. RAS and CAS clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 2048 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular RAS clock access time, t_{RAC}. Page mode operation consists of keeping RAS active while toggling CAS between V_{IH} and V_{IL}. The row is latched by RAS active transition, while each CAS active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, CAS transitions to inactive for minimum of t_{CP}, while RAS remains low (V_{IL}). The second CAS active transition while RAS is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM94430 require refresh every 32 milliseconds.

This is accomplished by cycling through the 2048 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds. Burst refresh, a refresh of all rows consecutively, must be performed every 32 milliseconds.

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decoded. Three other methods of refresh, **RAS–only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS–Only Refresh

RAS–only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle.

The output buffer remains at the same state it was in during the previous cycle (hidden refresh). W must be inactive for time t_{WRP} before and time t_{WRH} after RAS active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode cycle) as in CAS before RAS refresh.

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This test is performed with a read–write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 2048 cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed after a minimum of **8 CAS before RAS** initialization cycles. Test procedure:

1. Write 0s into all memory cells (normal write mode).
2. Select a column address, and read 0 out of the cell by performing **CAS before RAS refresh counter test, read cycle.** Repeat this operation 2048 times.
3. Select a column address, and write 1 into the cell by performing **CAS before RAS refresh counter test, write cycle.** Repeat this operation 2048 times.
4. Read 1s (normal read mode), which were written at step three.
5. Repeat steps one through four using complement data.

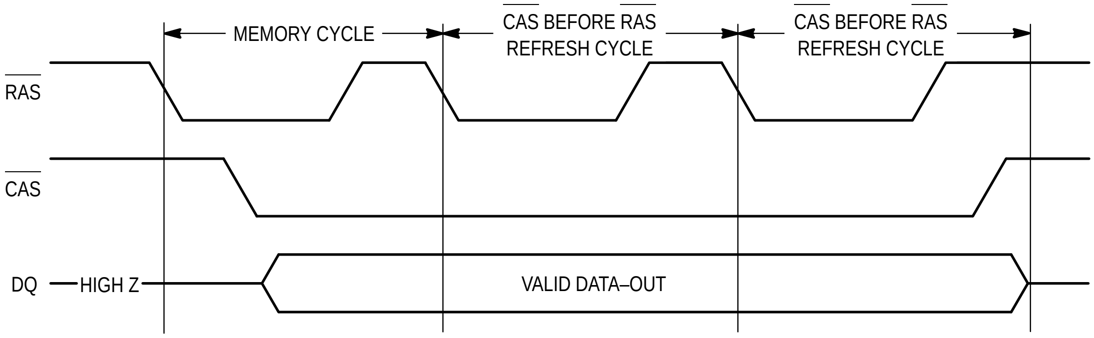


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION

(Order by Full Part Number)

MCM 94430 X XX

Motorola Memory Prefix — MCM

Part Number — 94430

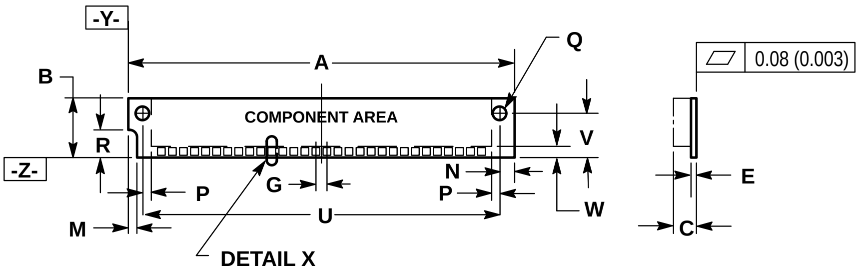
Package (S = SIMM, SG = Gold SIMM) — X

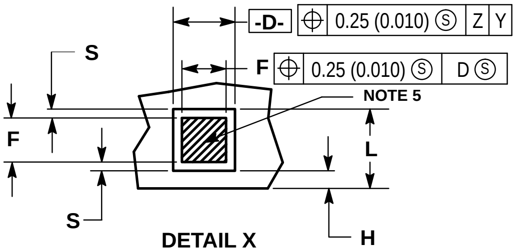
Speed (60 = 60 ns, 70 = 70 ns) — XX

Full Part Numbers — MCM94430S60 MCM94430SG60
MCM94430S70 MCM94430SG70

PACKAGE DIMENSIONS

S, SG PACKAGE
SIMM MODULE
CASE 839A–01





DETAIL X
60 PL

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TABS TO BE ELECTRICALLY CONNECTED BOTH SIDES OF CARD.
4. DIMENSION E INCLUDES PLATING AND/OR METALIZATION.
5. CONTACT ZONE MUST BE FREE OF HOLES.

	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	3.495	3.505	88.78	89.02
B	0.545	0.555	13.85	14.09
C	—	0.208	—	5.28
D	0.065	0.075	1.66	1.90
E	0.047	0.053	1.20	1.34
F	0.045	0.055	1.15	1.39
G	0.100 BSC		2.54 BSC	
H	—	0.010	—	0.25
L	0.080	—	2.04	—
M	0.075	0.085	1.91	2.15
N	0.128	0.138	3.26	3.50
P	0.045	—	1.15	—
Q	0.123	0.127	3.13	3.22
R	0.245	0.255	6.23	6.47
S	0.005	0.015	0.13	0.38
U	3.229	3.239	82.02	82.27
V	0.395	0.405	10.04	10.28
W	0.100	—	2.54	—

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