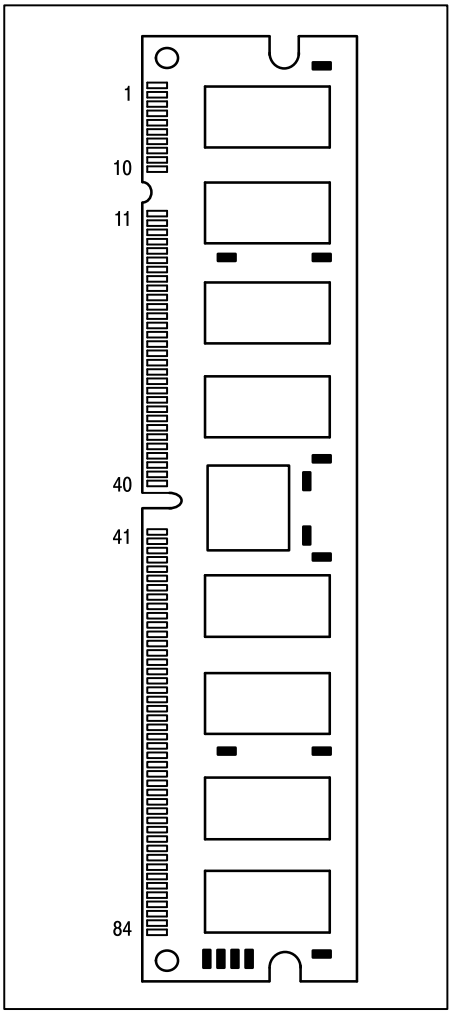
# MCM64100

*Product Preview*

# 1M x 64 Bit Dynamic Random Access Memory Module




The MCM64100 is a dynamic random access memory (DRAM) module organized as 1,048,576 x 64 bits. The module is a JEDEC-standard 168-lead dual-in-line memory module (DIMM) with 84 separate contacts per side, consisting of sixteen MCM54400A DRAMs housed in 300-mil thin small outline packages (TSOP), mounted on a substrate along with a 0.22 μF (min) decoupling capacitor mounted adjacent to each DRAM. Buffering is provided for address and all clock pins except $\overline{RAS}$. The MCM54400A is a CMOS high speed dynamic random access memory organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 2048 Cycle Refresh: 16 ms (Max)
- Consists of Sixteen 1M x 4 DRAMs, Sixteen 0.22 μF (Min) Decoupling Capacitors, and Two 20-Bit Buffers
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Presence Detect Enable ($\overline{PDE}$) Controls Access to 8 Bits of Buffered PD Information
- Notch Keys Prevent Accidental Insertion in Low Voltage (3.3 V) Systems
- Fast Access Time ($t_{RAC}$): MCM64100-60 = 60 ns (Max)
  MCM64100-70 = 70 ns (Max)
- Low Active Power Dissipation: MCM64100-60 = 10.89 W (Max)
  MCM64100-70 = 9.13 W (Max)
- Low Standby Power Dissipation: TTL Levels = 193 mW (Max)
  CMOS Levels = 105 mW (Max)

| PIN NAMES | |
|---|---|
| A0, B0, A1 – A9 . . . . . Address Inputs | DQ0 – DQ70* . . . . . Data Input/Output |
| $\overline{CAS0}$ – $\overline{CAS7}$ . . Column Address Strobe | $\overline{RAS0}$, $\overline{RAS2}$ . . . . . Row Address Strobe |
| $\overline{WE0}$, $\overline{WE2}$ . . . . . Write Enable | $\overline{OE0}$, $\overline{OE2}$ . . . . . Output Enable |
| PD1 – PD8 . . . Buffered Presence Detect | ID0, ID1 . . . . . Unbuffered ID Bit |
| $\overline{PDE}$ . . . . Presence Detect Output Enable | $V_{CC}$ . . . . . Power (+ 5 V) |
| $V_{SS}$ . . . . . Ground | NC . . . . . No Connection |

*DQ8, DQ17, DQ26, DQ35, DQ44, DQ53, and DQ62 are not present on 64 bit modules.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.





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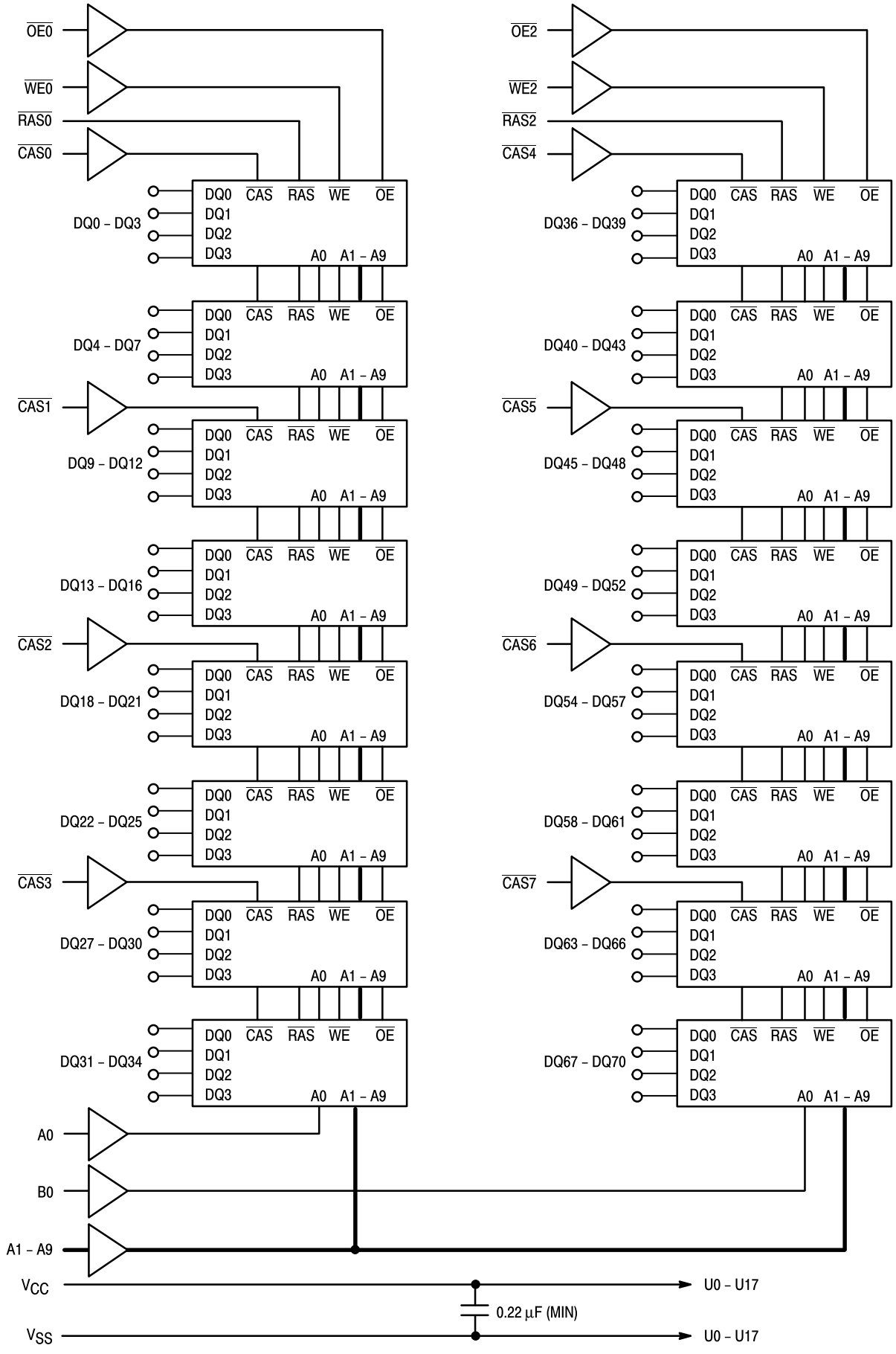
## BLOCK DIAGRAM



**1M x 64 168 DIMM Pinout**

| Front Side | | | | | | | | Back Side | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
| 1 | $V_{SS}$ | 22 | NC | 43 | $V_{SS}$ | 64 | NC | 85 | $V_{SS}$ | 106 | NC | 127 | $V_{SS}$ | 148 | NC |
| 2 | DQ0 | 23 | $V_{SS}$ | 44 | $\overline{OE2}$ | 65 | DQ25 | 86 | DQ36 | 107 | $V_{SS}$ | 128 | NC | 149 | DQ61 |
| 3 | DQ1 | 24 | NC | 45 | $\overline{RAS2}$ | 66 | NC | 87 | DQ37 | 108 | NC | 129 | NC | 150 | NC |
| 4 | DQ2 | 25 | NC | 46 | $\overline{CAS4}$ | 67 | DQ27 | 88 | DQ38 | 109 | NC | 130 | $\overline{CAS5}$ | 151 | DQ63 |
| 5 | DQ3 | 26 | $V_{CC}$ | 47 | $\overline{CAS6}$ | 68 | $V_{SS}$ | 89 | DQ39 | 110 | $V_{CC}$ | 131 | $\overline{CAS7}$ | 152 | $V_{SS}$ |
| 6 | $V_{CC}$ | 27 | $\overline{WE0}$ | 48 | $\overline{WE2}$ | 69 | DQ28 | 90 | $V_{CC}$ | 111 | NC | 132 | $\overline{PDE}$ | 153 | DQ64 |
| 7 | DQ4 | 28 | $\overline{CAS0}$ | 49 | $V_{CC}$ | 70 | DQ29 | 91 | DQ40 | 112 | $\overline{CAS1}$ | 133 | $V_{CC}$ | 154 | DQ65 |
| 8 | DQ5 | 29 | $\overline{CAS2}$ | 50 | NC | 71 | DQ30 | 92 | DQ41 | 113 | $\overline{CAS3}$ | 134 | NC | 155 | DQ66 |
| 9 | DQ6 | 30 | $\overline{RAS0}$ | 51 | NC | 72 | DQ31 | 93 | DQ42 | 114 | NC | 135 | NC | 156 | DQ67 |
| 10 | DQ7 | 31 | $\overline{OE0}$ | 52 | DQ18 | 73 | $V_{CC}$ | 94 | DQ43 | 115 | NC | 136 | DQ54 | 157 | $V_{CC}$ |
| 11 | NC | 32 | $V_{SS}$ | 53 | DQ19 | 74 | DQ32 | 95 | NC | 116 | $V_{SS}$ | 137 | DQ55 | 158 | DQ68 |
| 12 | $V_{SS}$ | 33 | A0 | 54 | $V_{SS}$ | 75 | DQ33 | 96 | $V_{SS}$ | 117 | A1 | 138 | $V_{SS}$ | 159 | DQ69 |
| 13 | DQ9 | 34 | A2 | 55 | DQ20 | 76 | DQ34 | 97 | DQ45 | 118 | A3 | 139 | DQ56 | 160 | DQ70 |
| 14 | DQ10 | 35 | A4 | 56 | DQ21 | 77 | NC | 98 | DQ46 | 119 | A5 | 140 | DQ57 | 161 | NC |
| 15 | DQ11 | 36 | A6 | 57 | DQ22 | 78 | $V_{SS}$ | 99 | DQ47 | 120 | A7 | 141 | DQ58 | 162 | $V_{SS}$ |
| 16 | DQ12 | 37 | A8 | 58 | DQ23 | 79 | PD1 | 100 | DQ48 | 121 | A9 | 142 | DQ59 | 163 | PD2 |
| 17 | DQ13 | 38 | NC | 59 | $V_{CC}$ | 80 | PD3 | 101 | DQ49 | 122 | NC | 143 | $V_{CC}$ | 164 | PD4 |
| 18 | $V_{CC}$ | 39 | NC | 60 | DQ24 | 81 | PD5 | 102 | $V_{CC}$ | 123 | NC | 144 | DQ60 | 165 | PD6 |
| 19 | DQ14 | 40 | $V_{CC}$ | 61 | NC | 82 | PD7 | 103 | DQ50 | 124 | $V_{CC}$ | 145 | NC | 166 | PD8 |
| 20 | DQ15 | 41 | NC | 62 | NC | 83 | ID0 | 104 | DQ51 | 125 | NC | 146 | NC | 167 | ID1 |
| 21 | DQ16 | 42 | NC | 63 | NC | 84 | $V_{CC}$ | 105 | DQ52 | 126 | B0 | 147 | NC | 168 | $V_{CC}$ |

NOTE: Contact your Motorola representative for additional information on the availability of other configurations and densities of modules in the new 168 pin DIMM family.

**Presence Detect/ID Bit Populations**

| Pin Name | 60 ns | 70 ns |
|---|---|---|
| PD1 | $V_{SS}$ | $V_{SS}$ |
| PD2 | $V_{SS}$ | $V_{SS}$ |
| PD3 | NC | NC |
| PD4 | $V_{SS}$ | $V_{SS}$ |
| PD5 | $V_{SS}$ | $V_{SS}$ |
| PD6 | NC | $V_{SS}$ |
| PD7 | NC | NC |
| PD8 | NC | NC |
| ID0 | $V_{SS}$ | $V_{SS}$ |
| ID1 | $V_{SS}$ | $V_{SS}$ |

NOTE: PDs and IDs must each be pulled up through a resistor to $V_{CC}$ at the next higher level of assembly. PDs are buffered and gated to the edge connector by the $\overline{PDE}$ (Presence Detect Enable) signal.

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