MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

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by MCM54800A/D

MCM54800A
MCM5L4800A
MCM5V4800A

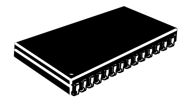
512K x 8 CMOS Dynamic RAM

Page Mode

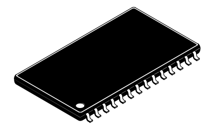
The MCM54800A is a 0.7µ CMOS high–speed, dynamic random access memory. It is organized as 524,288 eight–bit words and fabricated with CMOS silicon–gate process technology. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM54800A requires only 10 address lines; row and column address inputs are multiplexed. The device is packaged in a standard 400 mil J–lead small outline package and a 400 mil thin small outline package (TSOP).

- Three–State Data Output
- Fast Page Mode
- TTL–Compatible Inputs and Outputs
- RAS–Only Refresh
- CAS Before RAS Refresh
- Hidden Refresh
- Self Refresh (MCM5V4800A only)
- 1024 Cycle Refresh:
  MCM54800A = 16 ms
  MCM5L4800A and MCM5V4800A = 128 ms
- Fast Access Time (t_{RAC}):
  MCM54800A–70, MCM5L4800A–70, and MCM5V4800A–70 = 70 ns (Max)
  MCM54800A–80, MCM5L4800A–80, and MCM5V4800A–80 = 80 ns (Max)
  MCM54800A–10, MCM5L4800A–10, and MCM5V4800A–10 = 100 ns (Max)
- Low Active Power Dissipation:
  MCM54800A–70, MCM5L4800A–70, and MCM5V4800A–70 = 578 mW (Max)
  MCM54800A–80, MCM5L4800A–80, and MCM5V4800A–80 = 495 mW (Max)
  MCM54800A–10, MCM5L4800A–10, and MCM5V4800A–10 = 440 mW (Max)
- Low Standby Power Dissipation:
  MCM54800A, MCM5L4800A, and MCM5V4800A = 11 mW (Max, TTL Levels)
  MCM54800A = 5.5 mW (Max, CMOS Levels)
  MCM54L800A and MCM5V4800A = 1.1 mW (Max, CMOS Levels)
- Battery Backup Power Dissipation:
  MCM5L4800A = 1.7 mW (Max, Battery Backup Mode, t_{RC} = 125 µs)
- Self Refresh Power Dissipation:
  MCM5V4800A = 1.1 mW (Max, Self Refresh Mode)



J PACKAGE
400 MIL SOJ
CASE 810–03



T PACKAGE
400 MIL TSOP
CASE 899–01

PIN ASSIGNMENT

V_{CC}	1	28	V_{SS}
DQ0	2	27	DQ7
DQ1	3	26	DQ6
DQ2	4	25	DQ5
DQ3	5	24	DQ4
NC	6	23	CAS
W	7	22	G
RAS	8	21	NC
A9R	9	20	A8
A0	10	19	A7
A1	11	18	A6
A2	12	17	A5
A3	13	16	A4
V_{CC}	14	15	V_{SS}

PIN NAMES

A0 – A8, A9R	Address Input
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Write Input
G	Output Enable
DQ0 – DQ7	Data Input/Output
V_{CC}	Power Supply (+ 5 V)
V_{SS}	Ground
NC	No Connect

Motorola is announcing the end–of–life status of the 512Kx8 CMOS (MCM54800A) Dynamic RAM product family. Motorola will accept orders until April 3, 1996, and will support deliveries until October 3, 1996. There are no Motorola offerings that will directly replace these devices.

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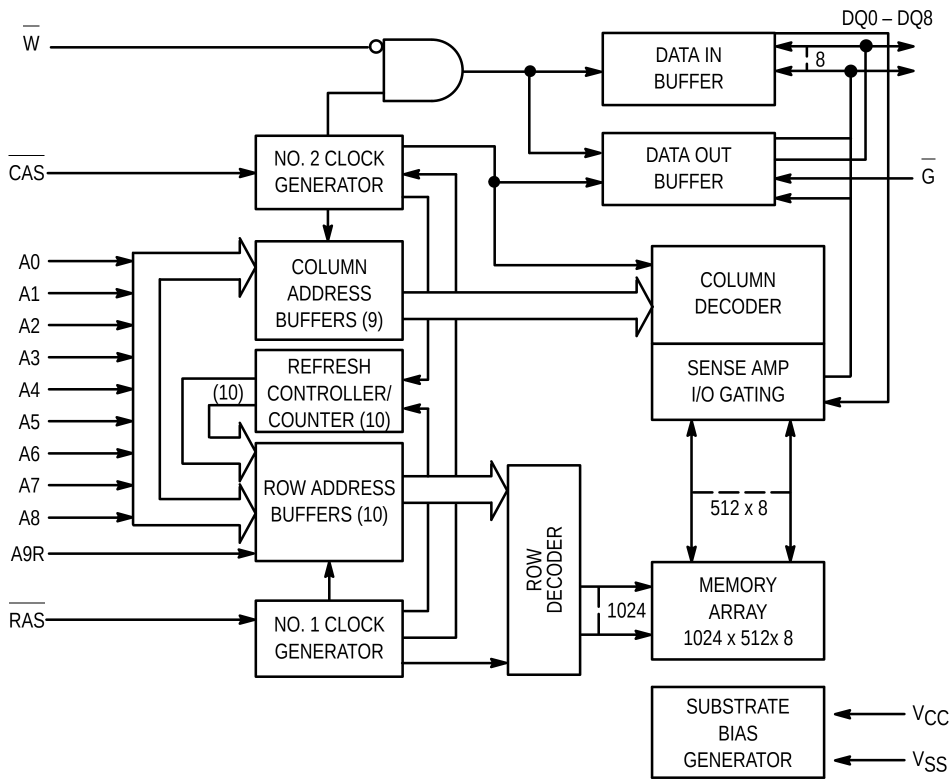
MOTOROLA

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Out Current	I_{out}	50	mA
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs Except DQ0 – DQ7	V_{IL}	– 1.0*	—	0.8	V
Logic Low Voltage, DQ0 – DQ7	V_{IL}	– 0.5**	—	0.8	V

*– 2.5 V at pulse width ≤ 20 ns
**– 2.0 V at pulse width ≤ 20 ns

DC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM54800A–70, MCM5L4800A–70, and MCM5V4800A–70, t_{RC} = 130 ns MCM54800A–80, MCM5L4800A–80, and MCM5V4800A–80, t_{RC} = 150 ns MCM54800A–10, MCM5L4800A–10, and MCM5V4800A–10, t_{RC} = 180 ns	I_{CC1}	 — — —	 105 90 80	mA	1, 2
V_{CC} Power Supply Current (Standby) (RAS = CAS = V_{IH})	I_{CC2}	—	2	mA	
V_{CC} Power Supply Current During RAS Only Refresh Cycles (CAS = V_{IH}) MCM54800A–70, MCM5L4800A–70, and MCM5V4800A–70, t_{RC} = 130 ns MCM54800A–80, MCM5L4800A–80, and MCM5V4800A–80, t_{RC} = 150 ns MCM54800A–10, MCM5L4800A–10, and MCM5V4800A–10, t_{RC} = 180 ns	I_{CC3}	 — — —	 105 90 80	mA	1, 2
V_{CC} Power Supply Current During Fast Page Mode Cycle (RAS = V_{IL}) MCM54800A–70, MCM5L4800A–70, and MCM5V4800A–70, t_{PC} = 45 ns MCM54800A–80, MCM5L4800A–80, and MCM5V4800A–80, t_{PC} = 50 ns MCM54800A–10, MCM5L4800A–10, and MCM5V4800A–10, t_{PC} = 60 ns	I_{CC4}	 — — —	 75 65 60	mA	1, 2
V_{CC} Power Supply Current (Standby) (RAS = CAS = V_{CC} – 0.2 V) MCM54800A MCM5L4800A and MCM5V4800A	I_{CC5}	— —	1.0 200	mA µA	
V_{CC} Power Supply Current During CAS Before RAS Refresh Cycle MCM54800A–70, MCM5L4800A–70, and MCM5V4800A–70, t_{RC} = 130 ns MCM54800A–80, MCM5L4800A–80, and MCM5V4800A–80, t_{RC} = 150 ns MCM54800A–10, MCM5L4800A–10, and MCM5V4800A–10, t_{RC} = 180 ns	I_{CC6}	 — — —	 105 90 80	mA	1
V_{CC} Power Supply Current, Battery Backup Mode—MCM5L4800A Only (t_{RC} = 125 µs; t_{RAS} = 1 µs; CAS = CAS Before RAS Cycle or 0.2 V; A0 – A8, A9R, W, D = V_{CC} – 0.2 V or 0.2 V)	I_{CC7}	—	300	µA	1, 3
V_{CC} Power Supply Current, Self Refresh Mode — MCM5V4800A Only (RAS = CAS = V_{IL}; A0 – A8, A9R, W, G = V_{CC} – 0.2 V or 0.2 V; DQ0–DQ7 = V_{CC} – 0.2 V, 0.2 V, or Open)	I_{CC8}	—	200	µA	
Input Leakage Current (0 V ≤ V_{in} ≤ 7.0 V)	$I_{lkg(I)}$	– 10	10	µA	
Output Leakage Current (0 V ≤ V_{out} ≤ 7.0 V, Output Disable)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:
1. Current is a function of cycle rate and output loading. Maximum currents are at the specified cycle time (min) with the output open.
2. Column address can be changed once or less while RAS = V_{IL} and CAS = V_{IH}.
3. t_{RAS} (max) = 1 µs is only applied to refresh of battery back–up. t_{RAS} (max) = 10 µs is applied to functional operating.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, periodically sampled, not 100% tested)

Parameter		Symbol	Max	Unit
Input Capacitance	A0 – A8, A9R	C_{in}	5	pF
	RAS, CAS, W, G		7	
Input/Output Capacitance (CAS = V_{IH} to Disable Output)	DQ0 – DQ7	C_{out}	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ–MODIFY–WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM54800A–70 MCM5L4800A–70 MCM5V4800A–70		MCM54800A–80 MCM5L4800A–80 MCM5V4800A–80		MCM54800A–10 MCM5L4800A–10 MCM5V4800A–10		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	130	—	150	—	180	—	ns	5
Read–Modify–Write Cycle Time	t_{RELREL}	t_{RWC}	185	—	205	—	245	—	ns	5
Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	50	—	60	—	ns	
Page Mode Read–Modify–Write Cycle Time	t_{CELCEL}	t_{PRWC}	100	—	105	—	125	—	ns	
Access Time from RAS	t_{RELQV}	t_{RAC}	—	70	—	80	—	100	ns	6, 8, 9
Access Time from CAS	t_{CELQV}	t_{CAC}	—	20	—	20	—	25	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	35	—	40	—	50	ns	6, 9
Access Time from CAS Precharge	t_{CEHQV}	t_{CPA}	—	40	—	45	—	55	ns	6
CAS to Output in Low–Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer Turn–Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	7
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
RAS Precharge Time	t_{REHREL}	t_{RP}	50	—	60	—	70	—	ns	
RAS Pulse Width	t_{RELREH}	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
RAS Pulse Width (Page Mode)	t_{RELREH}	t_{RASP}	70	100,000	80	100,000	100	100,000	ns	
RAS Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	25	—	ns	
CAS Hold Time	t_{RELCEH}	t_{CSH}	70	—	80	—	100	—	ns	
CAS Pulse Width	t_{CELCEH}	t_{CAS}	20	10,000	20	10,000	25	10,000	ns	
RAS to CAS Delay Time	t_{RELCEL}	t_{RCD}	20	50	20	60	25	75	ns	8
RAS to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	35	15	40	20	50	ns	9
CAS to RAS Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	10	—	ns	
CAS Precharge Time (Page Mode Only)	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
RAS Hold Time From CAS Precharge (Page Mode Only)	t_{CEHREH}	t_{RHCP}	40	—	45	—	55	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	15	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	20	—	ns	
Column Address Hold Time Referenced to RAS	t_{RELAX}	t_{AR}	55	—	60	—	75	—	ns	
Column Address to RAS Lead Time	t_{AVREH}	t_{RAL}	35	—	40	—	50	—	ns	

NOTES: (continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100 µs is required after power–up followed by 8 RAS only refresh cycles or 8 CAS before RAS refresh cycles, before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specifications for t_{RC} (min) and t_{RMW} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0 \le T_A \le 70°C$) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. t_{OFF} (max) and t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.

READ, WRITE, AND READ–MODIFY–WRITE CYCLES (Continued)

Parameter	Symbol Std	Symbol Alt	MCM54800A–70 MCM5L4800A–70 MCM5V4800A–70 Min	Max	MCM54800A–80 MCM5L4800A–80 MCM5V4800A–80 Min	Max	MCM54800A–10 MCM5L4800A–10 MCM5V4800A–10 Min	Max	Unit	Notes
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	10
Read Command Hold Time Referenced to RAS	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{CELWH}	t_{WCH}	15	—	15	—	20	—	ns	
Read Command Hold Time Referenced to CAS	t_{RELWH}	t_{WCR}	55	—	60	—	75	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	15	—	15	—	20	—	ns	
Write Command to RAS Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	25	—	ns	
Write Command to CAS Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	25	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	11
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	20	—	ns	11
Data in Hold Time Referenced to RAS	t_{RELDX}	t_{DHR}	55	—	60	—	75	—	ns	
Refresh Period MCM54800A MCM5L4800A and MCM5V4800A	t_{RVRV}	t_{RFSH}	— —	16 128	— —	16 128	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	12
CAS to Write Delay	t_{CELWL}	t_{CWD}	50	—	50	—	60	—	ns	12
RAS to Write Delay	t_{RELWL}	t_{RWD}	100	—	110	—	135	—	ns	12
Column Address to Write Delay	t_{AVWL}	t_{AWD}	65	—	70	—	85	—	ns	12
CAS Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	70	—	75	—	90	—	ns	12
CAS Setup Time for CAS Before RAS Cycle	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
CAS Hold Time for CAS Before RAS Cycle	t_{RELCEH}	t_{CHR}	15	—	15	—	20	—	ns	
RAS Precharge to CAS Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
CAS Precharge Time (CAS Before RAS Counter Test)	t_{CEHCEL}	t_{CPT}	40	—	40	—	50	—	ns	
RAS Hold Time Referenced to G	t_{GLREH}	t_{ROH}	10	—	10	—	20	—	ns	
G Access Time	t_{GLQV}	t_{GA}	—	20	—	20	—	25	ns	6
G to Data Delay	t_{GLHDX}	t_{GD}	20	—	20	—	25	—	ns	
Output Buffer Turn–Off Delay Time from G	t_{GHQZ}	t_{GZ}	0	20	0	20	0	25	ns	7
G Command Hold Time	t_{WLGL}	t_{GH}	20	—	20	—	25	—	ns	
Output Disable Setup Time	t_{GLCEL}	t_{GDS}	0	—	0	—	0	—	ns	

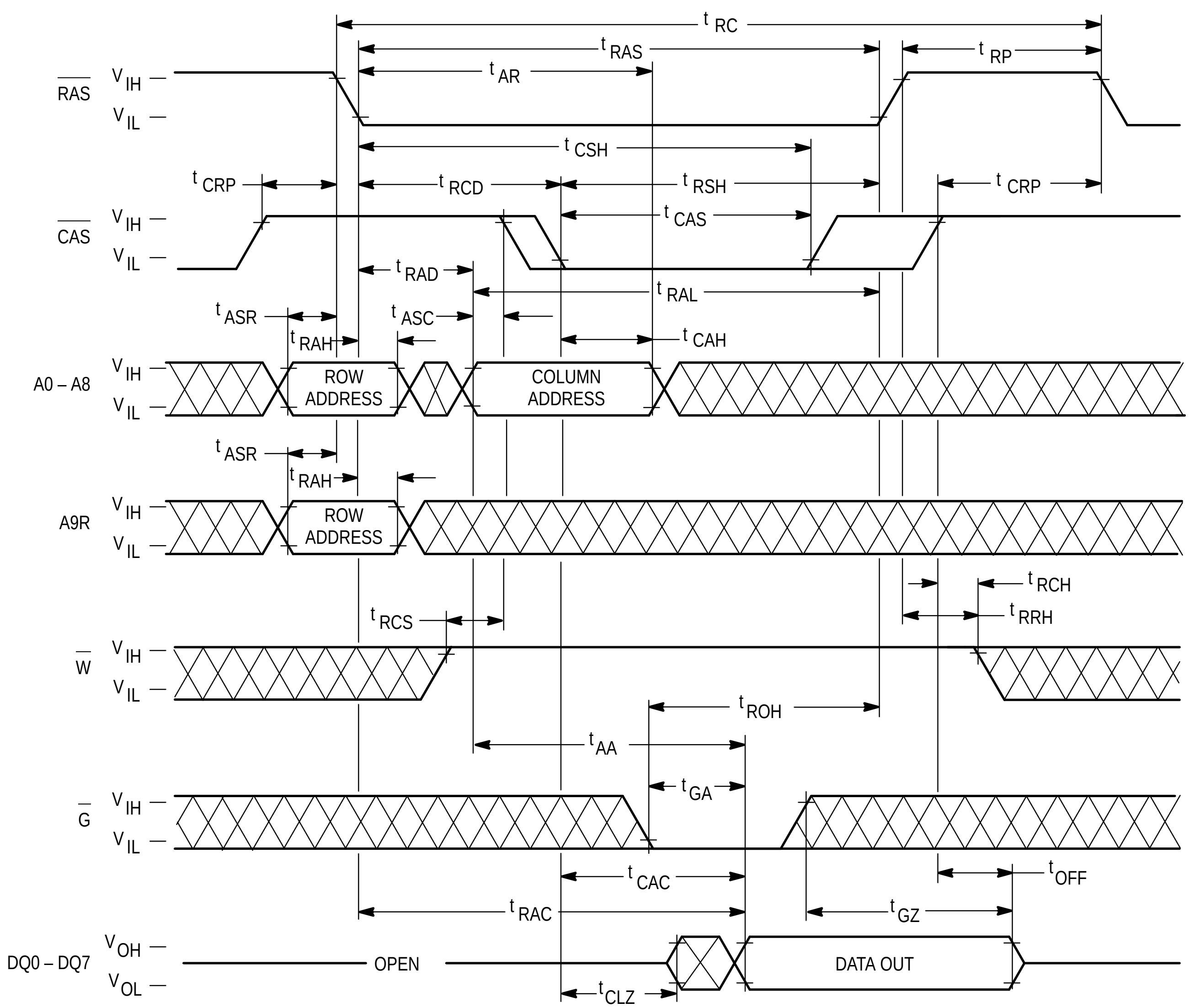
NOTES:

10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. These parameters are referenced to CAS leading edge in early write cycles and to W leading edge in late write or read–write cycles.
12. t_{WCS}, t_{RWD}, t_{CWD}, t_{CPWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{CPWD} \geq t_{CPWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read–modify–write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

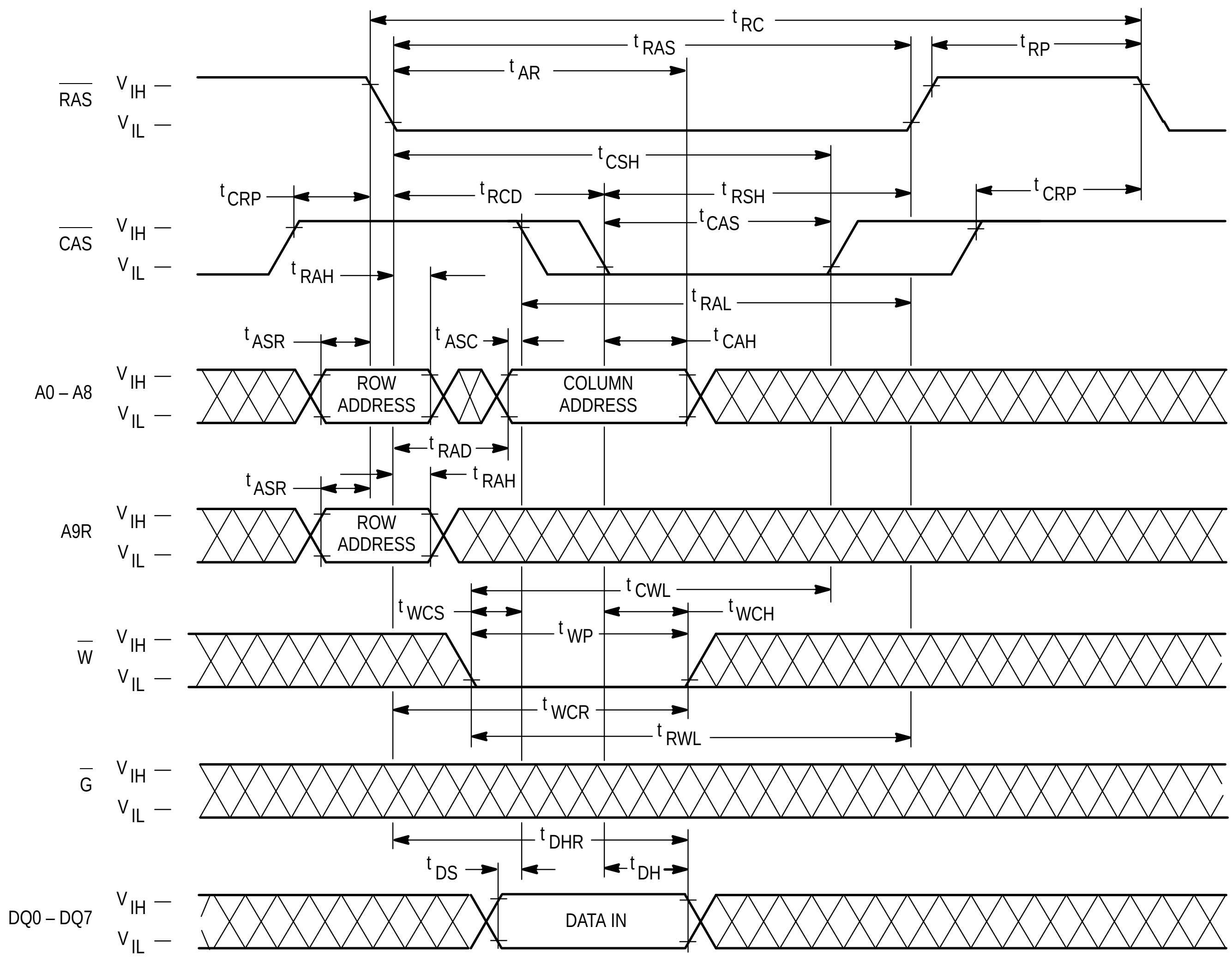
SELF REFRESH CYCLE

Parameter	Symbol Std	Symbol Alt	MCM54800A–70 MCM5L4800A–70 MCM5V4800A–70 Min	Max	MCM54800A–80 MCM5L4800A–80 MCM5V4800A–80 Min	Max	MCM54800A–10 MCM5L4800A–10 MCM5V4800A–10 Min	Max	Unit	Notes
RAS Pulse Width (CAS Before RAS Self Refresh, MCM5V4800A Only)	$t_{RELREHS}$	t_{RASS}	100	—	100	—	100	—	µs	
RAS Precharge Time (CAS Before RAS Self Refresh, MCM5V4800A Only)	$t_{REHRELS}$	t_{RPS}	130	—	150	—	180	—	ns	
CAS Hold Time (CAS Before RAS Self Refresh, MCM5V4800A Only)	t_{REHCEH}	t_{CHS}	– 50	—	– 60	—	– 70	—	ns	

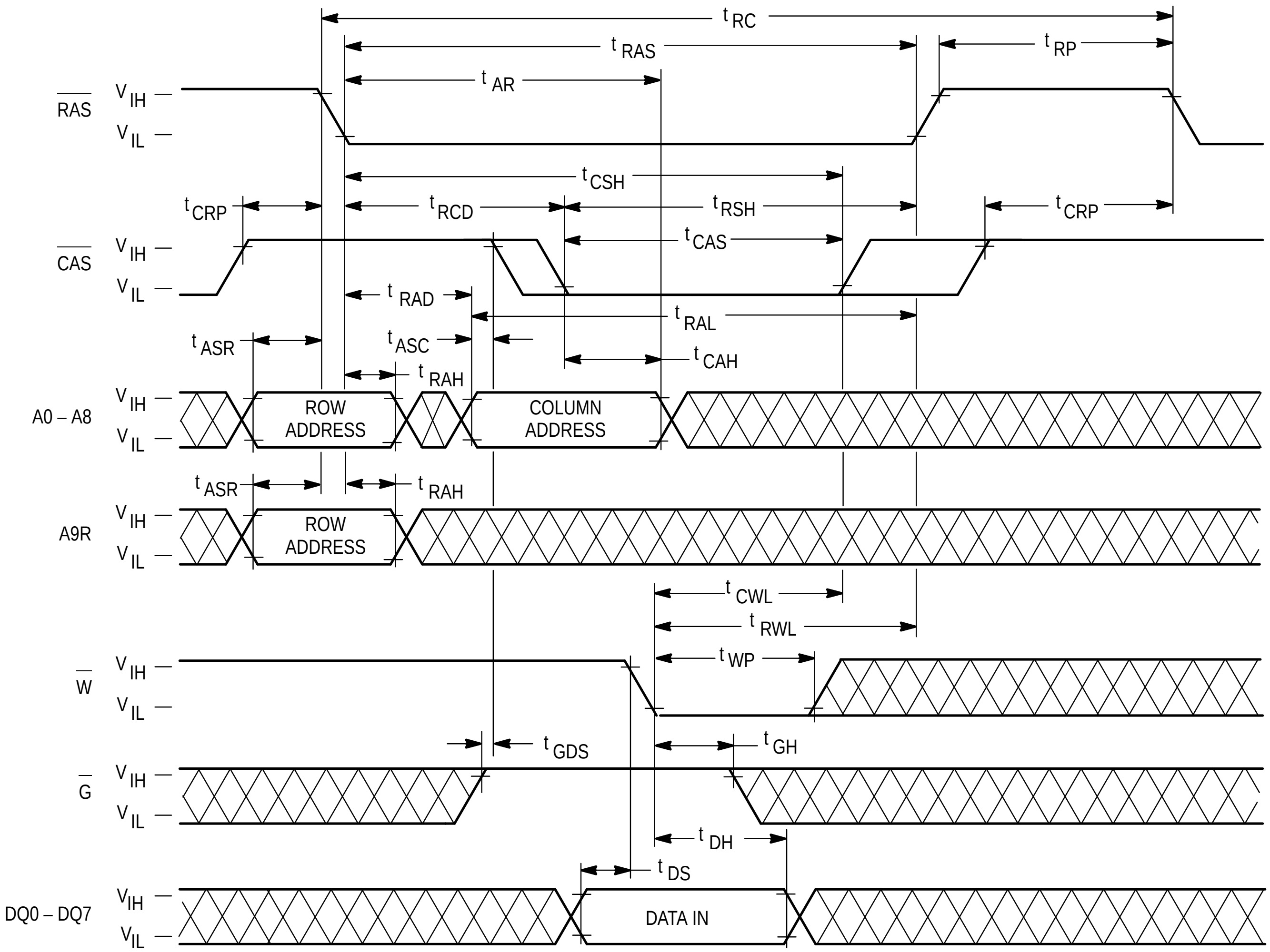
READ CYCLE



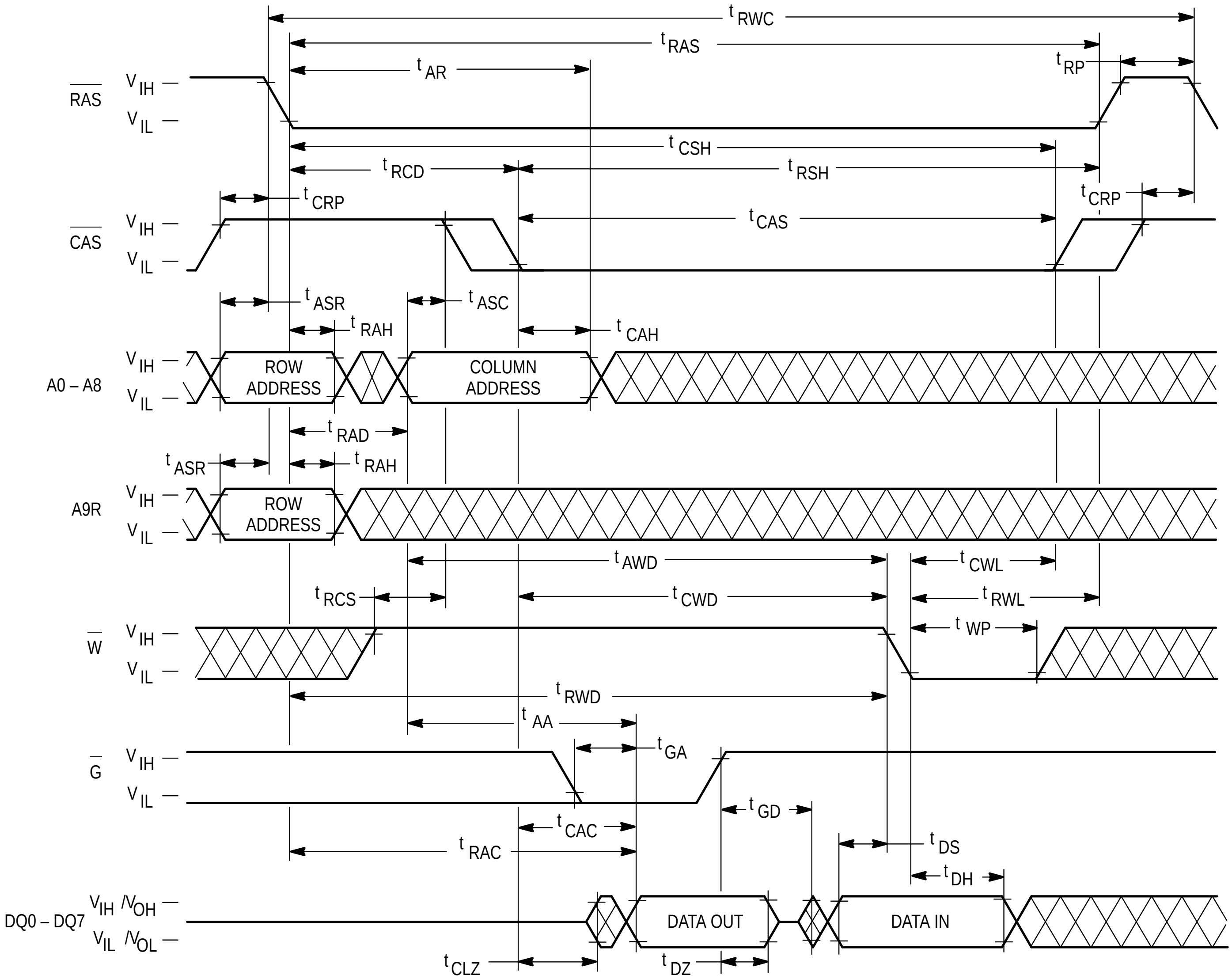
EARLY WRITE CYCLE



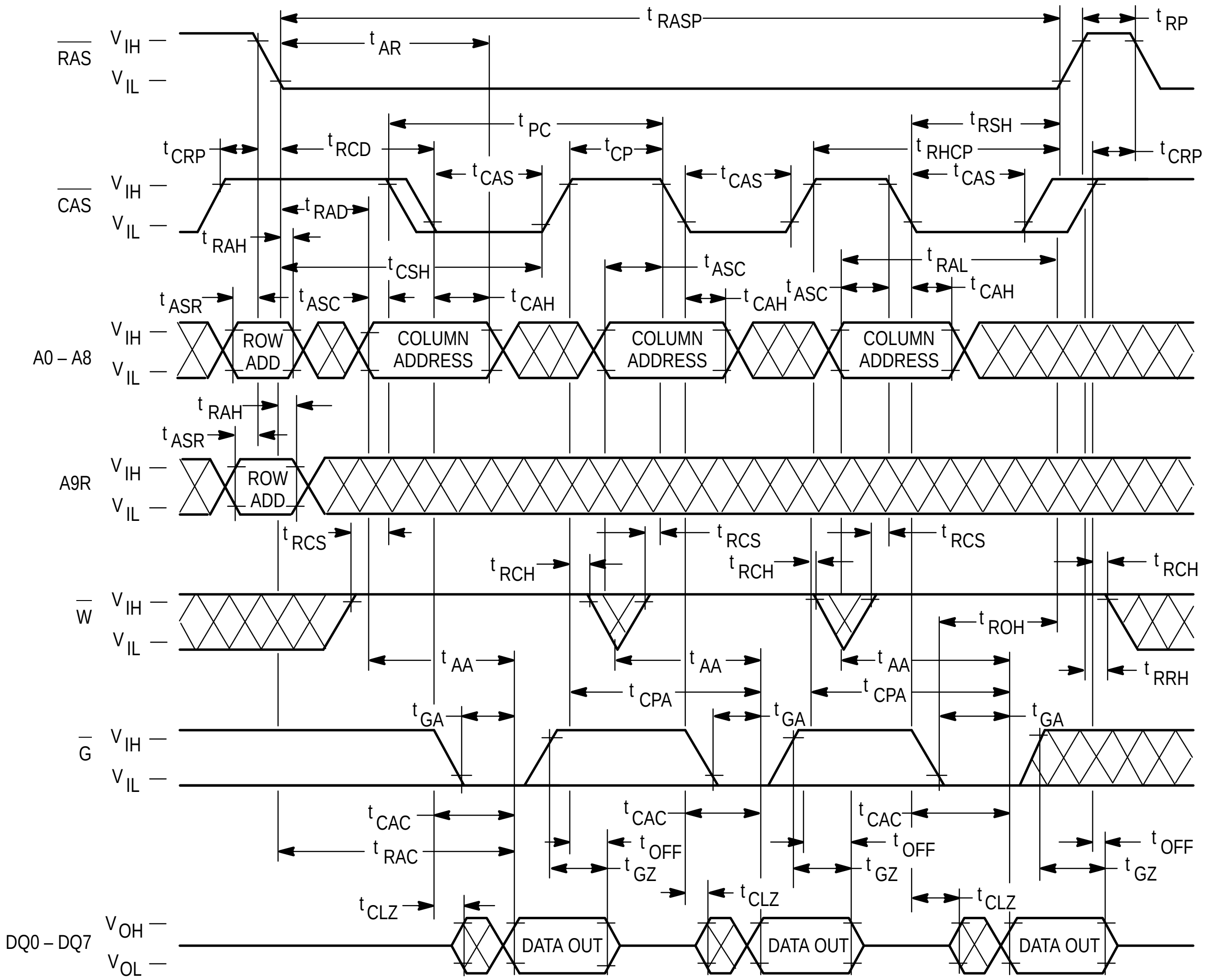
$\overline{G}$ CONTROLLED WRITE CYCLE



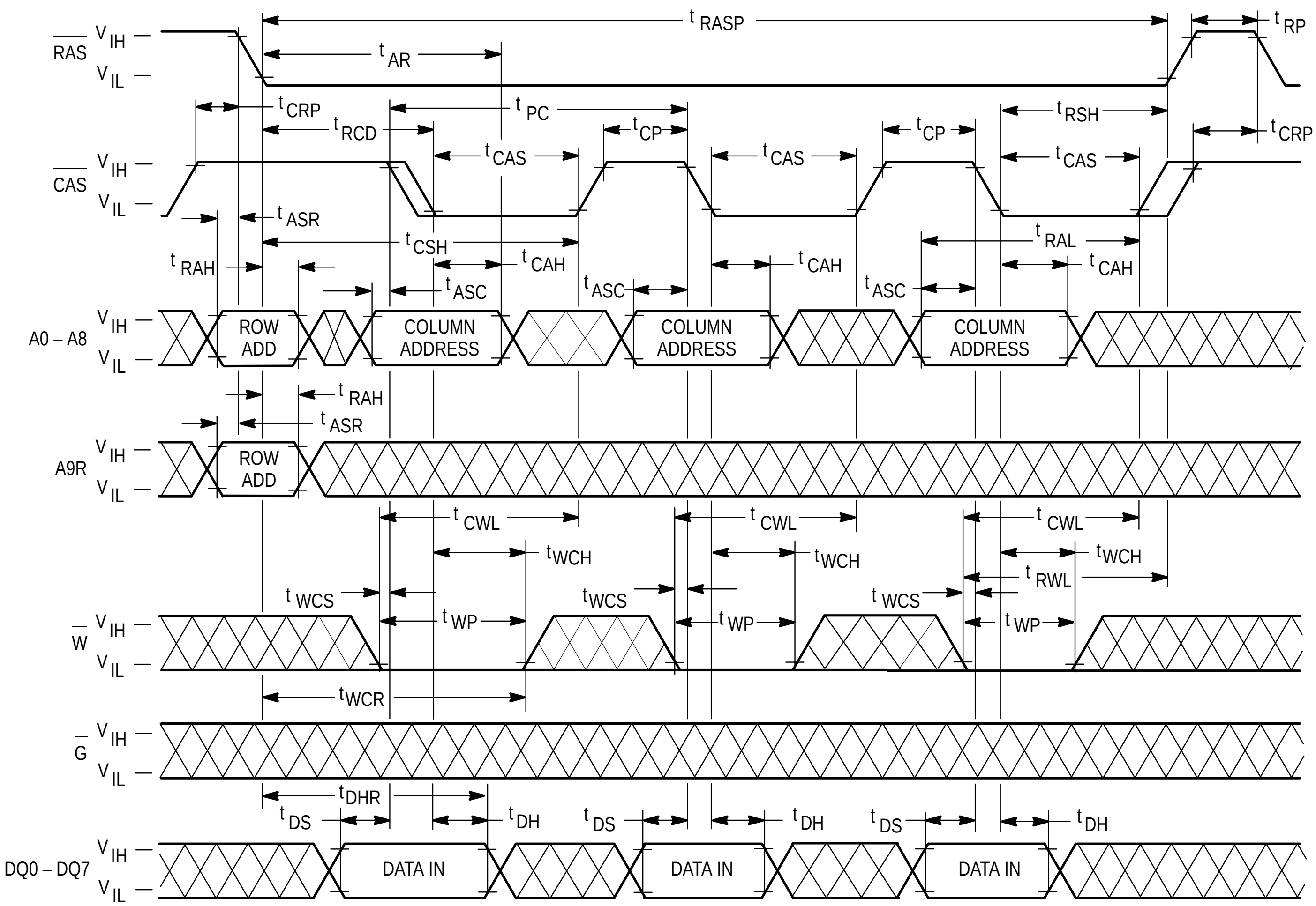
READ–MODIFY–WRITE CYCLE



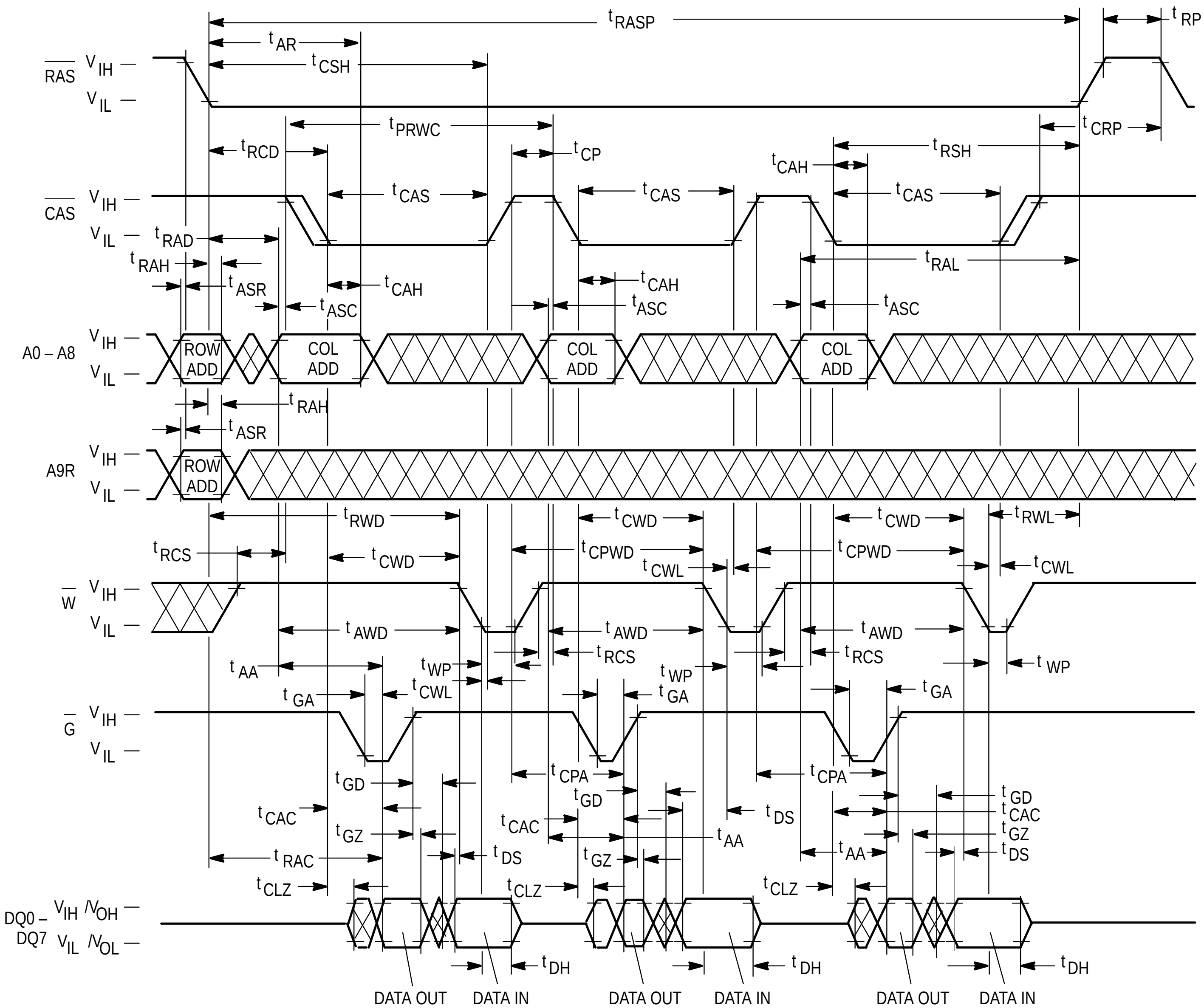
FAST PAGE MODE READ CYCLE



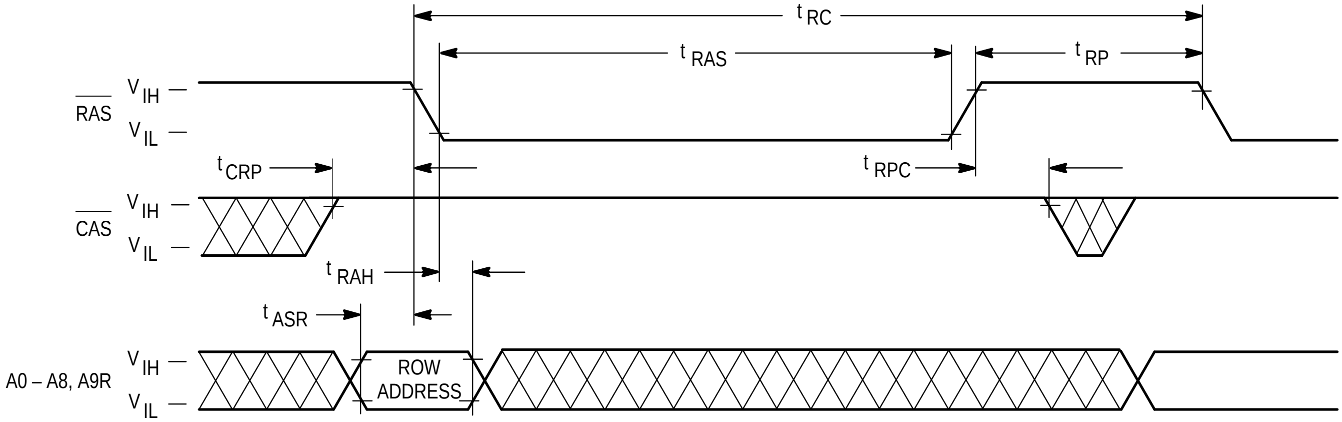
FAST PAGE MODE WRITE CYCLE



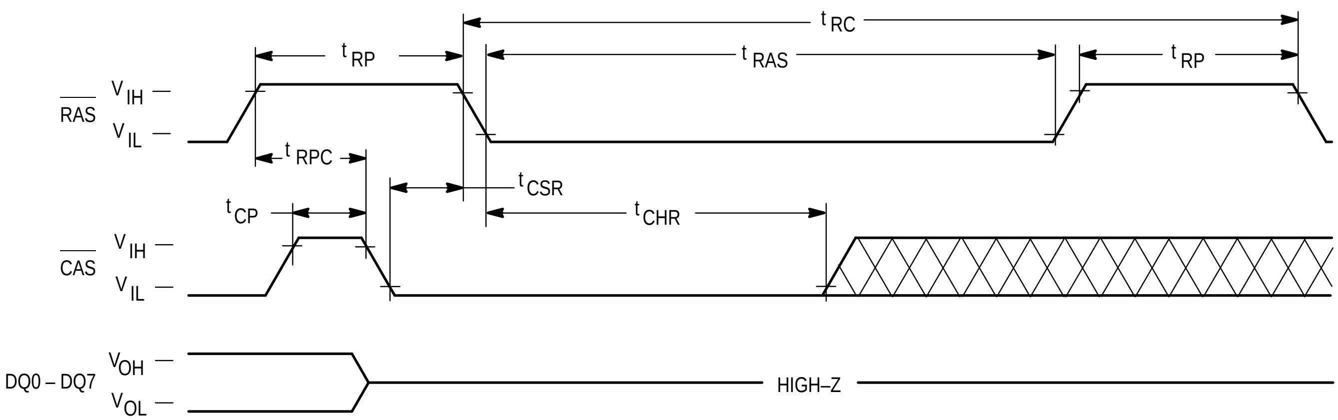
FAST PAGE MODE READ–MODIFY–WRITE CYCLE



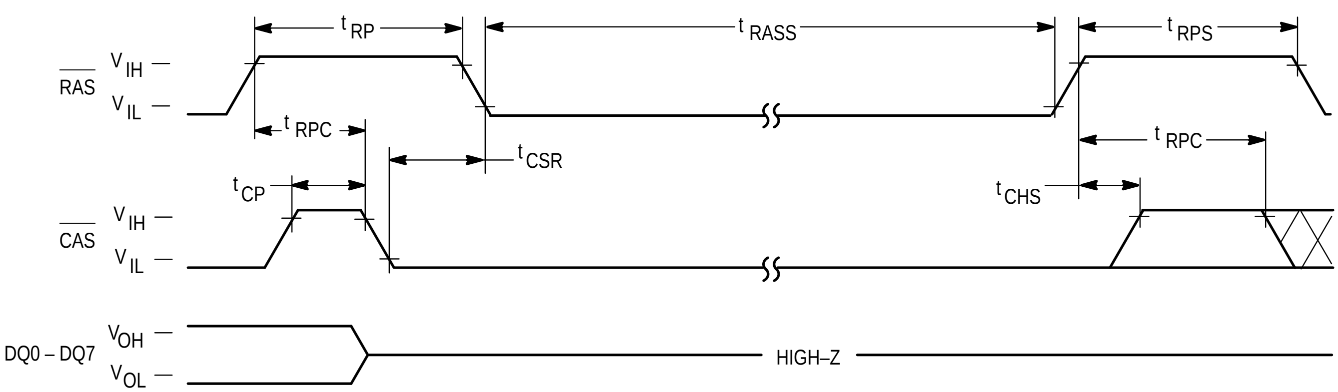
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE



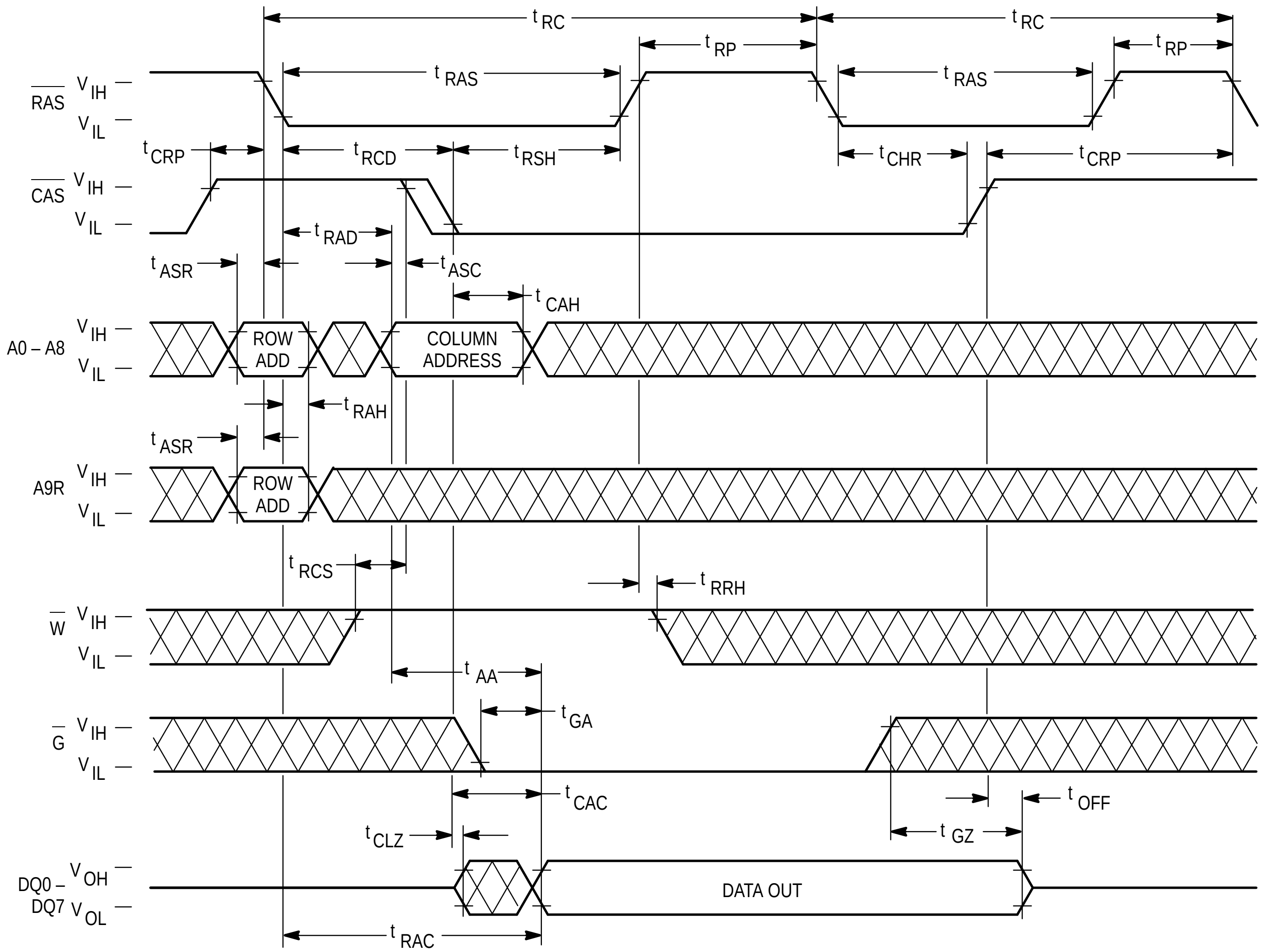
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



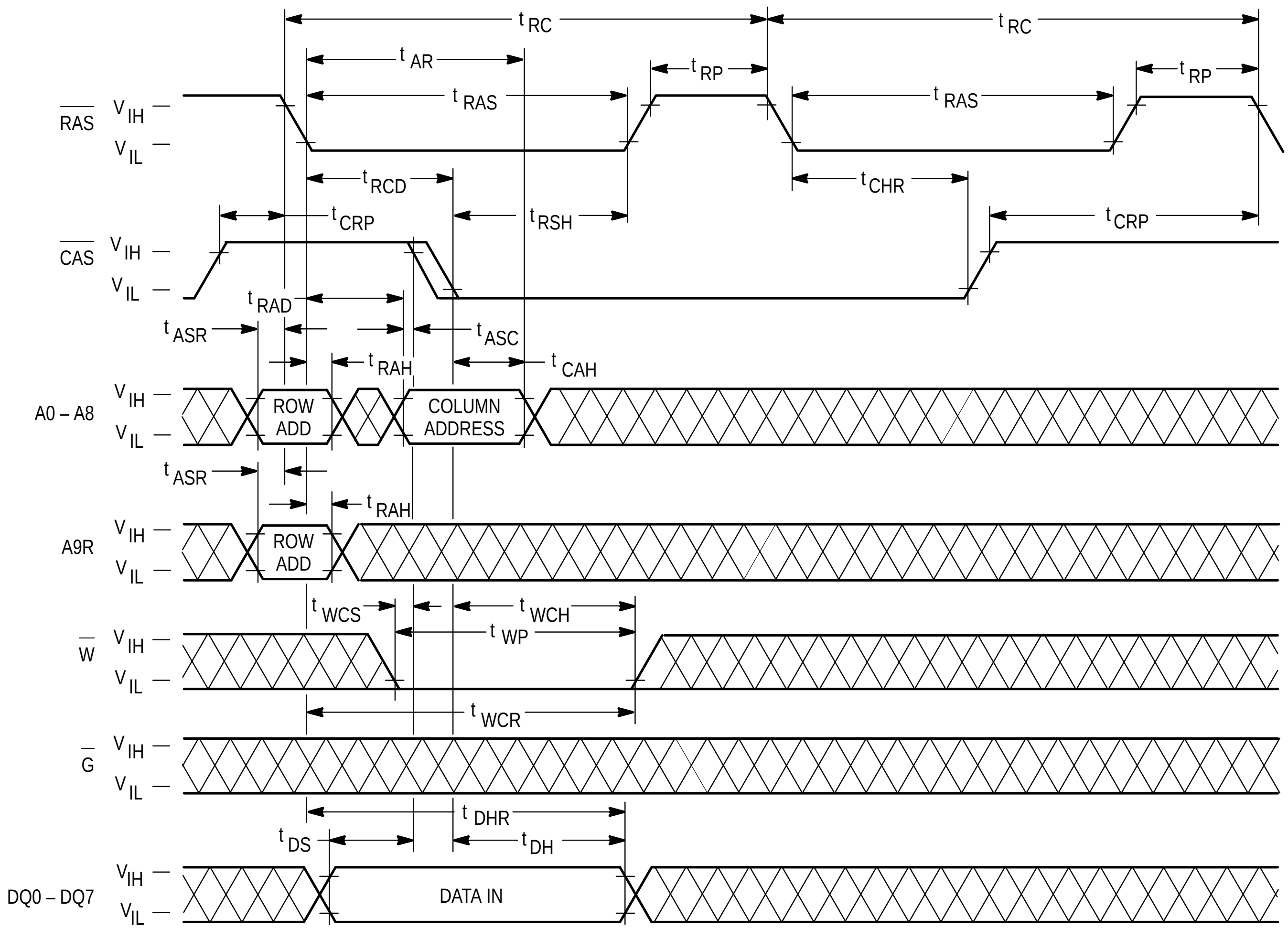
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ SELF REFRESH CYCLE (MCM5V4800A ONLY)



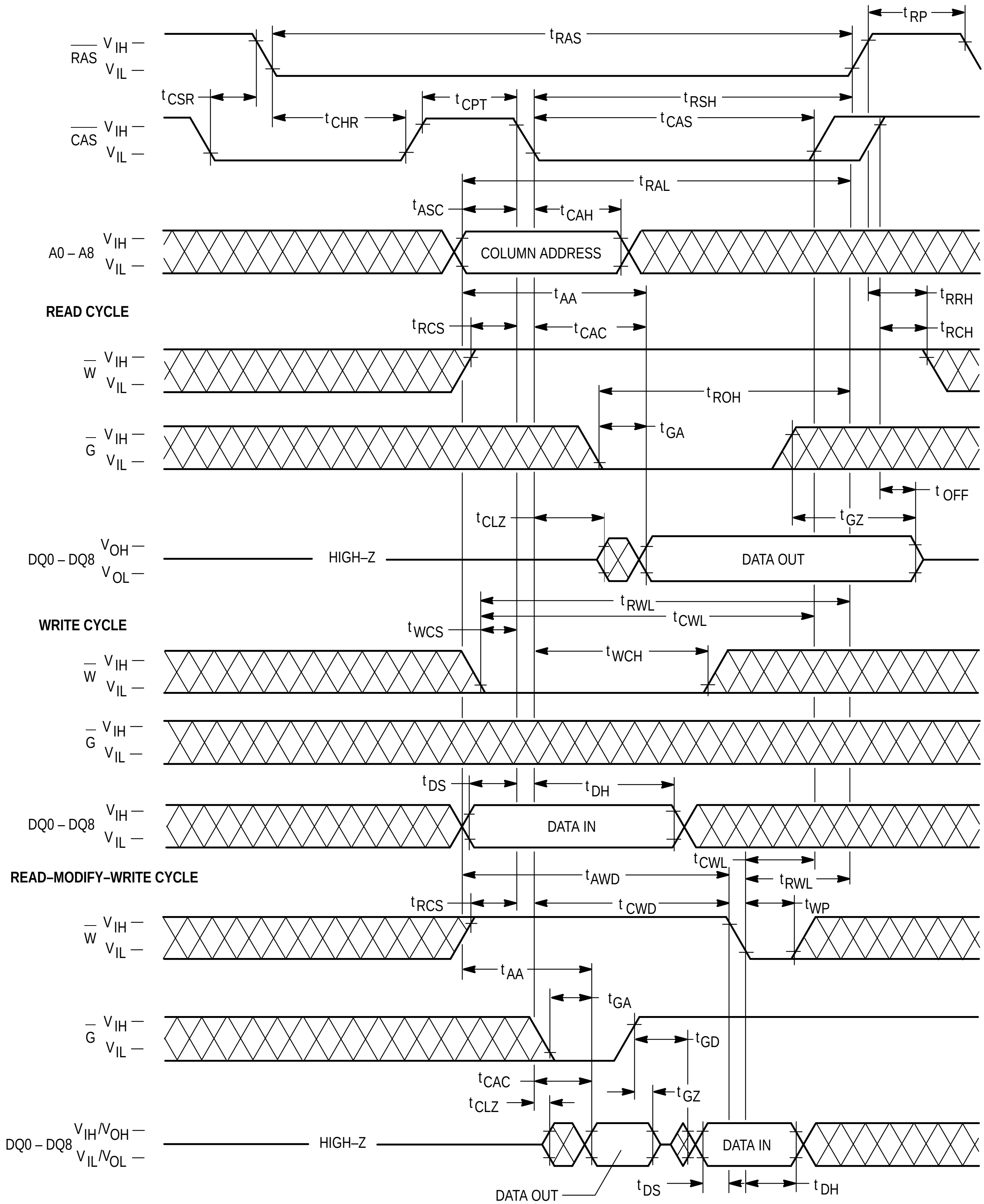
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power–up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight RAS–Only refresh cycles or CAS–Before–RAS refresh cycles to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds with the device powered up), a wake up sequence of eight RAS–Only refresh cycles or CAS–Before–RAS refresh cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks and will decode one of the 524,288 bit locations in the device. The row address strobe (RAS) latches 10 row addresses, and the column access strobe CAS latches nine column addresses. RAS active transition followed by CAS active transition (active = V_{IL}, t_{RCD} minimum) follows RAS on all read or write cycles. The delay between RAS and CAS active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

There are three other variations in addressing the 512K x 8 RAM: **RAS–only refresh cycle, CAS before RAS refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: “normal” random read cycle, page mode read cycle, read–write cycle, and page mode read–write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with RAS and CAS active transitions latching the desired bit location. The write (W) input level must be high (V_{IH}), t_{RCS} (minimum) before the CAS active transition, to enable read mode.

Both the RAS and CAS clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both CAS and output enable (G) control read access time: CAS must be active before or at t_{RCD} maximum, and G must be active $t_{RAC} - t_{GA}$ (both minimum) to guarantee valid data out (Q) at t_{RAC} (access time from RAS active transition). If the t_{RCD} maximum is exceeded and/or G active transition does not occur in time, read access time is determined by either the CAS or G clock active transition (t_{CAC} or t_{GA}).

The RAS and CAS clocks must remain active for a minimum time of t_{RAS} and t_{CAS}, respectively, to complete the read cycle. W must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after RAS or CAS inactive transition, respectively, to maintain the data at that bit location. Once RAS transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the CAS and G clocks are active. When either the CAS or G clock transitions to inactive, the output will switch to High–Z (three–state) t_{OFF} or t_{GZ} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read–write. Early and late write modes are discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of W to active (V_{IL}). Early and late write modes are distinguished by the active transition of W, with respect to CAS. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by W active transition at minimum time t_{WCS} before CAS active transition. Data in (D) is referenced to CAS in an early write cycle. RAS and CAS clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three–state condition throughout an early write cycle because W active transition precedes or coincides with CAS active transition, keeping data–out buffers and G disabled.

A late write cycle (referred to as G–controlled write) occurs when W active transition is made after CAS active transition. W active transition could be delayed for almost 10 ms after CAS active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D is referenced to W active transition in a late write cycle. Output buffers are enabled by CAS active transition but outputs are switched off by G inactive transition, which is required to write to the device. Q may be indeterminate — see note 12 of AC Operating Conditions table. RAS and CAS must remain active for t_{RWL} and t_{CWL}, respectively, after W active transition to complete the write cycle. G must remain inactive for t_{GH} after W active transition to complete the write cycle.

READ–WRITE CYCLE

A read–write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except W must remain high for t_{CWD} minimum after the CAS active transition, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the 512K x 8 dynamic RAM. Read access time in page mode (t_{CAC}) is typically half the regular RAS clock access time, t_{RAC}. Page mode operation consists of keeping RAS active while toggling CAS between V_{IH} and V_{IL}. The row is latched by RAS active transition, while each CAS active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read–write cycle, as described in the prior sections. Once the timing requirements for the first cycle are met, CAS transitions to inactive for minimum t_{CP}, while RAS remains low (V_{IL}). The second CAS active transition while RAS is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read–write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by

t_{RASP}. Page mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM54800A require refresh every 16 milliseconds, while refresh for the MCM5L4800A and MCM5V4800A is 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM54800A, and 124.8 microseconds for the MCM5L4800A and MCM5V4800A. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM54800A, and 128 milliseconds for the MCM5L4800A and MCM5V4800A.

A normal read, write, or read–write operation to the RAM will refresh all the bits (4096) associated with the particular row decodes. Three other methods of refresh, **RAS–only refresh, CAS before RAS refresh, hidden refresh,** and **self refresh** (MCM5V4800A only) are available on this device for greater system flexibility.

RAS–Only Refresh

RAS–only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure that all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order actives an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh).

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1).

Self Refresh (MCM5V4800A Only)

The self refresh is a CAS before RAS refresh where RAS is held low for a period greater than t_{RASS} (100 microseconds). After this time, an internal timer activates a refresh operation of consecutive row addresses in the dynamic RAM. The self refresh mode is exited when either RAS or CAS transitions to high (V_{IH}). Because of the long periods involved for this method of refresh, it is recommended that the self refresh mode only be used for long periods of standby, such as a battery backup.

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This test is performed with a read–write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed after a minimum of **eight CAS before RAS** initialization cycles. Test procedure:

1. Write 0s into all memory cells with normal write mode.
2. Select a column address, read 0 out and write 1 into the cell by performing the **CAS before RAS refresh counter test, read–write cycle**. Repeat this operation 1024 times.
3. Read the 1s which were written in step two in normal read mode.
4. Using the same starting column address as in step two, read one out and write 0 into the cell by performing the **CAS before RAS refresh counter test, read–write cycle**. Repeat this operation 1024 times.
5. Read 0s which were written in step four in normal read mode.
6. Repeat steps one through five using complement data.

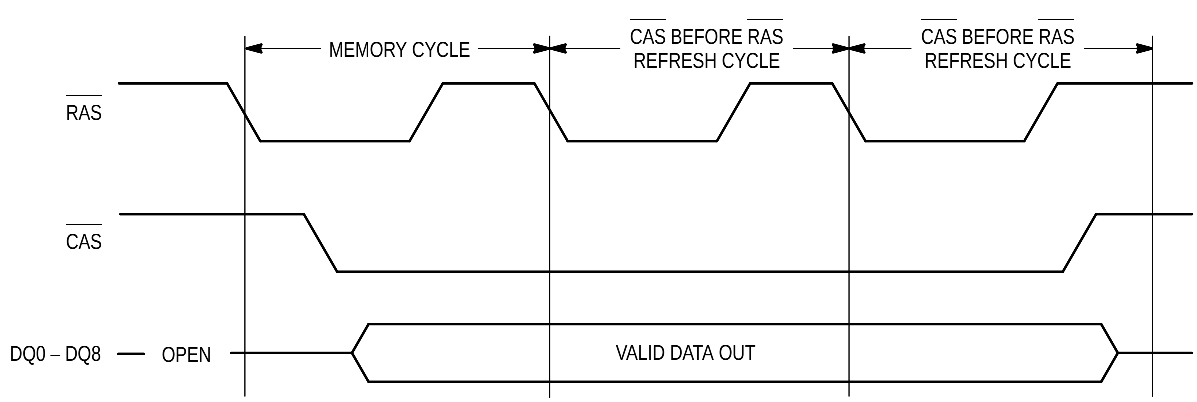


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

MCM 54800A XX X XX XX

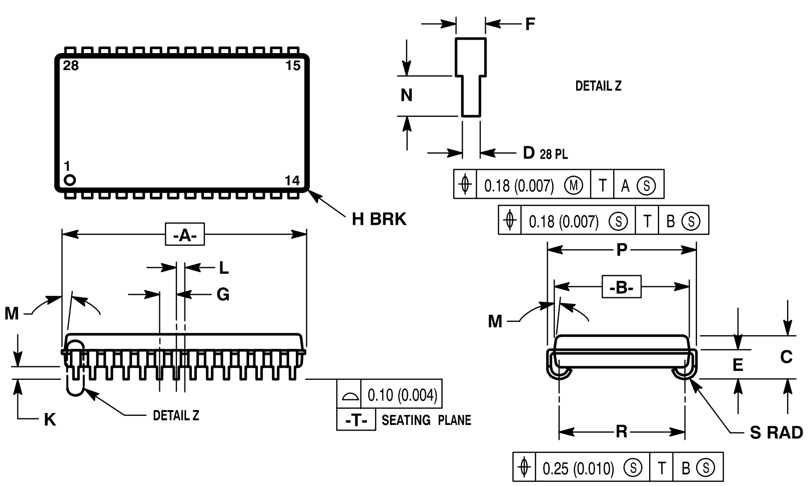
- MCM — Motorola Memory Prefix
- 54800A — Part Number
- XX — Package (J = 400 mil SOJ, T = 400 mil TSOP)
- X — Temperature Range (C = 0 to 70°C)
- XX — Speed (70 = 70 ns, 80 = 80 ns, 10 = 100 ns)
- XX — Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers —

MCM54800AJ70	MCM54800AJ70R2	MCM54800AT70	MCM54800AT70R2
MCM54800AJ80	MCM54800AJ80R2	MCM54800AT80	MCM54800AT80R2
MCM54800AJ10	MCM54800AJ10R2	MCM54800AT10	MCM54800AT10R2
MCM5L4800AJ70	MCM5L4800AJ70R2	MCM5L4800AT70	MCM5L4800AT70R2
MCM5L4800AJ80	MCM5L4800AJ80R2	MCM5L4800AT80	MCM5L4800AT80R2
MCM5L4800AJ10	MCM5L4800AJ10R2	MCM5L4800AT10	MCM5L4800AT10R2
MCM5V4800AJ70	MCM5V4800AJ70R2	MCM5V4800AT70	MCM5V4800AT70R2
MCM5V4800AJ80	MCM5V4800AJ80R2	MCM5V4800AT80	MCM5V4800AT80R2
MCM5V4800AJ10	MCM5V4800AJ10R2	MCM5V4800AT10	MCM5V4800AT10R2

PACKAGE DIMENSIONS

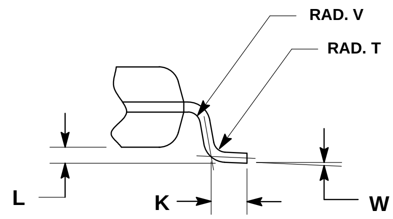
J PACKAGE
400 MIL SOJ
CASE 810–03



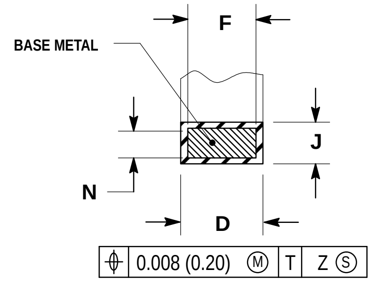
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. DIMENSION A & B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
3. CONTROLLING DIMENSION: INCH.
4. DIM R TO BE DETERMINED AT DATUM -T-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.29	18.54	0.720	0.730
B	10.04	10.28	0.395	0.405
C	3.26	3.75	0.128	0.148
D	0.39	0.50	0.015	0.020
E	2.24	2.48	0.088	0.098
F	0.67	0.81	0.026	0.032
G	1.27 BSC		0.050 BSC	
H	—	0.50	—	0.020
K	0.89	1.14	0.035	0.045
L	0.64 BSC		0.025 BSC	
M	0°	5°	0°	5°
N	0.76	1.14	0.030	0.045
P	11.05	11.30	0.435	0.445
R	9.15	9.65	0.360	0.380
S	0.77	1.01	0.030	0.040

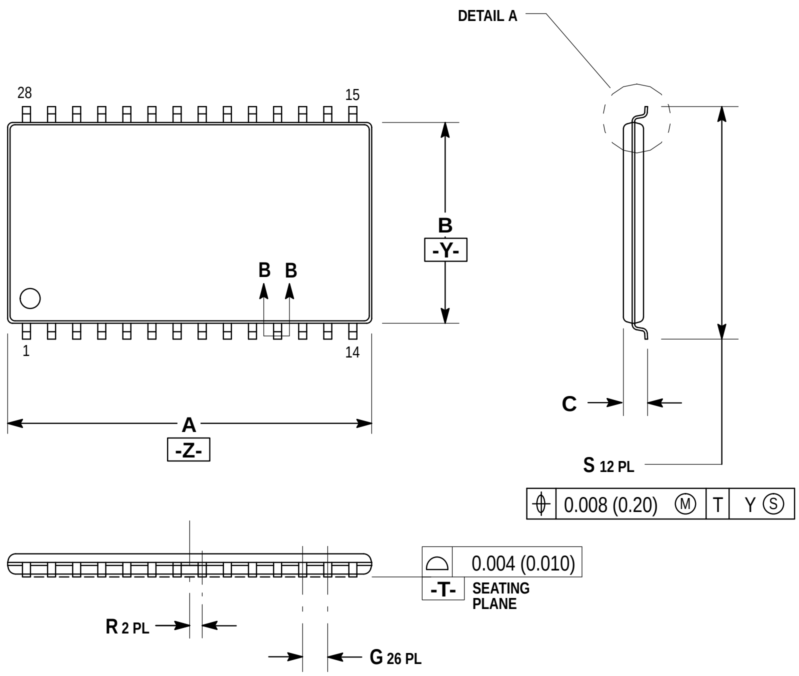
T PACKAGE
400 MIL TSOP
CASE 899–01



DETAIL A
ROTATED 90° CW



SECTION B-B



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION IS .006 (0.15) PER SIDE.
4. DIMENSION D DOES NOT INCLUDE DAM BAR PROTRUSIONS. ALLOWABLE PROTRUSION IS .007 (0.18), TOTAL, IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	18.34	18.52	0.721	0.729
B	10.05	10.26	0.396	0.404
C	—	1.27	—	0.050
D	0.33	0.48	0.013	0.019
F	0.33	0.43	0.013	0.017
G	1.27 BASIC		0.050 BASIC	
J	0.12	0.20	0.005	0.008
K	0.41	0.58	0.016	0.023
L	0.02	0.18	0.001	0.007
N	0.11	0.16	0.004	0.006
R	0.635 BASIC		0.025 BASIC	
S	11.59	11.93	0.456	0.470
T	0.10 BASIC		0.004 REF	
V	0.10 BASIC		0.004 REF	
W	0°	5°	0°	5°

How to reach us:
USA / EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298