MOTOROLA
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4M x 4

MCM417400

Fast Page Mode
2048 Cycle Refresh

Advance Information

16M CMOS Dynamic RAM Family

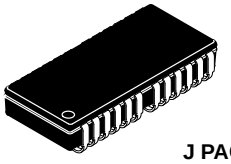
Fast Page Mode x4 2K Refresh

The family of 16M dynamic RAMs is fabricated using sub–micron CMOS high–speed silicon–gate process technology. It includes devices organized as 4,194,304 four–bit words. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

The MCM417400 is a x4 device with 2048 cycle refresh, requiring only 11 address lines.

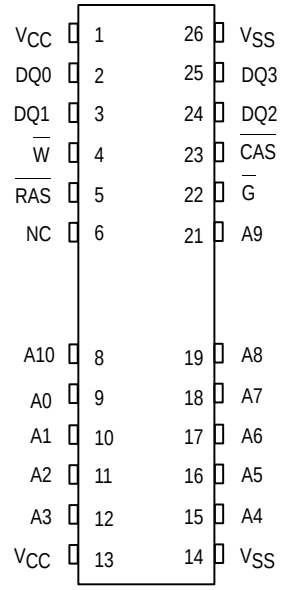
The device is packaged in a standard 300 mil J–lead small outline package (SOJ).

- Three–State Data Output
- Fast Page Mode
- TTL–Compatible Inputs and Outputs
- RAS–Only Refresh
- CAS Before RAS Refresh
- Hidden Refresh
- 2048 Cycle Refresh: = 32 ms
- Fast Access Time (t_{RAC}):
  MCM417400–60 = 60 ns (Max)
  MCM417400–70 = 70 ns (Max)
- Low Active Power Dissipation:
  MCM417400–60 = 605 mW (Max)
  MCM417400–70 = 550 mW (Max)
- Low Standby Power Dissipation:
  CMOS Levels = 5.5 mW (Max)



J PACKAGE
300 MIL SOJ
CASE 880B–01

PIN ASSIGNMENT
300 MIL SOJ



PIN NAMES	
A0 – A10 . . . . . Address Input	CAS . . . . . Column Address Strobe
DQ0 – DQ3 . . . . . Data Input/Output	V_{CC} . . . . . Power Supply (+ 5 V)
G . . . . . Output Enable	V_{SS} . . . . . Ground
W . . . . . Read/Write Enable	NC . . . . . No Connection
RAS . . . . . Row Address Strobe	

This document contains information on a new product. Specifications and information herein are subject to change without notice.

10/95

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current	I_{out}	50	mA
Power Dissipation	P_D	1.0	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	6.5	V
Logic Low Voltage, All Inputs	V_{IL}	– 1.0	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS (All voltages referenced to V_{SS})

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current	I_{CC1}			mA	1, 2
MCM417400–60, t_{RC} = 110 ns		—	110		
MCM417400–70, t_{RC} = 130 ns		—	100		
V_{CC} Power Supply Current (Standby) (RAS = CAS = V_{IH}) Output Open	I_{CC2}	—	2	mA	
V_{CC} Power Supply Current During RAS–Only Refresh Cycles (RAS = V_{IH})	I_{CC3}			mA	2
MCM417400–60, t_{RC} = 110 ns		—	110		
MCM417400–70, t_{RC} = 130 ns		—	100		
V_{CC} Power Supply Current During Fast Page Mode Cycle (RAS = V_{IL})	$I_{CC4(P)}$			mA	1, 2
MCM417400–60, t_{PC} = 40 ns		—	80		
MCM417400–70, t_{PC} = 45 ns		—	70		
V_{CC} Power Supply Current (Standby) (RAS = CAS = V_{CC} – 0.2 V)	I_{CC5}	—	1.0	mA	
V_{CC} Power Supply Current During CAS Before RAS Refresh Cycle	I_{CC6}			mA	
MCM417400–60, t_{RC} = 110 ns		—	110		
MCM417400–70, t_{RC} = 130 ns		—	100		
Input Leakage Current (0 V ≤ V_{in} ≤ V_{CC})	$I_{lkg(I)}$	–10	10	µA	
Output Leakage Current (0 V ≤ V_{out} ≤ V_{CC}, Output Disable)	$I_{lkg(O)}$	–10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	V_{CC}	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	0	0.4	V	

NOTES:
1. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
2. Address may be changed once or less while RAS = V_{IL}. In the case of I_{CC4}, it can be changed once or less during t_{PC}.

CAPACITANCE (T_A = 25°, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit	Notes
Input Capacitance	A0 – A10	C_{in}	5	pF	1
	$\overline{G}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$		7		
Output Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	DQ0 – DQ3	$C_{I/O}$	7	pF	1, 2

NOTES:
1. Capacitance measured with a Boonton Meter or effective capacitance measuring method.
2. CAS = V_{IH} to disable outputs.

16M FAMILY AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

ALL DEVICES: READ, WRITE, AND READ–WRITE CYCLES (See Notes 1, 2, 3, 4, and 15)

Parameter	Symbol		MCM417400–60		MCM417400–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	ns	5
Read–Write Cycle Time	t_{RELREL}	t_{RWC}	155	—	181	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	—	70	ns	6, 8, 17
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	15	—	18	ns	6, 10, 14, 17
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	ns	6, 7, 9, 14, 17
$\overline{CAS}$ to Output in Low–Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	
Output Buffer and Turn–Off Delay	t_{CEHQZ}	t_{OFF}	—	15	—	15	ns	11
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	1
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	15	—	18	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	ns	
$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	t_{CEHREH}	t_{RHCP}	35	—	40	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	15	10 k	18	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	45	20	52	ns	12
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	ns	13
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	10	—	15	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	ns	

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 μs is required after power–up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 μA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \le t_{RCD}$ (max) and $t_{RAD} \le t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in the table, t_{RAC} exceeds t_{RAC} (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. Assumes that $t_{RCD} \ge t_{RCD}$ (max) and $t_{RAD} \le t_{RAD}$ (max).
11. t_{OFF} (max) and t_{GZ} (max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
12. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
13. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by t_{AA}.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
15. In late write or read–write cycles, G must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OEH} \ge t_{CWL}$, the I/O pin will remain open circuit (high impedance); if $t_{OEH} \le t_{CWL}$, invalid data will be out at each I/O.

ALL DEVICES, READ, WRITE, AND READ–WRITE CYCLES (Continued)

Parameter	Symbol		MCM417400–60		MCM417400–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to CAS	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	16
Read Command Hold Time Referenced to RAS	t_{REHWX}	t_{RRH}	0	—	0	—	ns	16
Write Command Hold Time Referenced to CAS	t_{CELWH}	t_{WCH}	10	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	10	—	ns	
Write Command to RAS Lead Time	t_{WLREH}	t_{RWL}	15	—	18	—	ns	
Write Command to CAS Lead Time	t_{WLCEH}	t_{CWL}	15	—	18	—	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	18
Data In Hold Time	t_{CELDX}	t_{DH}	10	—	15	—	ns	18
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	19
CAS to Write Delay	t_{CELWL}	t_{CWD}	40	—	46	—	ns	19
RAS to Write Delay	t_{RELWL}	t_{RWD}	85	—	98	—	ns	19
Column Address to Write Delay	t_{AVWL}	t_{AWD}	55	—	63	—	ns	19
Refresh Period	t_{RVRV}	t_{RFSH}	—	32	—	32	ms	
CAS Setup Time for CAS Before RAS Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	ns	
CAS Hold Time for CAS Before RAS Refresh	t_{RELCEH}	t_{CHR}	10	—	10	—	ns	
RAS Precharge to CAS Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	ns	
CAS Precharge Time for CAS Before RAS Counter Time	t_{CEHCEL}	t_{CPT}	20	—	30	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	0	—	0	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	ns	
Write to RAS Precharge Time (CAS Before RAS Refresh)	t_{WHREL}	t_{WRP}	0	—	0	—	ns	
Write to RAS Hold Time (CAS Before RAS Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	ns	
G Access Time	t_{GLQV}	t_{GA}	—	15	—	18	ms	17, 20
G to Data Delay	t_{GLHDX}	t_{GD}	15	—	18	—	ns	21
Output Buffer Turn–off Delay Time From G	t_{GHQZ}	t_{GZ}	—	15	—	15	ns	11
G Command Hold Time	t_{WLGL}	t_{GH}	15	—	18	—	ns	

NOTES: (continued)

16. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC}, and t_{CPA} is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
18. These parameters are referenced to CAS leading edge in early write cycles and to W leading edge in late write or read–write cycles.
19. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min), the cycle is a read–write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
20. Measured with a current load equivalent to 2 TTL (–200 µA + 4mA) loads and 100 pF with the data output trip points set at V_{OH} = 2 V, and V_{OL} = 0.8 V.
21. t_{GD} must be satisfied.

16M FAMILY AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

FAST PAGE MODE READ, WRITE, AND READ–WRITE CYCLES (See Notes 1, 2, 3, 4, and 9)

Parameter	Symbol		MCM417400–60		MCM417400–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	40	—	45	—	ns	
Access Time from Precharge CAS	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	5, 7, 8
CAS Precharge to RAS Hold Time	t_{CEHREH}	t_{RHCP}	35	—	40	—	ns	
Fast Page Mode Read–Write Cycle Time	t_{CELCEL}	t_{PRWC}	85	—	96	—	ns	
RAS Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	10 k	70	10 k	ns	
CAS Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	60	—	68	—	ns	6

NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power–up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. Measured with a current load equivalent to 2 TTL (–200 µA, + 4mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V, and V_{OL} = 0.8 V.
6. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min), the cycle is a read–write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
7. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
8. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC}, and t_{CPA} is delayed by 2 ns to 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
9. In late write or read–write cycles, G must disable output buffer prior to applying data to the device. After RAS is reset, if $t_{OEH} \geq t_{CWL}$, the I/O pin will remain open circuit (high Impedance); if $t_{OEH} \leq t_{CWL}$, invalid data will be out at each I/O.

TIMING DIAGRAMS

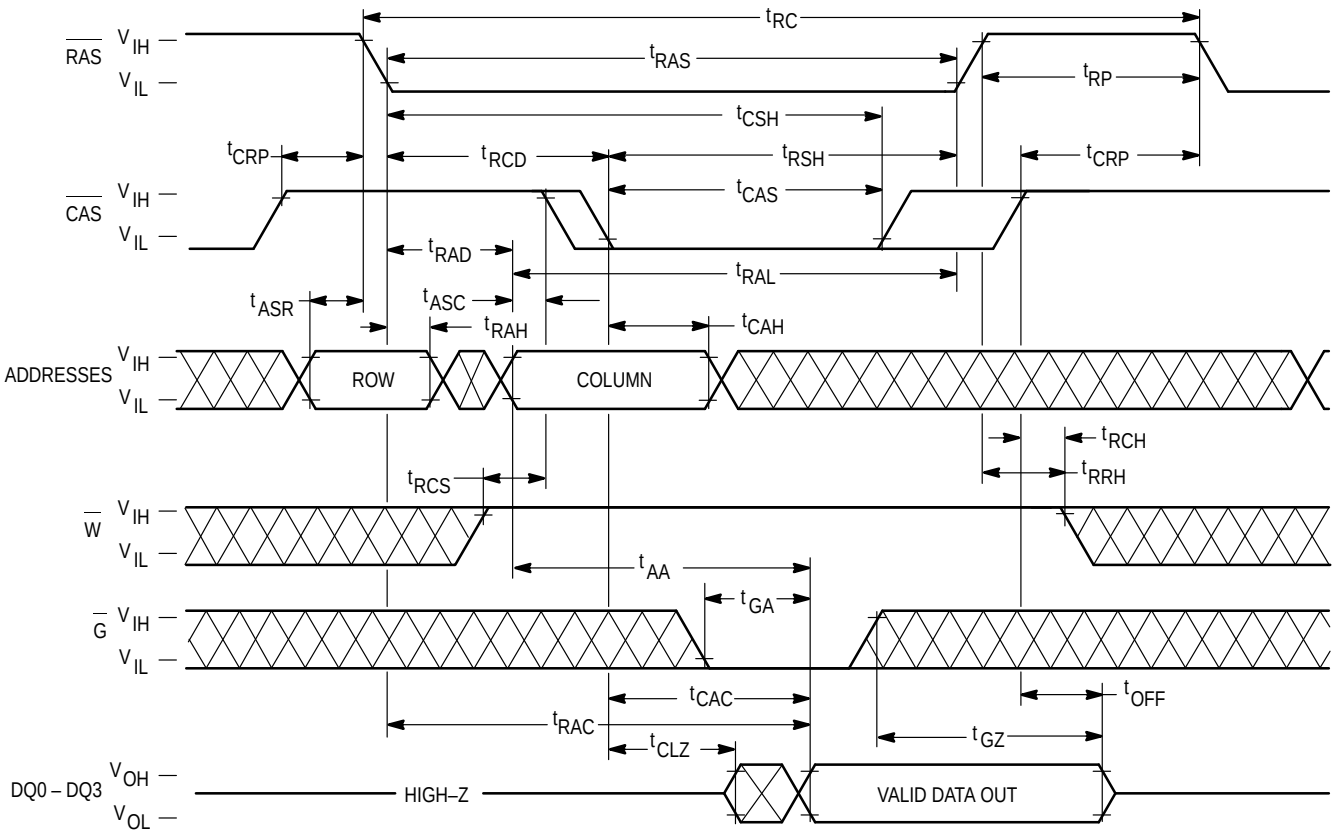


Figure 1. Read Cycle

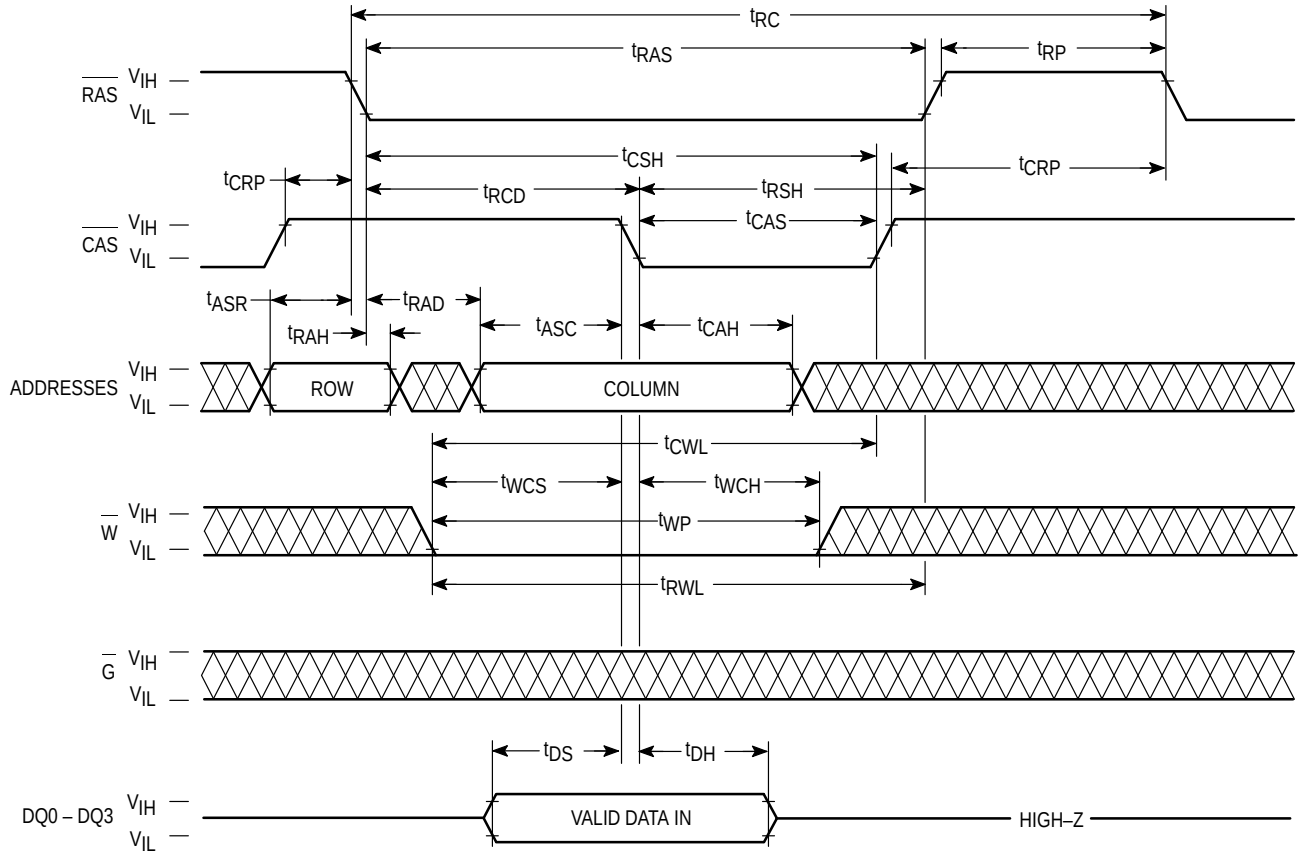


Figure 2. Early Write Cycle

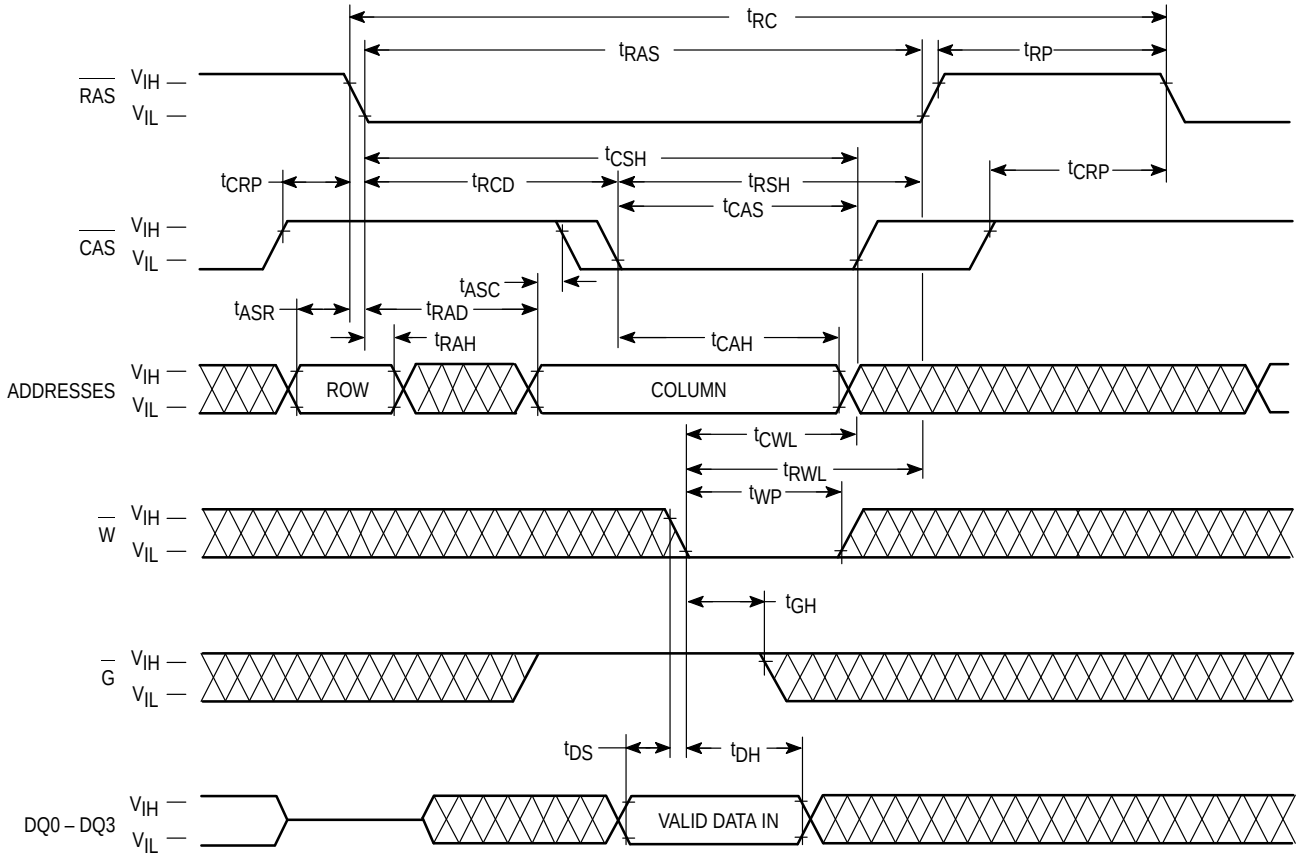


Figure 3. $\overline{G}$ Controlled Late Write Cycle

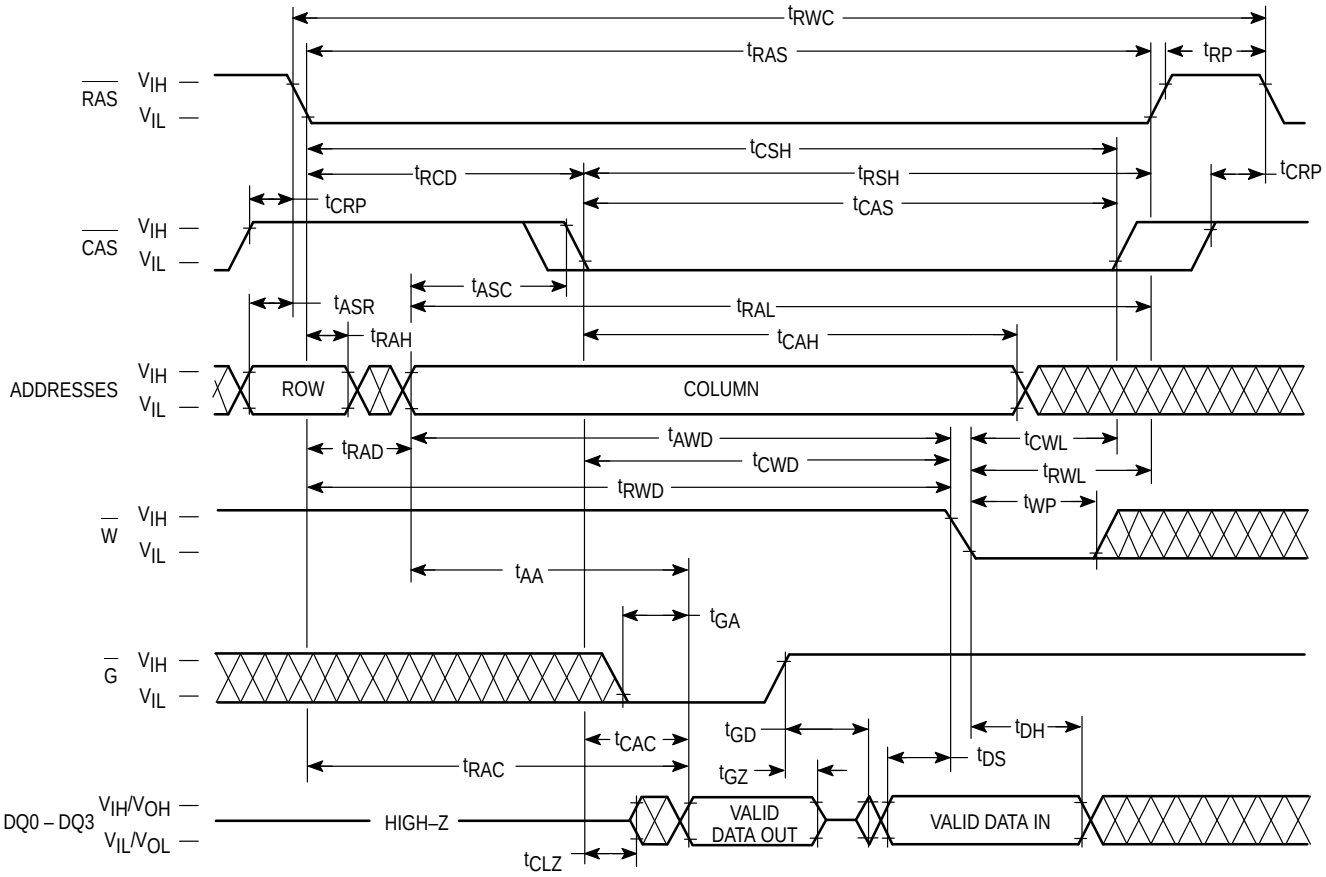


Figure 4. Read–Write Cycle

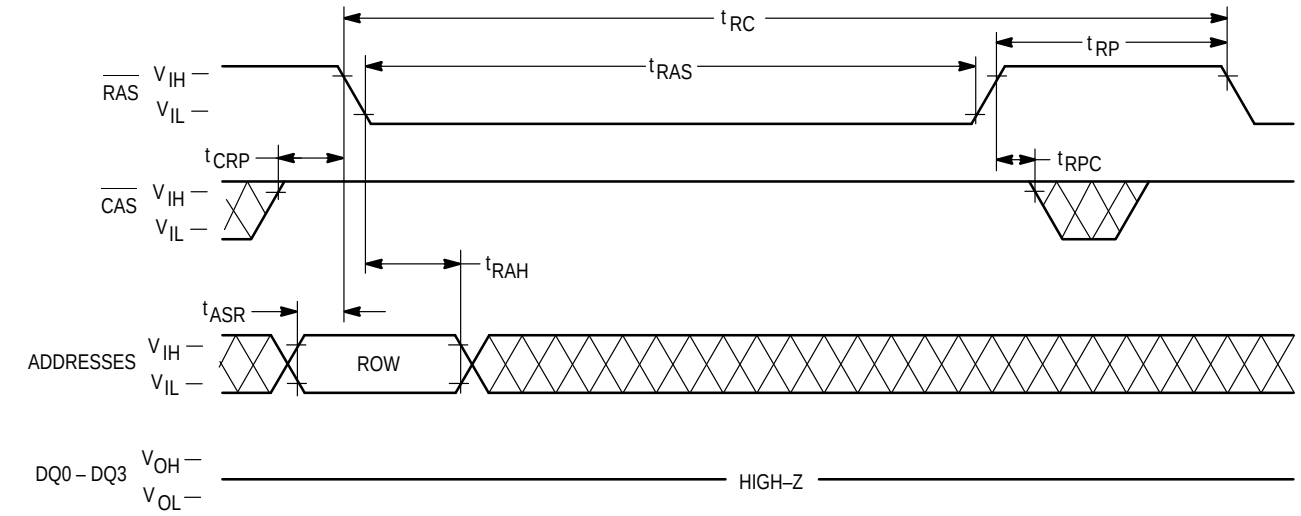


Figure 5. RAS Only Refresh Cycle
(W and G are Don't Care)

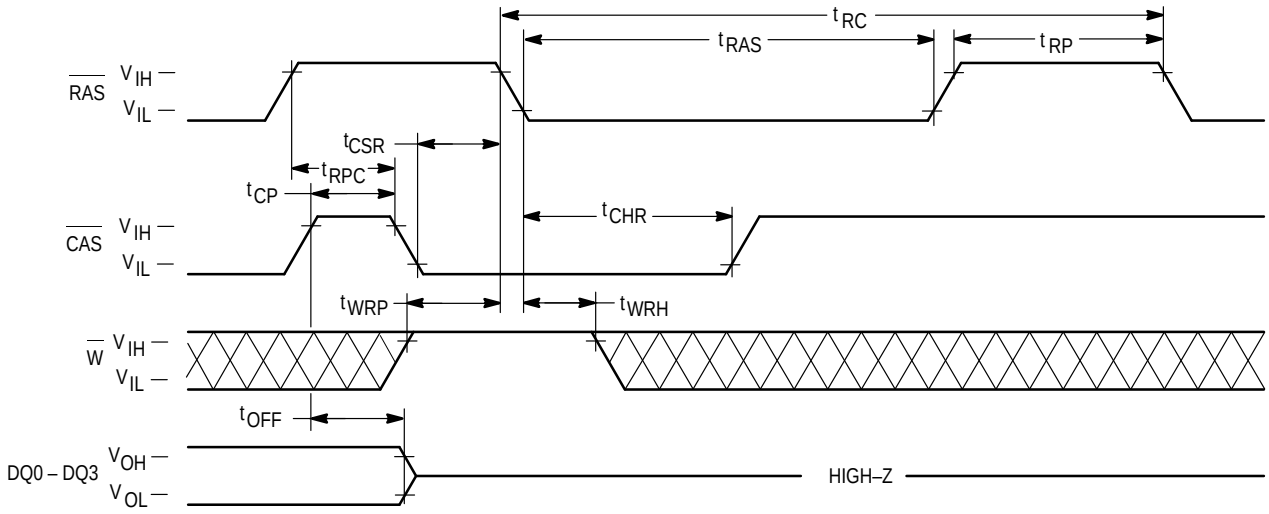


Figure 6. $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle
(G and A0 – A10 are Don't Care)

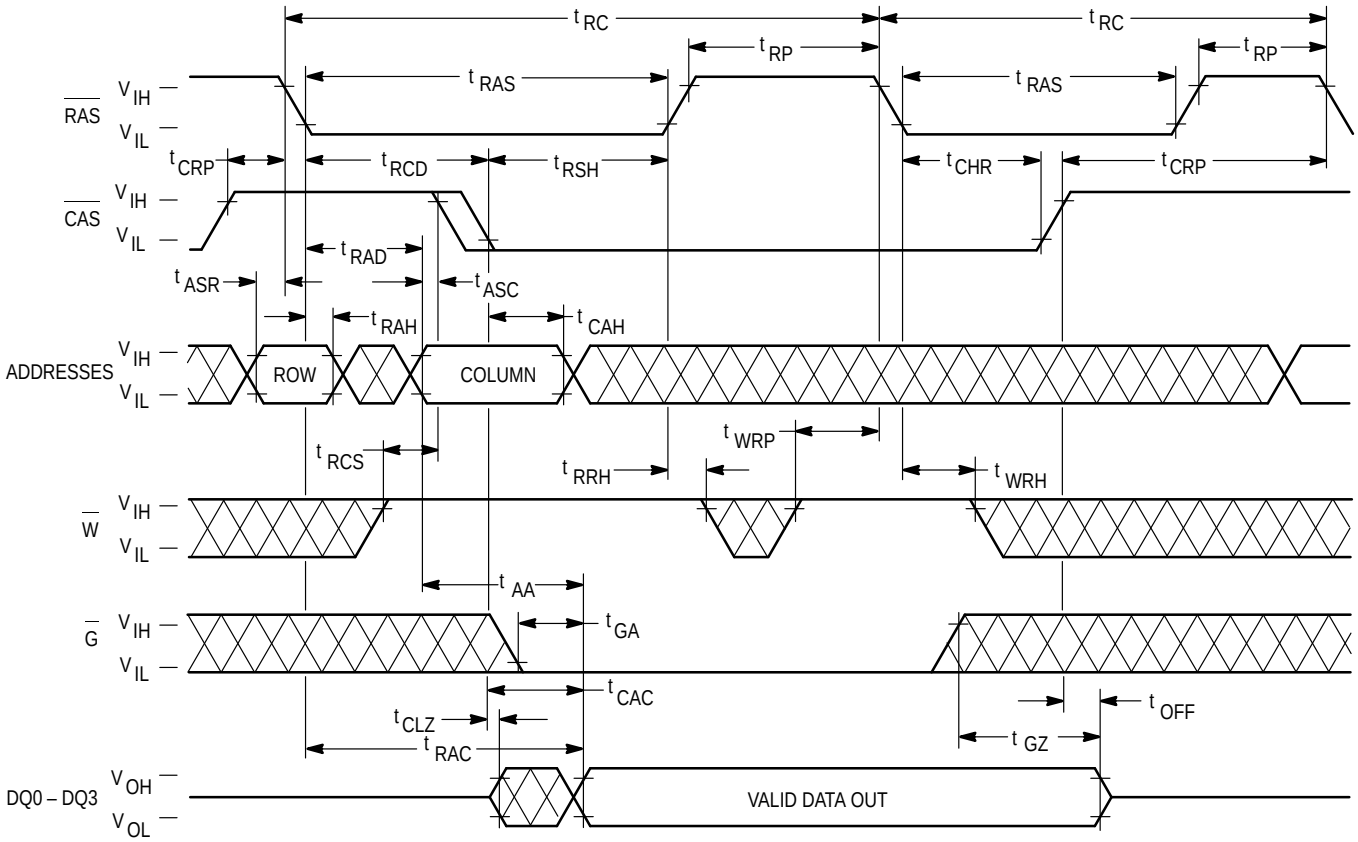


Figure 7. Hidden Refresh Cycle

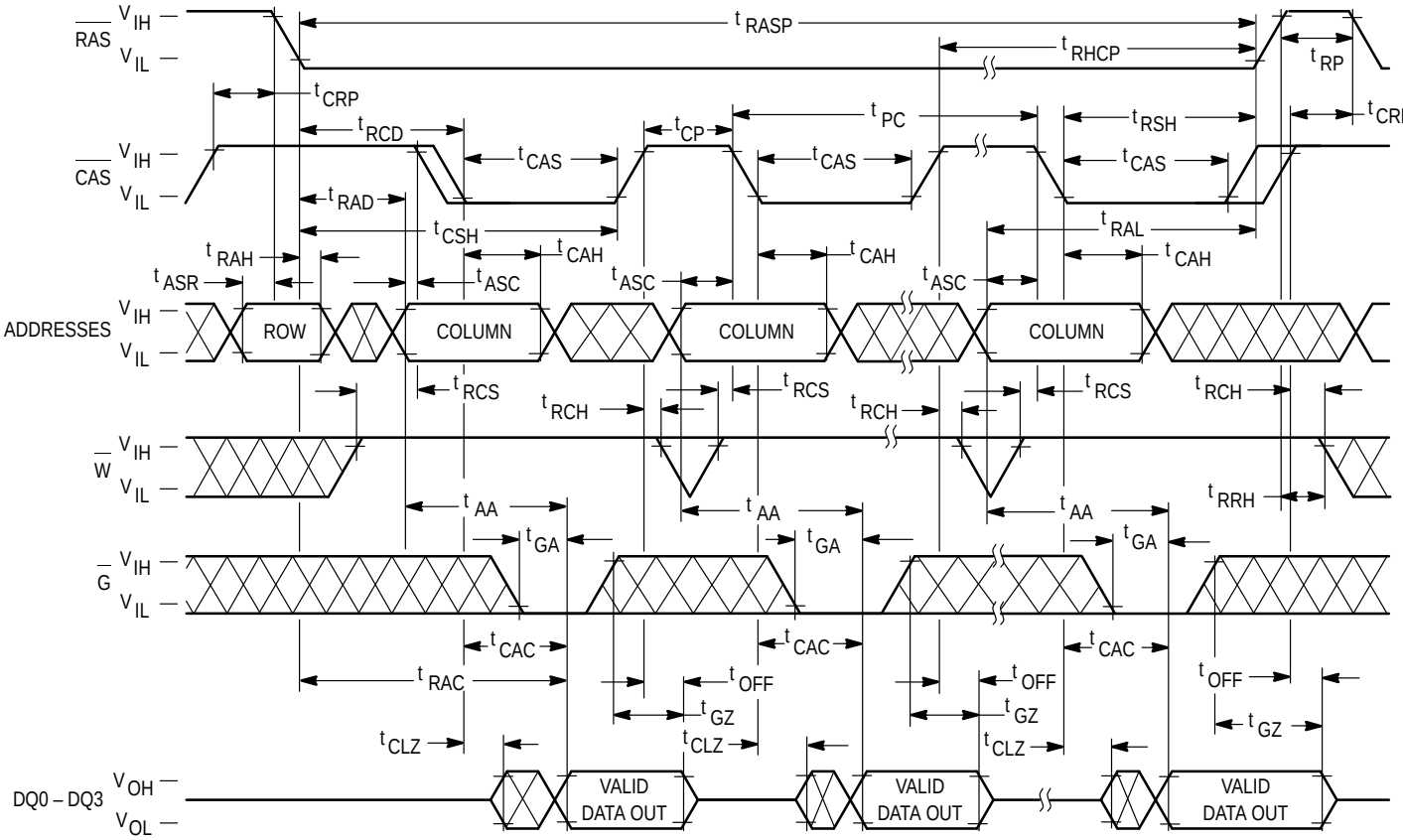


Figure 8. Fast Page Mode Read Cycle

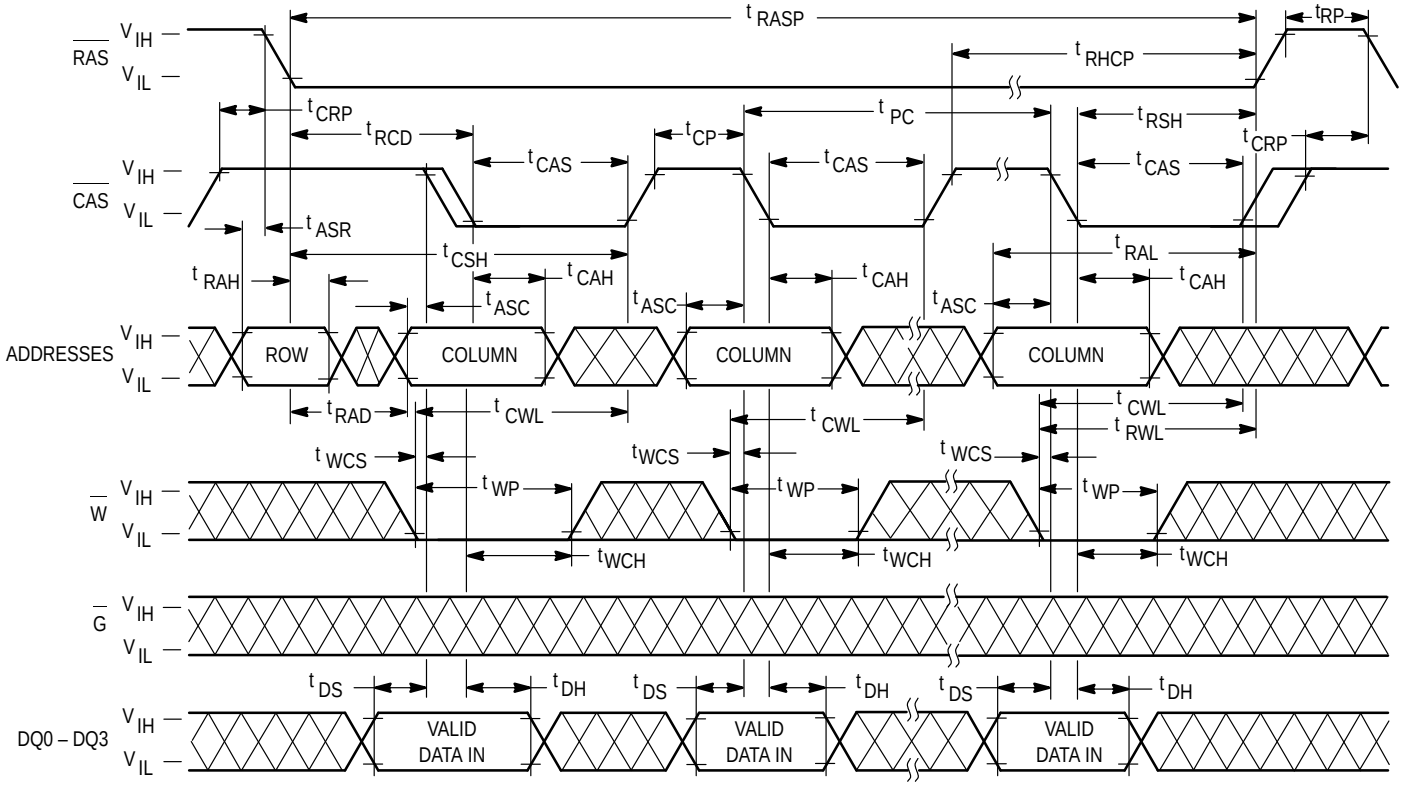


Figure 9. Fast Page Mode Early Write Cycle

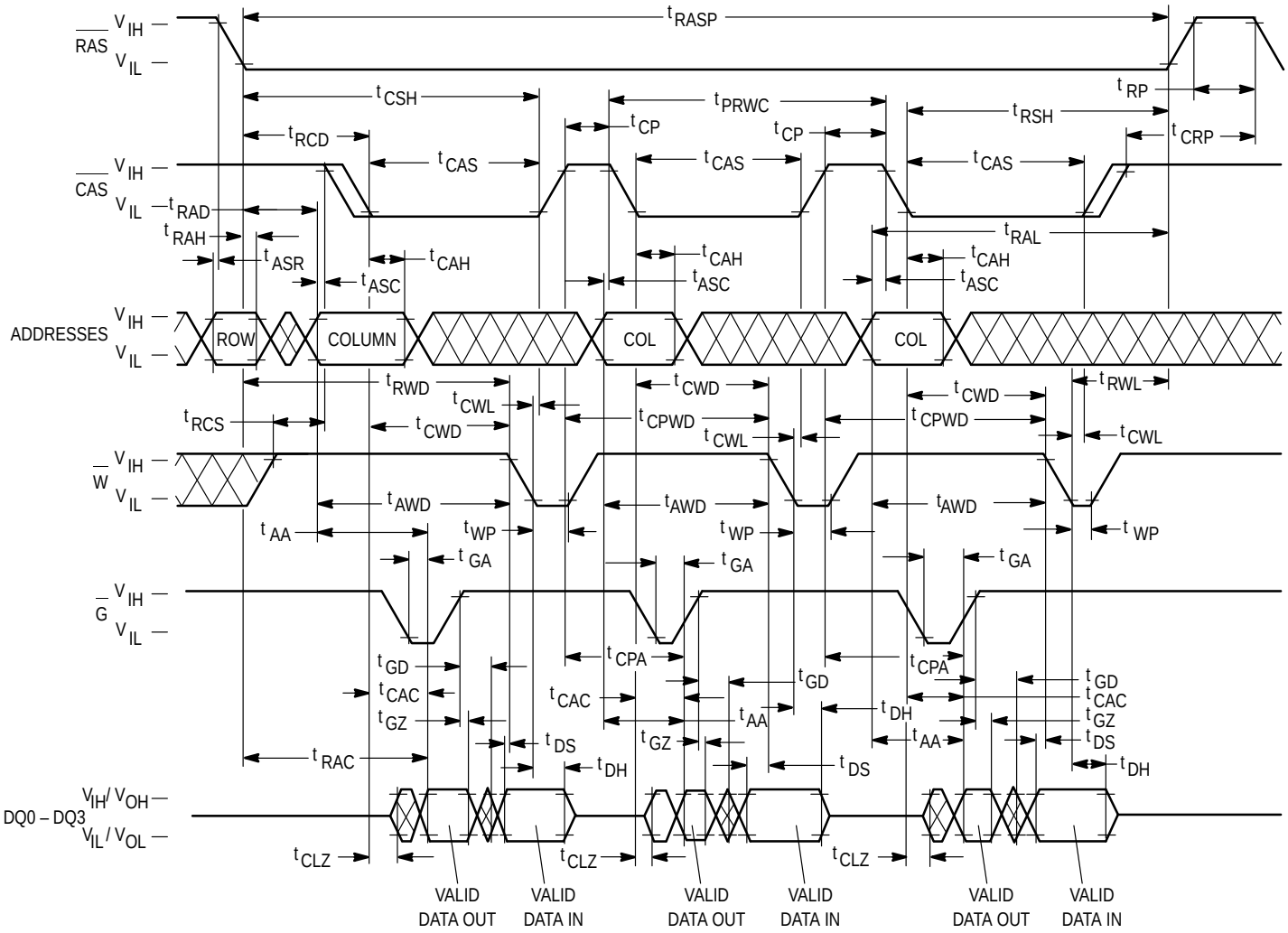


Figure 10. Fast Page Mode Read–Write Cycle

TEST MODE TIMING DIAGRAMS

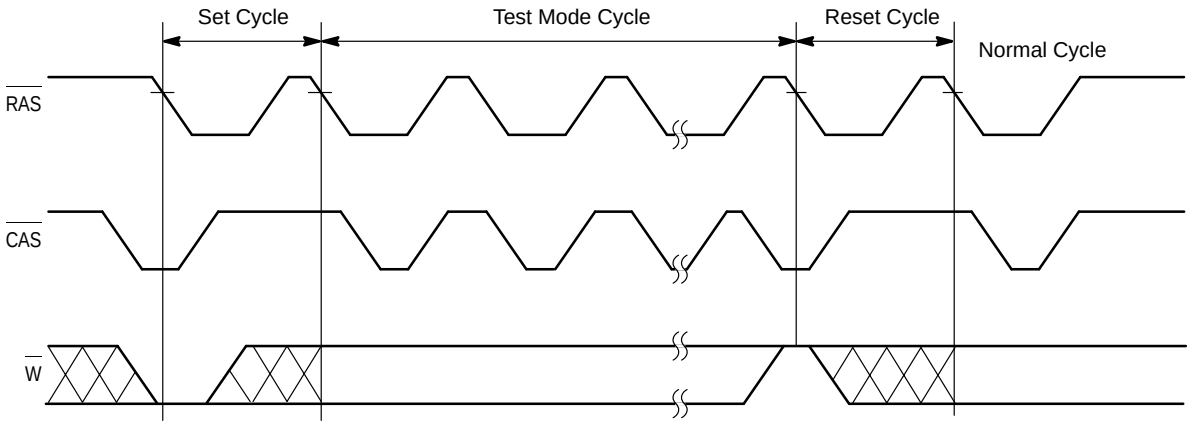


Figure 11. Test Mode Cycle

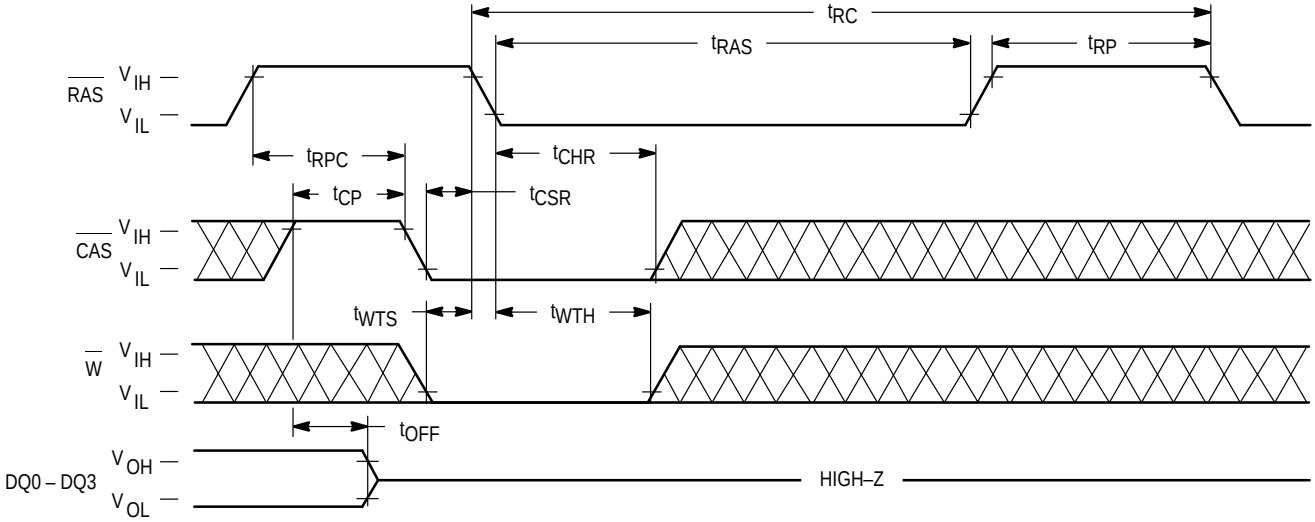


Figure 12. WRITE or CAS Before RAS Refresh Cycle (Test Mode Entry)
(G and A0 – A10 are Don't Care)

NOTE: Once the device is put into Test Mode with the Test Mode Entry Cycle, any of the standard cycles (Read or Write) may be used to test the part, providing that the timing parameters are modified as described in the Test Mode AC Operating Conditions and Characteristics table. The timing diagrams previously presented are valid for all cycles performed in Test Mode.

MODE DEPENDENT ON CAS AND W WHEN RAS FALLS

Mode	CAS	W*
CBR Refresh, Test Mode Exit	0	1
Test Mode Entry	0	0

*Logic state when RAS transitions low.

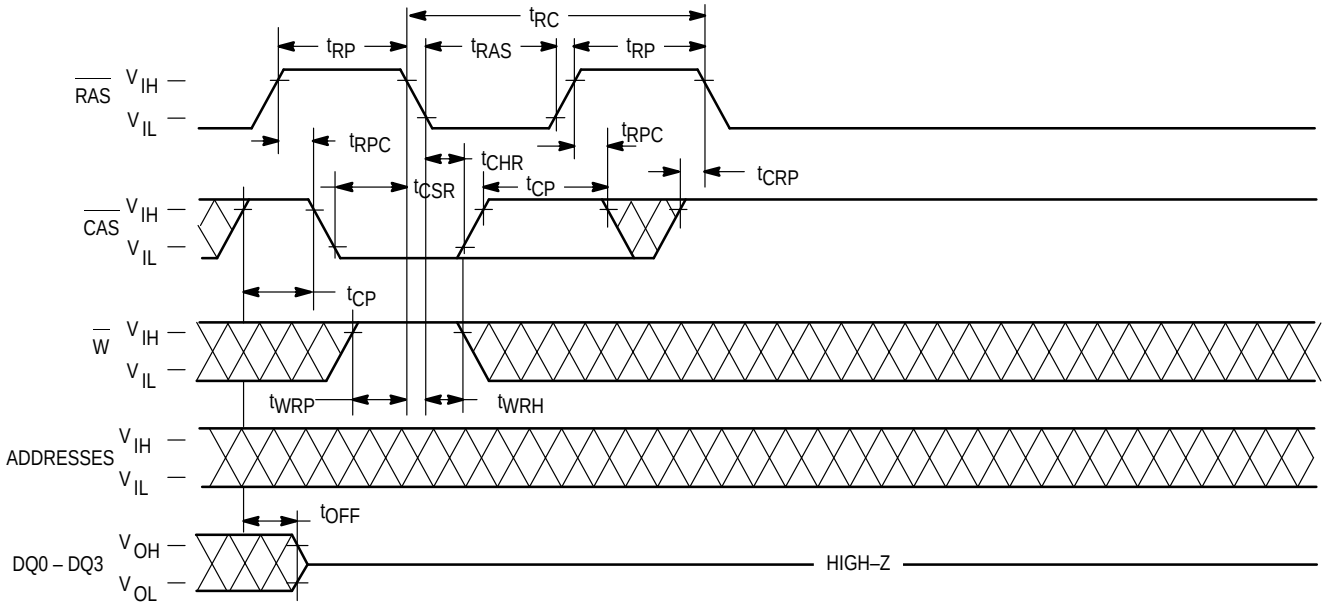


Figure 13. Test Mode Reset Cycle

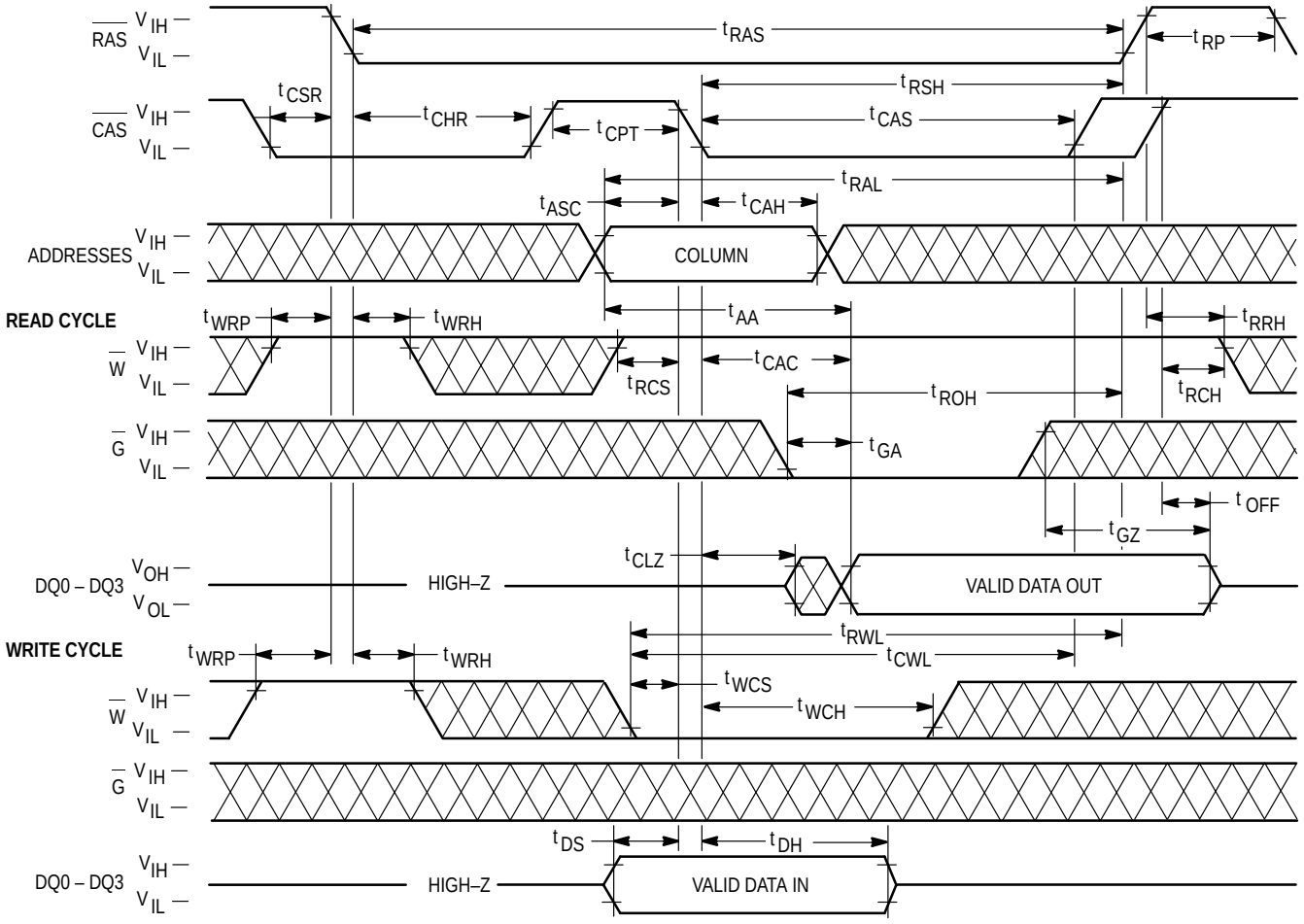


Figure 14. $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Counter Test Cycle

DEVICE INITIALIZATION

On power–up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 32 milliseconds), a wakeup sequence of eight active cycles is necessary to ensure proper operation. If the internal refresh counter is used, a minimum of eight CAS before RAS refresh cycles are required.

ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe (RAS) and column address strobe (CAS), into two separate 11–bit address fields. A total of twenty two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 four bit word locations in the device. RAS active transition is followed by CAS active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between RAS and CAS active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external CAS signal is ignored until an internal RAS signal is available. This "gate" feature on the external CAS clock enables the internal CAS line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the CAS clock.

There are three other variations in addressing the 16M DRAM Family per device: RAS–only refresh cycle, CAS before RAS refresh cycle, and page mode. All are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, fast page mode read cycle, read–write cycle, and fast page mode read–write cycle. The normal read cycle is outlined here,while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with RAS and CAS active transitions latching the desired bit location. The write (W) input level must be high (V_{IH}), t_{RCS} (minimum) before the CAS or active transition, to enable read mode.

Both the RAS and CAS clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window.

For both CAS and output enable ($\overline{G}$) control read access time: CAS must be active before or at t_{RCD} maximum and G must be active t_{RAC}–t_{GA} (both minimum) after RAS active transition to guarantee valid data out (Q) at t_{RAC}. If the t_{RCD} maximum is exceeded and/or G active transition does not occur in time, read access time is determined by either the CAS or G clock active transition (t_{CAC} or t_{GA}).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, fast page mode early write, and fast page mode read–write. Early and late write modes are discussed here, while fast page mode write operation is covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of W to active (V_{IL}). Early and late write modes are distinguished by the active transition of W, with respect to CAS. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP}, apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before CAS active transition. Column address setup and hold times (t_{ASC}, t_{CAH}) and data in (D) setup and hold times (t_{DS}, t_{DH}) are referenced to CAS in an early write cycle. RAS and CAS clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three–state condition throughout an early write cycle because W active transition precedes or coincides with CAS active transition, keeping data–out buffers disabled. (G also is disabled).

A late–write cycle (referred to as $\overline{G}$–controlled write occurs when W active transition is made after CAS active transition. W active transition could be delayed for almost 10 ms after CAS active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T$) ≤ t_{RAS}, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) aremaintained. D timing parameters are referenced to W active transition in a late write cycle. Output buffers are enabled by CAS active transition. 4M x 4 outputs are switched off by G inactive transition, which is required to write to the device. Q may be indeterminate (see note 19 of AC Operating Conditions table). RAS and CAS must remain active for t_{RWL} and t_{CWL}, respectively, after W active transition to complete the write cycle. G must remain inactive for t_{GH} after W active transition to complete the write cycle.

READ–WRITE CYCLE

A read–write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except W must remain high for t_{CWD} and/or t_{AWD} minimum, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all column locations (MCM417400: 2048 columns) on a selected row of the 16M DRAM family. Read access time in page mode (t_{CAC}) is typically half the regular RAS clock access time, t_{RAC}. Page mode operation consists of keeping RAS active while toggling CAS between V_{IH} and V_{IL}. The row is latched by RAS active transition, while each CAS active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read–write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, CAS transitions to inactive for minimum t_{CP}, while RAS remains low (V_{IL}). The second CAS active transition while RAS is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read–write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when RAS

transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM417400 require refresh every 32 milliseconds.

This is accomplished by cycling through the 2048 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the 16M DRAM device family. Burst refresh, a refresh of all rows consecutively, must be performed every 32 milliseconds on the MCM417400.

A normal read, write, or read–write operation to the RAM will refresh all the bits (2048) associated with the particular row decodes. Three other methods of refresh, **RAS–only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{RAS}$–Only Refresh

$\overline{RAS}$–only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter should be employed to ensure that all rows are refreshed within the specified limit.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CAS}$ active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{W}$ must be inactive for time t_{WRP} before and time t_{WRH} after RAS active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle while RAS cycles inactive for t_{RP} and back to active starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 7). $\overline{W}$ is subject to the same conditions with respect to RAS active transition (to prevent test mode entry) as in CAS before RAS refresh.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This test is performed with a read–write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 2048 cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram (Figure 14).

The test can be performed after a minimum of eight **CAS before RAS** initialization cycles. Test procedure:

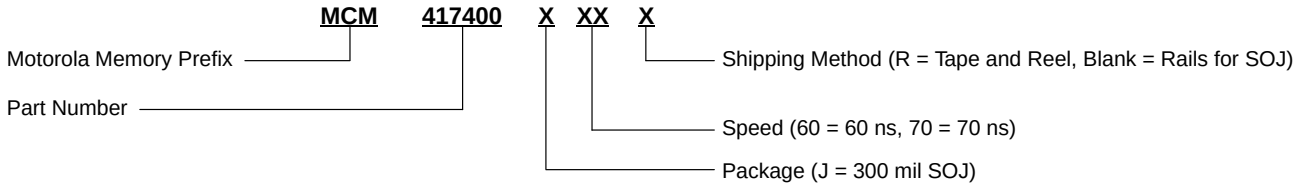
1. Write 0s into all memory cells with normal write mode.
2. Select a column address, read 0 out and write 1 into the cell by performing the **CAS before RAS refresh counter test, read–write cycle**. Repeat this operation 2048 times, depending on device type.
3. Read the 1s that were written in step two in normal read mode.
4. Using the same starting column address as in step two, read 1 out and write 0 into the cell by performing the **CAS before RAS refresh counter test, read–write cycle**. Repeat this operation 2048 times, depending on device type.
5. Read 0s which were written in step four in normal read mode.
6. Repeat steps one through five using complement data.

TEST MODE

The internal organization of the MCM417400 allows the device to be tested as if it were a 1M x 16 DRAM. In **Test Mode** operation, column addresses A1 and A0 are ignored. A test mode cycle reads and/or writes data to a bit in each of the sixteen 1M blocks in parallel. During a write cycle, data is written using all four I/O pins, during a read cycle, if all 16 bits are equal (all 0s or all 1s), all four I/O pins will indicate a 1. Otherwise, they will indicate a 0. See Test Mode block diagram.

W, CAS before RAS timing puts the device in **Test Mode**, as shown in the test mode timing diagram (Figure 12). Refresh is performed in test mode by using a **W, CAS before RAS** refresh cycle which uses the internal refresh address counter, or normal read cycles. To get out of test mode and enter normal operation, perform either a CAS before RAS refresh or RAS only refresh cycle.

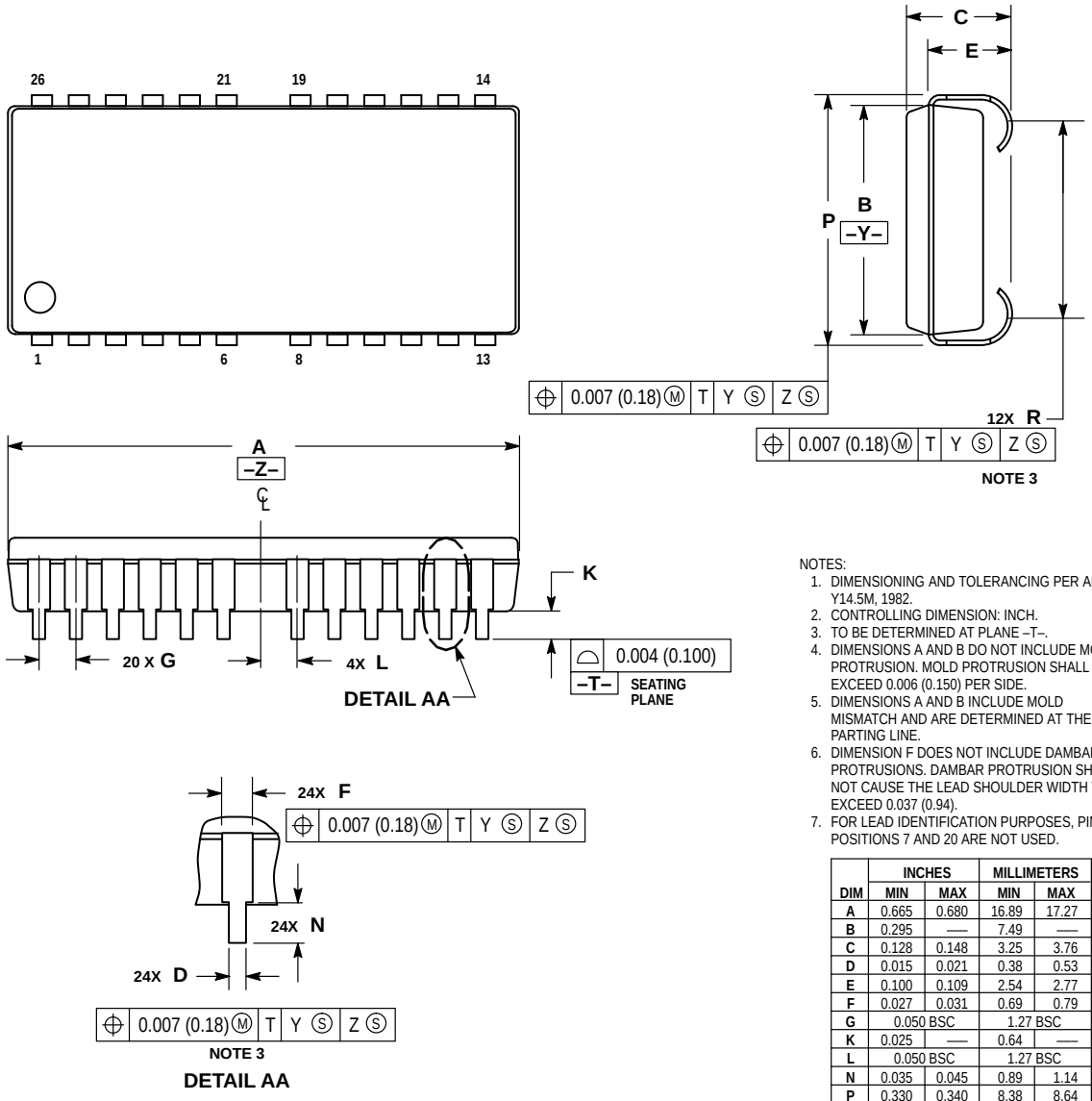
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers – MCM417400J60 MCM417400J60R
MCM417400J70 MCM417400J70R

PACKAGE DIMENSIONS

J PACKAGE
300 MIL SOJ
CASE 880B–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TO BE DETERMINED AT PLANE –T–.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.006 (0.150) PER SIDE.
5. DIMENSIONS A AND B INCLUDE MOLD MISMATCH AND ARE DETERMINED AT THE PARTING LINE.
6. DIMENSION F DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD SHOULDER WIDTH TO EXCEED 0.037 (0.94).
7. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 7 AND 20 ARE NOT USED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.665	0.680	16.89	17.27
B	0.295	—	7.49	—
C	0.128	0.148	3.25	3.76
D	0.015	0.021	0.38	0.53
E	0.100	0.109	2.54	2.77
F	0.027	0.031	0.69	0.79
G	0.050 BSC		1.27 BSC	
K	0.025	—	0.64	—
L	0.050 BSC		1.27 BSC	
N	0.035	0.045	0.89	1.14
P	0.330	0.340	8.38	8.64
R	0.260	0.274	6.60	6.96

How to reach us:
USA / EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298