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TECHNICAL DATA

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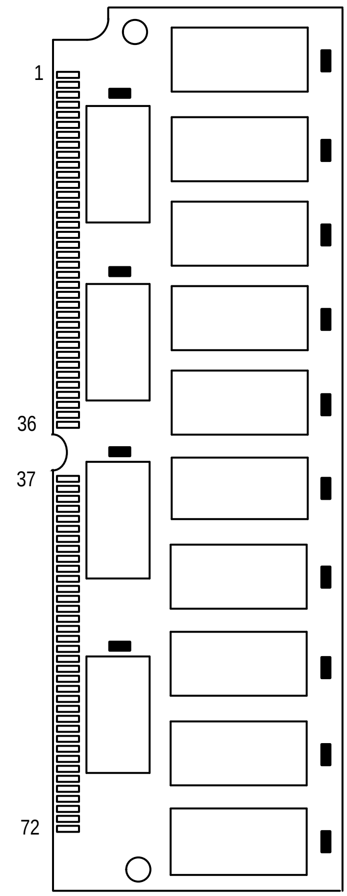
MCM36800

8M x 36 Bit Dynamic Random Access Memory Module

AS PACKAGE
SIMM MODULE
CASE 866J–01
TOP VIEW



The MCM36800 is a dynamic random access memory (DRAM) module organized as 8,388,608 x 36 bits. The module is a 72–lead single–in–line memory module (SIMM) consisting of sixteen MCM517400B DRAMs, housed in 300 mil J–lead small outline packages (SOJ), and eight MCM54100AN DRAMs housed in 300 mil J–lead small outline packages (SOJ), mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted adjacent to each DRAM. The MCM517400B is a CMOS high–speed dynamic random access memory organized as 4,194,304 four–bit words and fabricated with CMOS silicon–gate process technology.

- Three–State Data Output
- Early–Write Common I/O Capability
- Fast Page Mode Capability
- TTL–Compatible Inputs and Outputs
- RAS–Only Refresh
- CAS Before RAS Refresh
- Hidden Refresh
- 2048 Cycle Refresh: 32 ms
- Consists of Sixteen 4M x 4 DRAMs, Eight 4M x 1 DRAMs, and Twenty–Four 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM36800–60 = 60 ns (Max)
  MCM36800–70 = 70 ns (Max)
- Low Active Power Dissipation: MCM36800–60 = 7.61 W (Max)
  MCM36800–70 = 6.51 W (Max)
- Low Standby Power Dissipation: TTL Levels = 264 mW (Max)
  CMOS Levels = 132 mW (Max)

PIN ASSIGNMENTS

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ24	37	DQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	DQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	CAS0	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	CAS2	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	CAS3	54	DQ29	66	NC
7	DQ20	19	A10	31	A8	43	CAS1	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	RAS0	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	RAS3	45	RAS1	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	RAS2	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	DQ26	47	W	59	V_{CC}	71	NC
12	A0	24	DQ6	36	DQ8	48	NC	60	DQ32	72	V_{SS}

PIN NAMES

A0 – A10	Address Inputs
DQ0 – DQ35	Data Input/Output
CAS0 – CAS3	Column Address Strobe
PD1 – PD4	Presence Detect
RAS0 – RAS3	Row Address Strobe
W	Read/Write Input
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

REV 2
10/95

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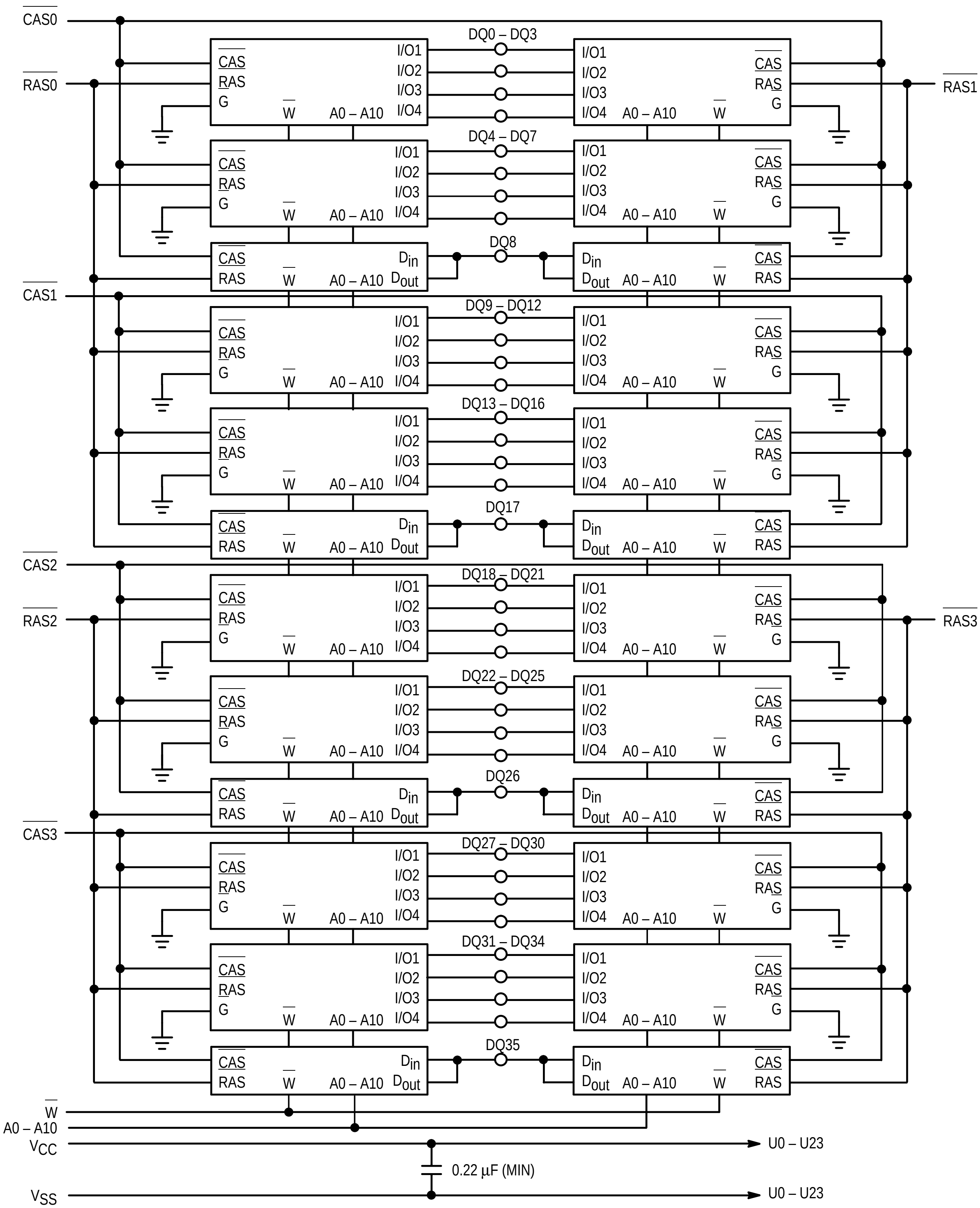
BLOCK DIAGRAM



PRESENCE DETECT PIN OUT		
Pin Name	**60 ns**	**70 ns**
PD1	NC	NC
PD2	V_{SS}	V_{SS}
PD3	NC	V_{SS}
PD4	NC	NC

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 1 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 1 to + 7	V
Data Output Current	I_{out}	50	mA
Power Dissipation	P_D	16.8	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	V_{CC} + 0.5 V	V
Logic Low Voltage, All Inputs	V_{IL}	– 0.5*	—	0.8	V

* – 2.0 V at pulse width ≤ 20 ns.

DC CHARACTERISTICS AND SUPPLY CURRENTS (All voltages referenced to V_{SS})

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM36800–60, t_{RC} = 110 ns MCM36800–70, t_{RC} = 130 ns	I_{CC1}	— —	1384 1184	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}	—	48	mA	
V_{CC} Power Supply Current During $\overline{RAS}$–Only Refresh Cycles ($\overline{CAS}$ = V_{IH}) MCM36800–60, t_{RC} = 110 ns MCM36800–70, t_{RC} = 130 ns	I_{CC3}	 — —	 1384 1184	mA	1, 2
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL})	$I_{CC4(P)}$	—	744	mA	1, 2
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.2 V)	I_{CC5}	—	24	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle MCM36800–60, t_{RC} = 110 ns MCM36800–70, t_{RC} = 130 ns	I_{CC6}	 — —	 1384 1184	mA	1
Input Leakage Current (0 V ≤ V_{in} ≤ V_{CC})	$I_{lkg(I)}$	– 240	240	µA	
Output Leakage Current (0 V ≤ V_{out} ≤ V_{CC}, Output Disable)	$I_{lkg(O)}$	– 20	20	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:
1. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
2. Address may be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less during t_{PC}.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic	Symbol	Max	Unit
Input Capacitance A0 – A10 $\overline{W}$ $\overline{RAS0}$ – $\overline{RAS3}$, $\overline{CAS0}$ – $\overline{CAS3}$	C_{in}	130 178 52	pF
I/O Capacitance DQ0 – DQ7, DQ9 – DQ16, DQ18 – DQ25, DQ27 – DQ34 DQ8, DQ17, DQ26, DQ35	$C_{I/O}$	24 34	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM36800–60		MCM36800–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	ns	5
Access Time from RAS	t_{RELQV}	t_{RAC}	—	60	—	70	ns	6, 7
Access Time from CAS	t_{CELQV}	t_{CAC}	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	ns	6, 9
Access Time from Precharge CAS	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	6
CAS to Output in Low–Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	6
Output Buffer and Turn–Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	ns	
RAS Precharge Time	t_{REHREL}	t_{RP}	45	—	50	—	ns	
RAS Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	ns	
RAS Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	ns	
CAS Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	ns	
CAS Precharge to RAS Hold Time	t_{CEHREH}	t_{RHCP}	40	—	40	—	ns	
CAS Pulse Width	t_{CELCEH}	t_{CAS}	20	10 k	20	10 k	ns	
RAS to CAS Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	ns	11
RAS to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	ns	12
CAS to RAS Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	
CAS Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	ns	
Column Address to RAS Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	
Read Command Hold Time Referenced to CAS	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	13
Read Command Hold Time Referenced to RAS	t_{REHWX}	t_{RRH}	0	—	0	—	ns	13
Write Command Hold Time Referenced to CAS	t_{CELWH}	t_{WCH}	10	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	ns	

NOTES: (continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power–up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
8. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

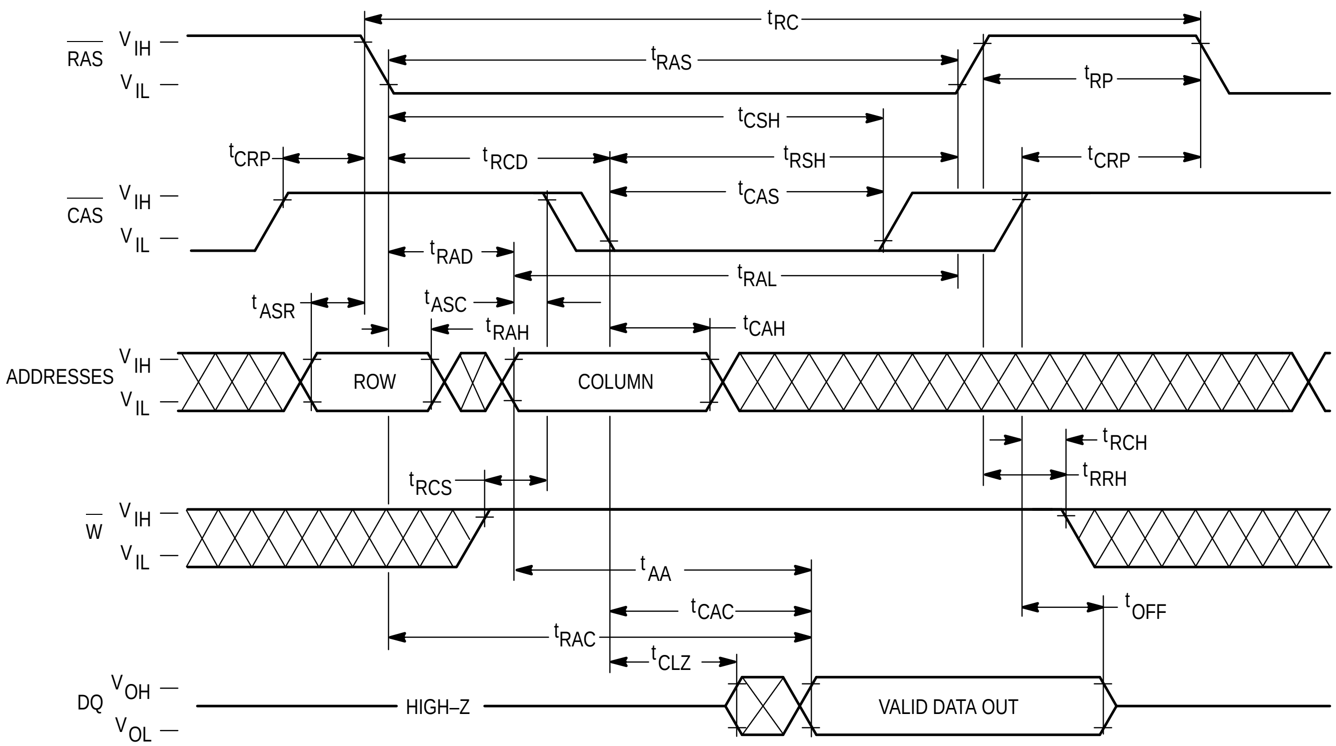
READ AND WRITE CYCLES (Continued)

Parameter	Symbol		MCM36800–60		MCM36800–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Write Command to RAS Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	ns	
Write Command to CAS Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	14
Data In Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	ns	14
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	15
Refresh Period	t_{RVRV}	t_{RFSH}	—	32	—	32	ns	
CAS Setup Time for CAS Before RAS Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	ns	
CAS Hold Time for CAS Before RAS Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	ns	
RAS Precharge to CAS Active Time	t_{REHCEL}	t_{RPC}	5	—	5	—	ns	
CAS Precharge Time for CAS Before RAS Counter Time	t_{CEHCEL}	t_{CPT}	30	—	40	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	ns	
Write to RAS Precharge Time (CAS Before RAS Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	ns	
Write to RAS Hold Time (CAS Before RAS Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	ns	
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	45	—	ns	
CAS Precharge to RAS Hold Time (Fast Page Mode)	t_{CEHREH}	t_{RHCP}	35	—	40	—	ns	
RAS Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	200 k	70	200 k	ns	

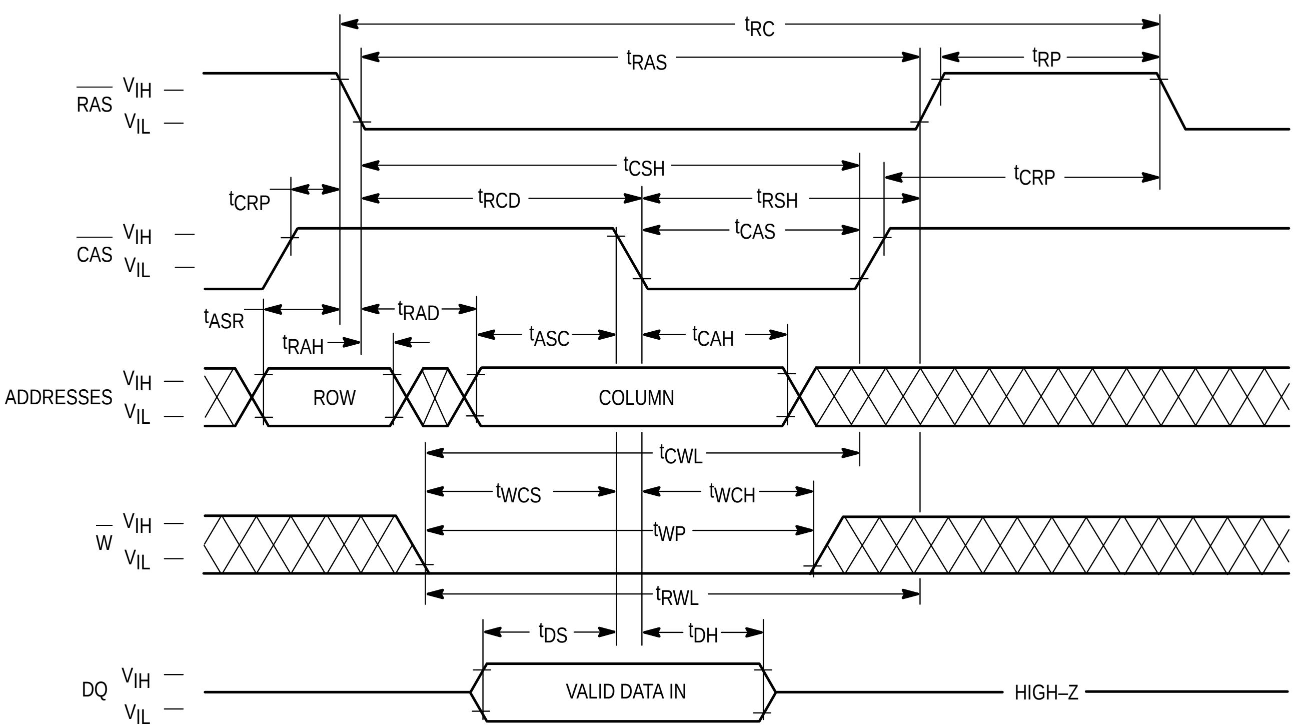
NOTES:

14. These parameters are referenced to CAS leading edge in early write cycles and to W leading edge in late write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisfied, the condition of the data out (at access time) is indeterminate.

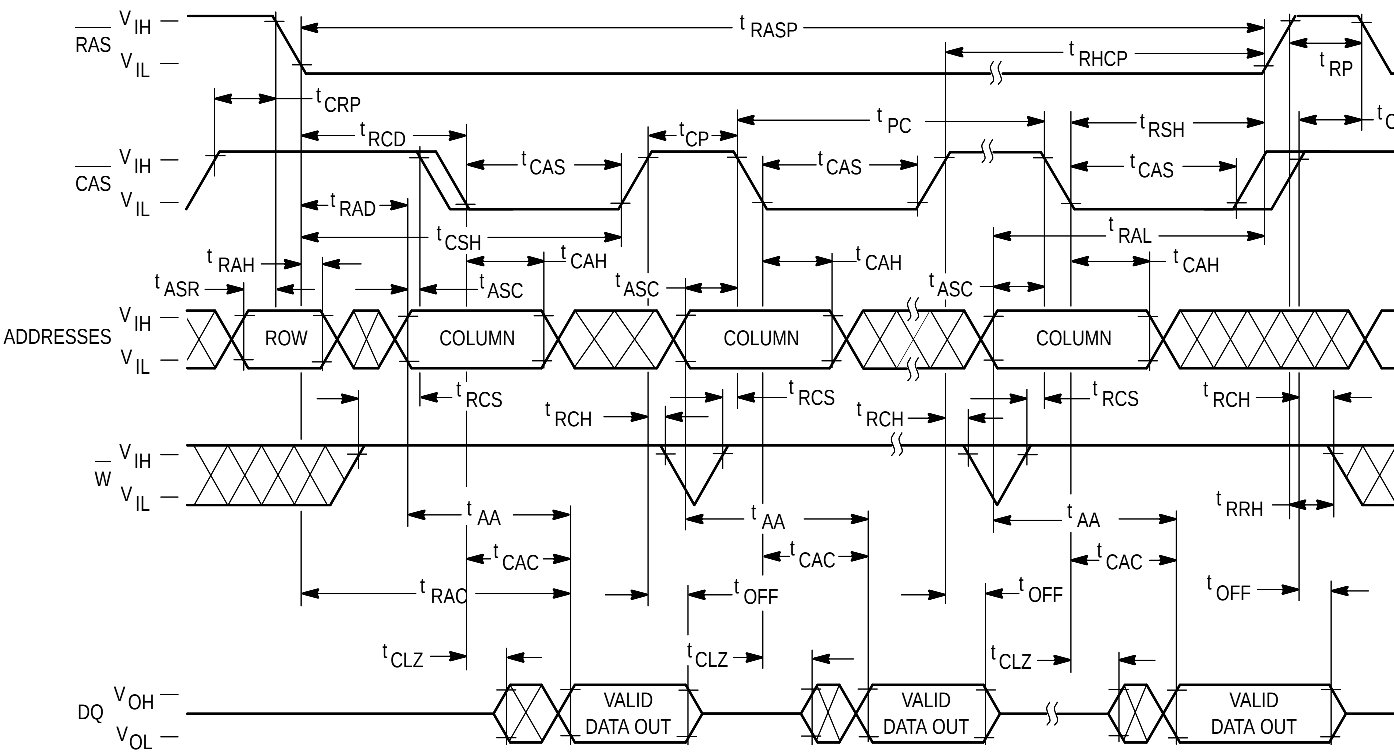
READ CYCLE (FAST PAGE MODE)



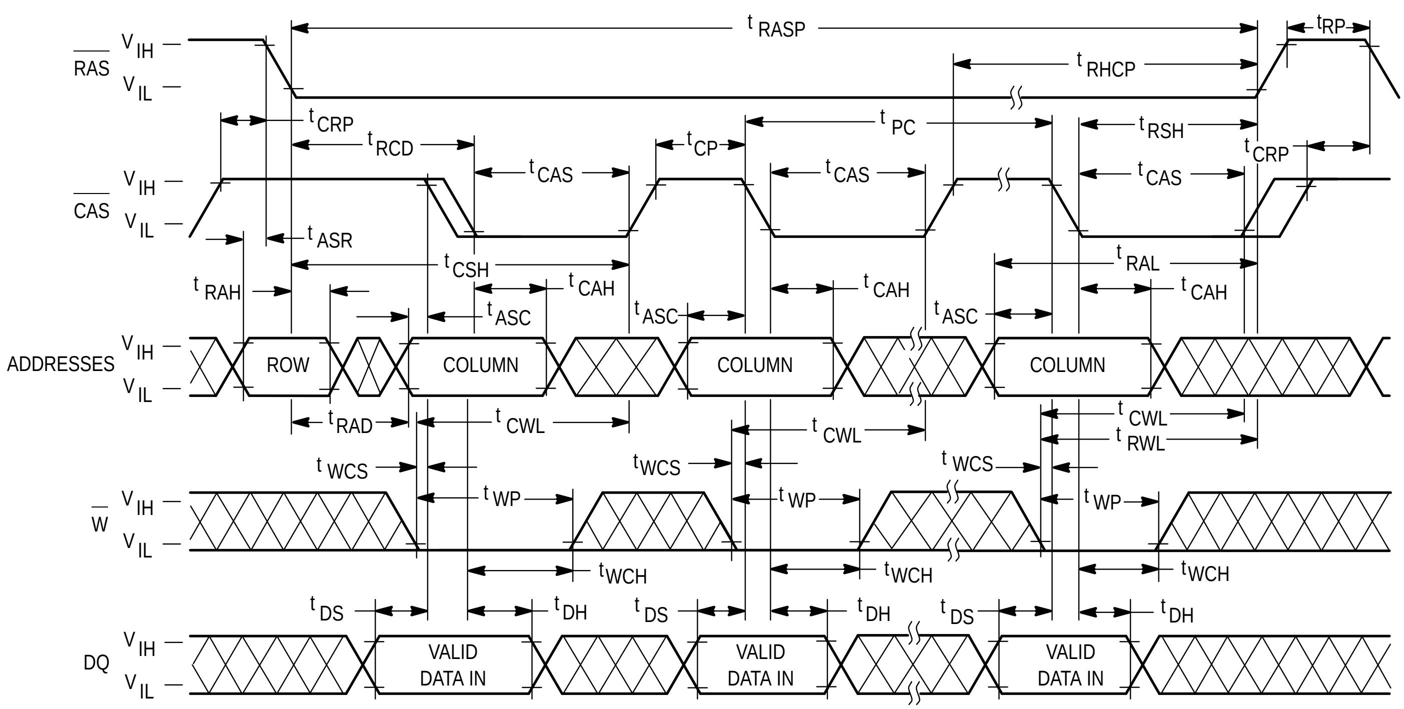
EARLY WRITE CYCLE



FAST PAGE MODE READ CYCLE

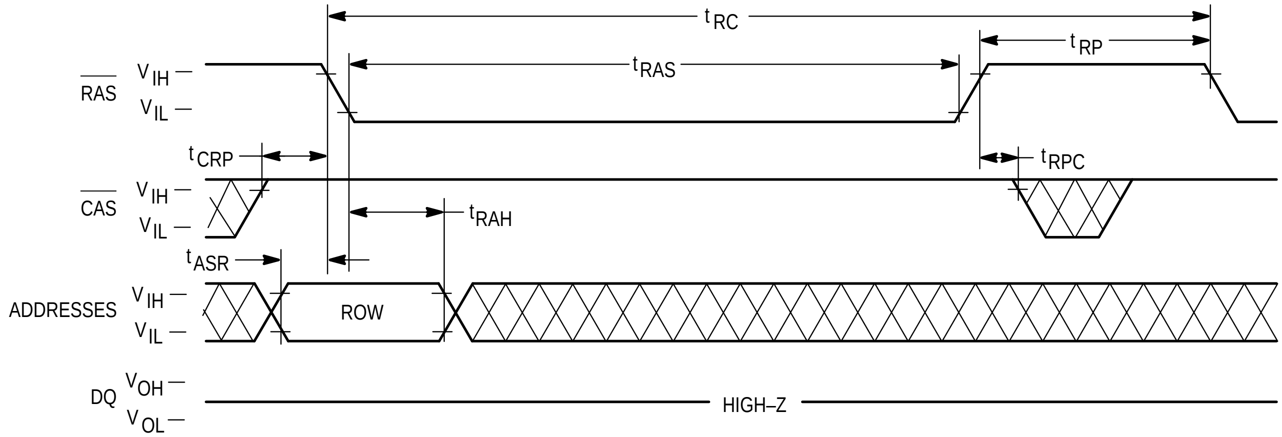


FAST PAGE MODE EARLY WRITE CYCLE



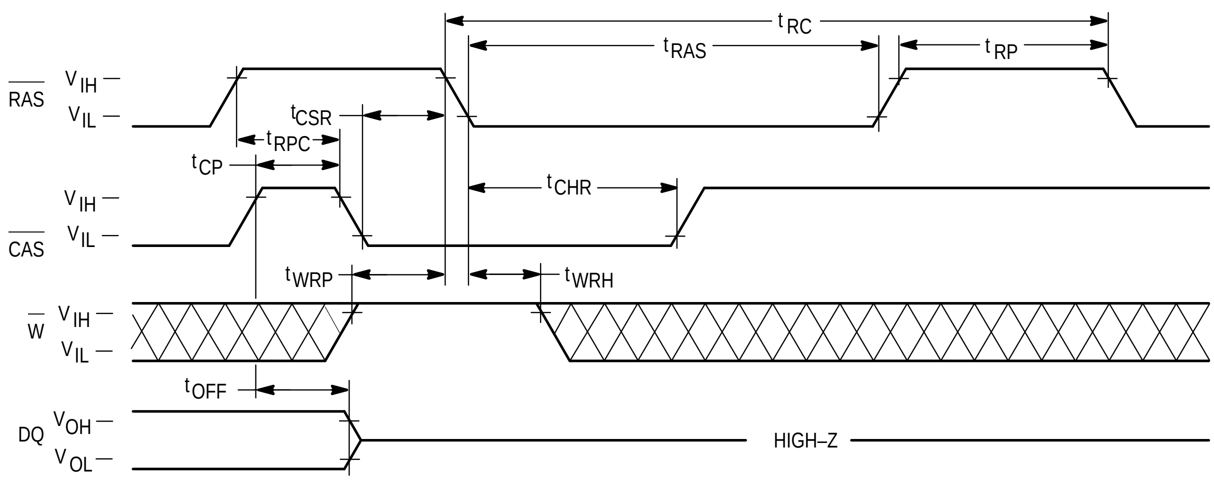
RAS–ONLY REFRESH CYCLE

(W is Don't Care)

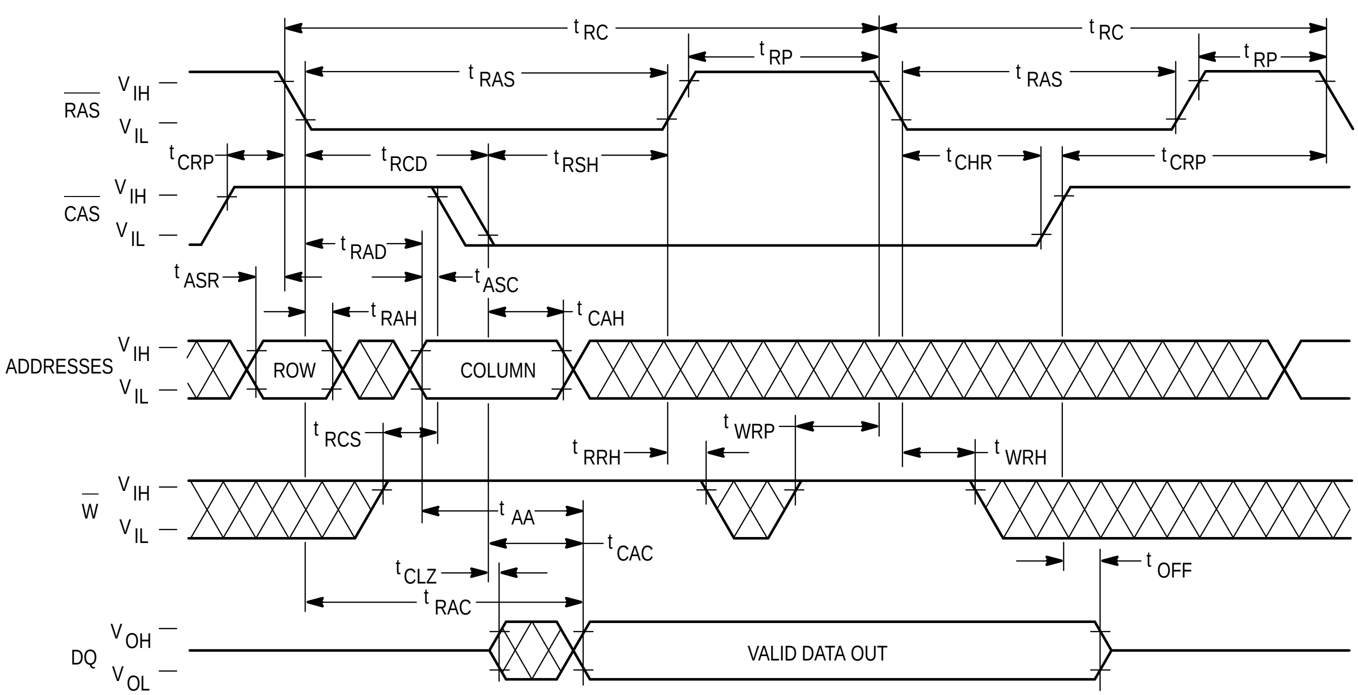


CAS BEFORE RAS REFRESH CYCLE

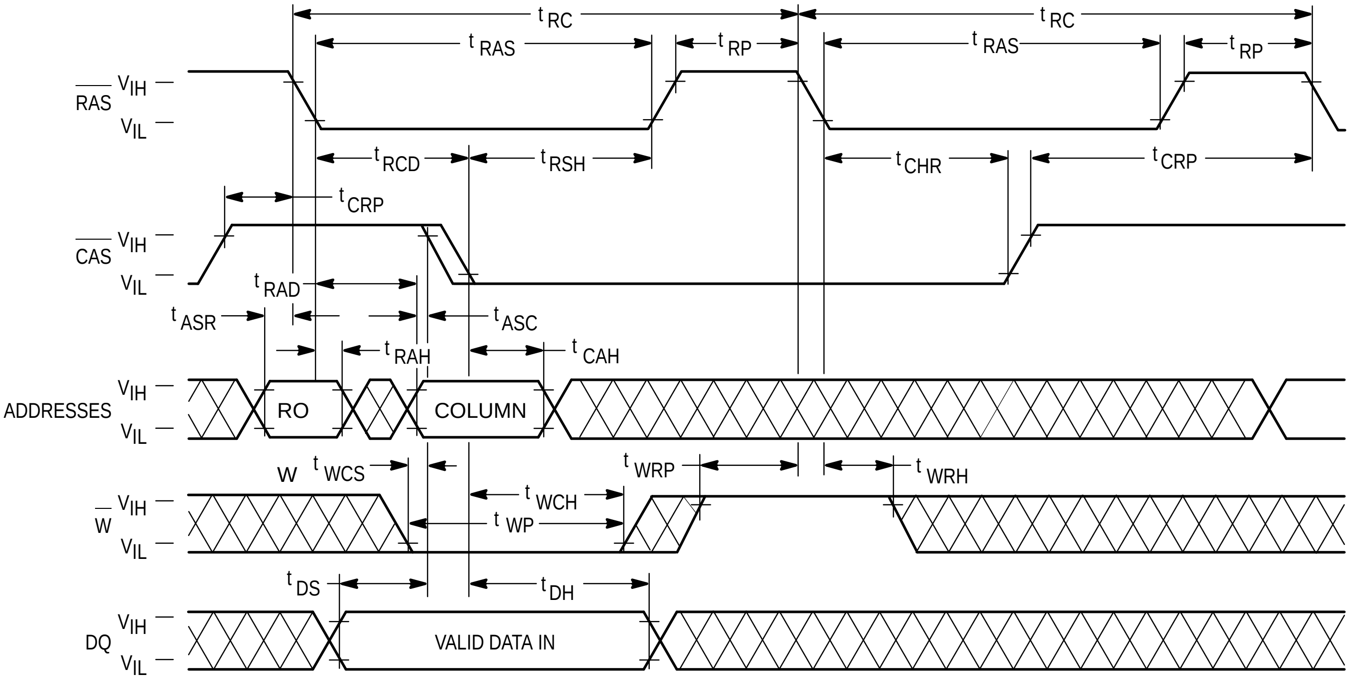
(A0 – A10 are Don't Care)



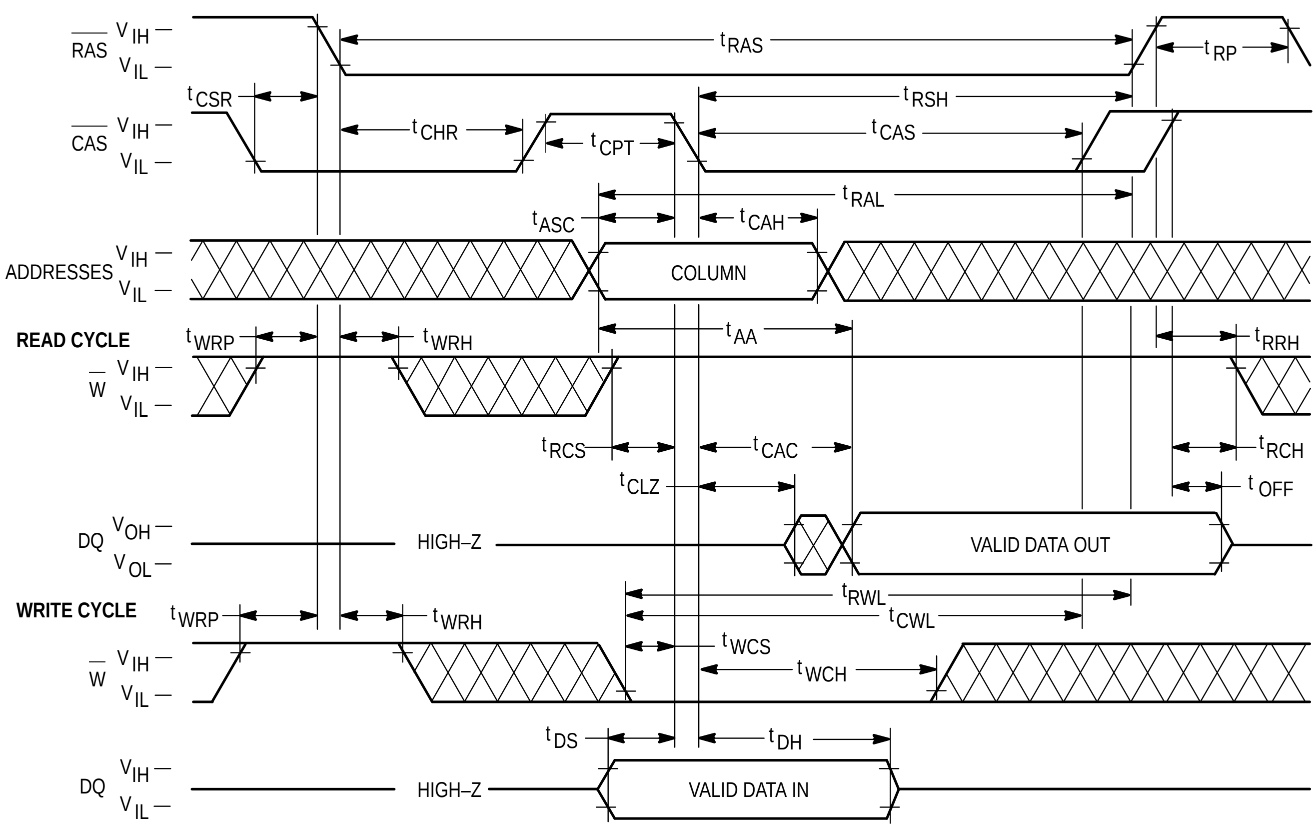
HIDDEN REFRESH CYCLE (READ) (FAST PAGE MODE)



HIDDEN REFRESH CYCLE (EARLY WRITE)



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power–up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe (RAS) and column address strobe (CAS), into two separate 11–bit address fields. A total of twenty two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 word locations in the device. RAS active transition is followed by CAS active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between RAS and CAS active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external CAS signal is ignored until an internal RAS signal is available. This "gate" feature on the external CAS clock enables the internal CAS line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the CAS clock.

There are three other variations in addressing the module family per device: RAS–only refresh cycle, CAS before RAS refresh cycle, and page mode. All are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with two different cycles: "normal" random read cycle and fast page mode read cycle. The normal read cycle is outlined here, while the fast page mode cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with RAS and CAS active transitions latching the desired bit location. The write (W) input level must be high (V_{IH}), t_{RCS} (minimum) before the CAS or active transition, to enable read mode.

Both the RAS and CAS clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window.

CAS controls read access time: CAS must be active before or at t_{RCD} maximum to guarantee valid data out (Q) at t_{RAC}. If the t_{RCD} maximum is exceeded, read access time is determined by the CAS clock active transition (t_{CAC}).

WRITE CYCLE

The user can write to the DRAM with any of two cycles: early write or fast page mode early write. Early write mode is discussed here, while fast page mode write operation is covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of W to active (V_{IL}). Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP}, apply to write mode, as in the read mode.

An early write cycle is characterized by W active transition at minimum time t_{WCS} before CAS active transition. Column address setup and hold times (t_{ASC}, t_{CAH}) and data in (D) setup and hold times (t_{DS}, t_{DH}) are referenced to CAS in an early write cycle. RAS and CAS clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three–state condition throughout an early write cycle because W active transition precedes or coincides with CAS active transition, keeping data–out buffers disabled.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all column locations (2048 columns) on a selected row of the module family. Read access time in page mode (t_{CAC}) is typically half the regular RAS clock access time, t_{RAC}. Page mode operation consists of keeping RAS active while toggling CAS between V_{IH} and V_{IL}. The row is latched by RAS active transition, while each CAS active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, CAS transitions to inactive for minimum t_{CP}, while RAS remains low (V_{IL}). The second CAS active transition while RAS is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the module require refresh every 32 milliseconds.

This is accomplished by cycling through the 2048 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the module family. Burst refresh, a refresh of all rows consecutively, must be performed every 32 milliseconds.

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decoded. Three other methods of refresh, **RAS–only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS–Only Refresh

RAS–only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter should be employed to ensure that all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). W must be inactive for time t_{WRP} before and time t_{WRH} after RAS active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle while RAS cycles inactive for t_{RP} and back to active starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode entry) as in CAS before RAS refresh.

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a **CAS before RAS refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 2048 test cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 CAS before RAS** initialization cycles. The test procedure is as follows:

1. Write 0s into all memory cells (normal write mode).
2. Select a column address, and read 0 out of the cell by performing **CAS before RAS refresh counter test, read cycle**. Repeat this operation 2048 times.
3. Select a column address, and write 1 into the cell by performing **CAS before RAS refresh counter test, write cycle**. Repeat this operation 2048 times.
4. Read 1s (normal read mode), which were written at step three.
5. Using the same starting column address as in step two, read 1 out and write 0 into the cell by performing the **CAS before RAS refresh counter test, read and write cycles**. Repeat this operation 2048 times.
6. Read 0s which were written in step five in normal read mode.
7. Repeat steps one through six using complement data.

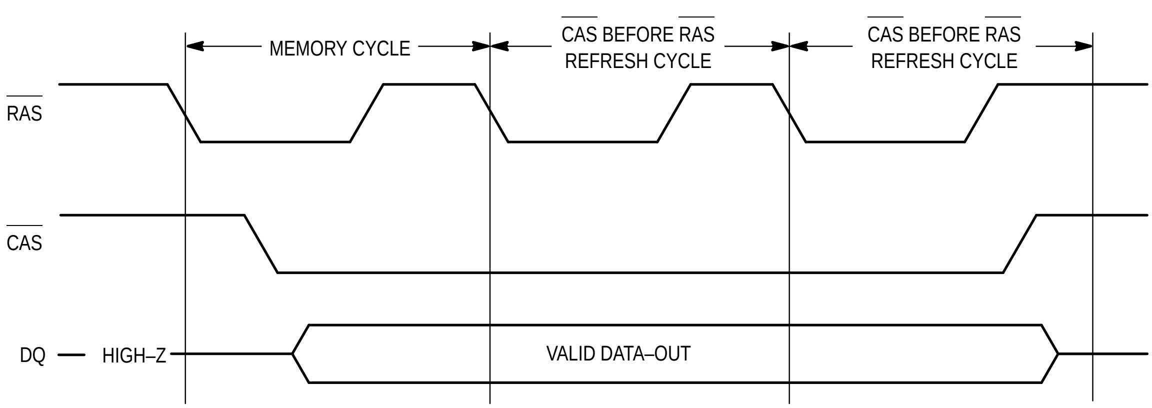


Figure 1. Hidden Refresh Cycle

ORDERING INFORMATION
(Order by Full Part Number)

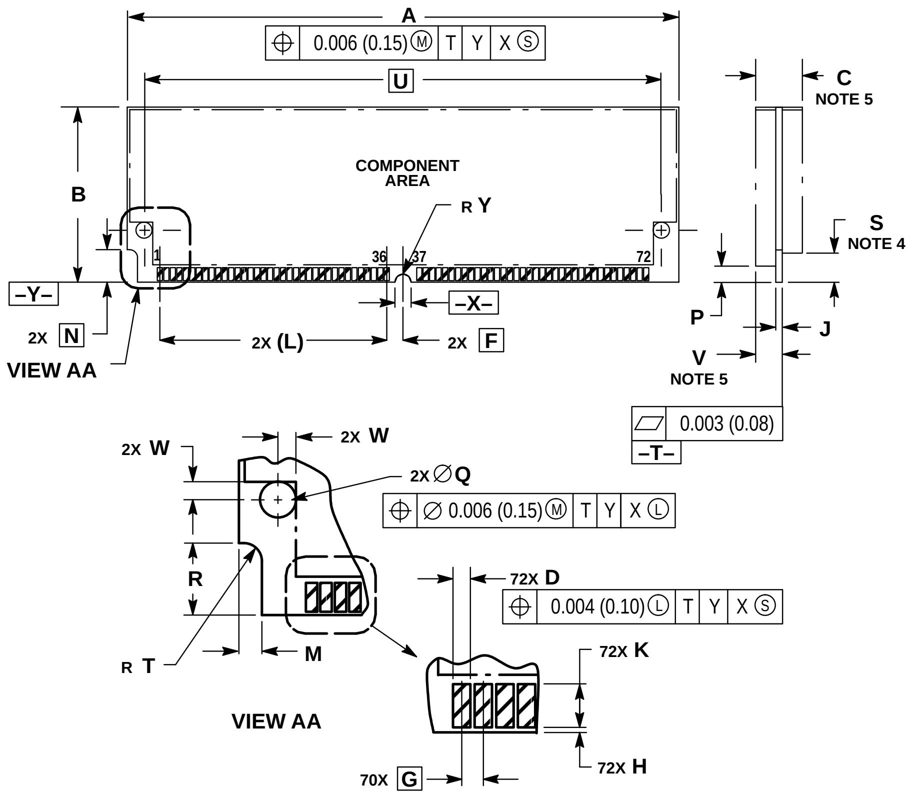
MCM 36800 X XX

- MCM — Motorola Memory Prefix
- 36800 — Part Number
- X — Package (AS = SIMM, ASG = Gold Pad SIMM)
- XX — Speed (60 = 60 ns, 70 = 70 ns)

Full Part Numbers — MCM36800AS60, MCM36800ASG60, MCM36800AS70, MCM36800ASG70

PACKAGE DIMENSIONS

AS PACKAGE
SIMM MODULE
CASE 866J–01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.
4. DIMENSION C AND S DEFINE A DOUBLE–SIDED MODULE.
5. DIMENSION V DEFINES OPTIONAL SINGLE–SIDED MODULE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	4.245	4.255	107.82	108.08
B	1.345	1.355	34.16	34.42
C	—	0.360	—	9.14
D	0.040	0.042	1.02	1.07
F	0.125 BSC		3.18 BSC	
G	0.050 BSC		1.27 BSC	
H	—	0.010	—	0.25
J	0.047	0.053	1.19	1.35
K	0.100	—	2.54	—
L	1.750 REF		44.45 REF	
M	0.075	0.085	1.90	2.16
N	0.400 BSC		10.16 BSC	
P	0.125	—	3.18	—
Q	0.123	0.127	3.12	3.23
R	0.245	0.255	6.22	6.48
S	0.225	—	5.72	—
T	0.060	0.064	1.52	1.63
U	3.984 BSC		101.19 BSC	
V	—	0.208	—	5.28
W	0.044	—	1.12	—
Y	0.060	0.064	1.52	1.63

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