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SEMICONDUCTOR
TECHNICAL DATA

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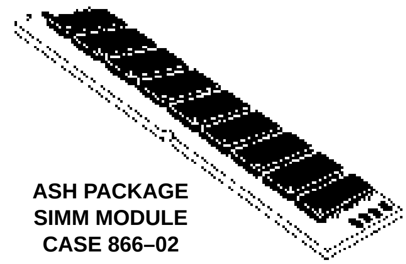
MCM36404

Product Preview

4M x 36 Bit Dynamic Random Access Memory Module

for Error Correction Applications

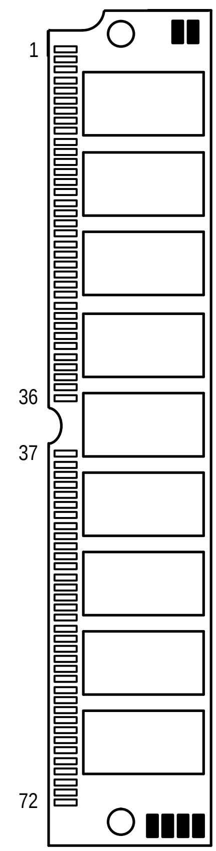


ASH PACKAGE
SIMM MODULE
CASE 866–02

The MCM36404 is a dynamic random access memory (DRAM) module organized as 4,194,304 x 36 bits. The module is a single–sided 72–lead single–in–line memory module (SIMM) consisting of nine MCM517400B DRAMs housed in J–lead small outline packages (SOJ), mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted adjacent to each DRAM. The MCM517400B is a CMOS high–speed dynamic random access memory organized as 4,194,304 four–bit words and fabricated with CMOS silicon–gate process technology.

- Three–State Data Output
- Early–Write Common I/O Capability
- Fast Page Mode Capability
- TTL–Compatible Inputs and Outputs
- RAS–Only Refresh
- CAS Before RAS Refresh
- Hidden Refresh
- 2048 Cycle Refresh: MCM36404 = 32 ms (Max)
- Consists of Nine 4M x 4 DRAMs, and Nine 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time (t_{RAC}): MCM36404–50 = 50 ns (Max)
  MCM36404–60 = 60 ns (Max)
  MCM36404–70 = 70 ns (Max)
- Low Active Power Dissipation: MCM36404–50 = 6.44 W (Max)
  MCM36404–60 = 5.45 W (Max)
  MCM36404–70 = 4.71 W (Max)
- Low Standby Power Dissipation: TTL Levels = 99 mW (Max)
  CMOS Levels = 50 mW (Max)

TOP VIEW



PIN ASSIGNMENTS

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	CAS0	52	DQ25	64	NC
5	DQ3	17	A5	29	DQ16	41	A10	53	DQ26	65	NC
6	DQ4	18	A6	30	V_{CC}	42	NC	54	DQ27	66	NC
7	DQ5	19	G	31	A8	43	NC	55	DQ28	67	PD1
8	DQ6	20	DQ8	32	A9	44	RAS0	56	DQ29	68	PD2
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ30	69	PD3
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD4
11	PD5	23	DQ11	35	DQ17	47	W	59	V_{CC}	71	NC
12	A0	24	DQ12	36	DQ18	48	ECC	60	DQ32	72	V_{SS}

PIN NAMES

A0 – A10	Address Inputs
DQ0 – DQ35	Data Input/Output
CAS0	Column Address Strobe
PD1 – PD5	Presence Detect
RAS0	Row Address Strobe
W	Read/Write Input
ECC	Configuration Detection
G	Output Enable
V_{CC}	Power (+ 5 V)
V_{SS}	Ground
NC	No Connection

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a product under development. Specifications and information herein are subject to change without notice.

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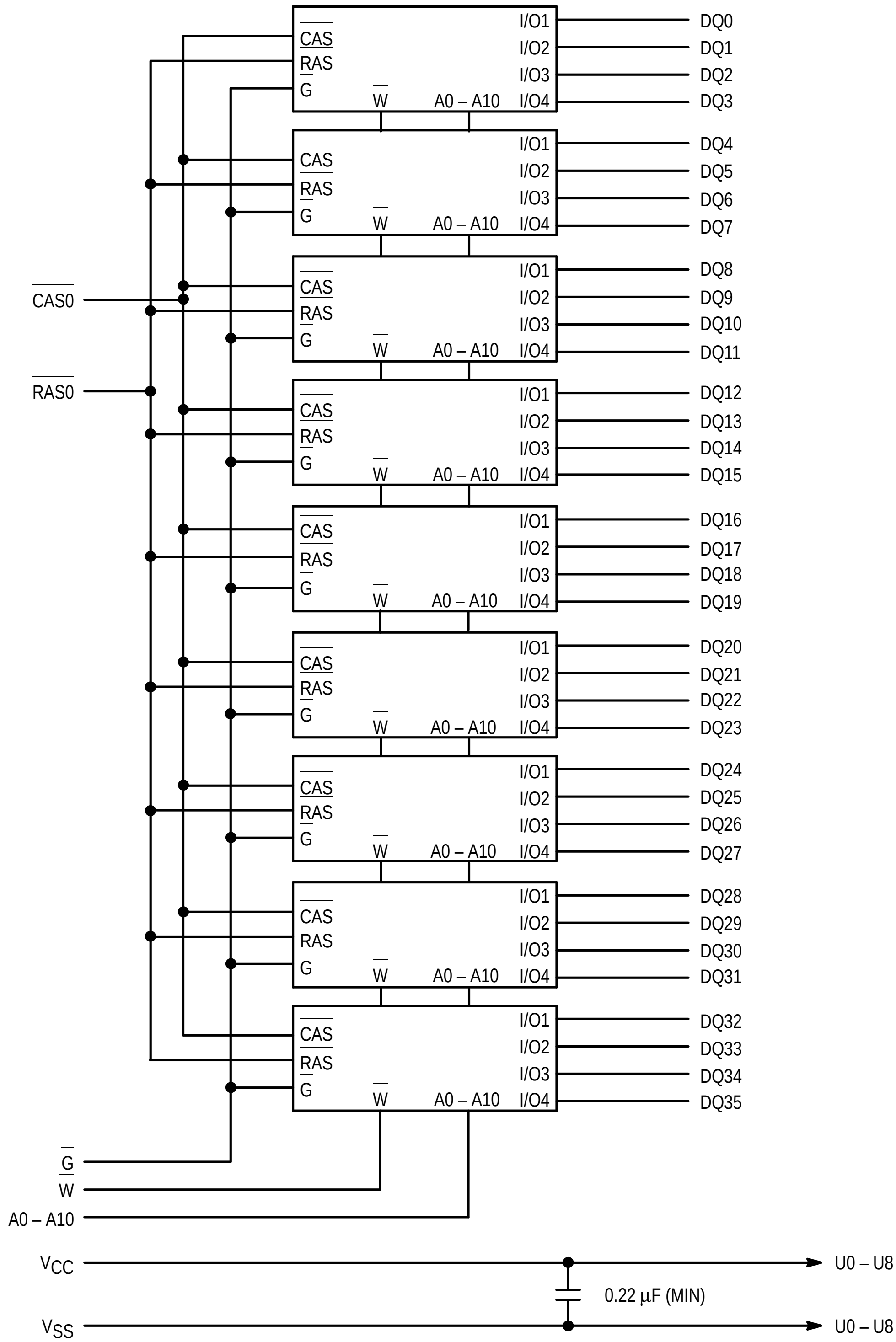
BLOCK DIAGRAM



PRESENCE DETECT PIN OUT			
Pin Name	**50 ns**	**60 ns**	**70 ns**
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	NC	NC	NC
PD3	V_{SS}	NC	V_{SS}
PD4	V_{SS}	NC	NC
PD5*	V_{SS}	V_{SS}	V_{SS}
ECC	V_{SS}	V_{SS}	V_{SS}

*PD5 tied to V_{SS} through a 2.6 kΩ resistor.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to + 7	V
Data Output Current	I_{out}	50	mA
Power Dissipation	P_D	8.1	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	V_{CC} + 0.5 V	V
Logic Low Voltage, All Inputs	V_{IL}	– 0.5*	—	0.8	V

* – 2.0 V at pulse width ≤ 20 ns.

DC CHARACTERISTICS AND SUPPLY CURRENTS (All voltages referenced to V_{SS})

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM36404–50, t_{RC} = 90 ns MCM36404–60, t_{RC} = 110 ns MCM36404–70, t_{RC} = 130 ns	I_{CC1}	— — —	1170 990 855	mA	1, 2
V_{CC} Power Supply Current (Standby) (RAS = CAS = V_{IH})	I_{CC2}	—	18	mA	
V_{CC} Power Supply Current During RAS–Only Refresh Cycles (CAS = V_{IH}) MCM36404–50, t_{RC} = 90 ns MCM36404–60, t_{RC} = 110 ns MCM36404–70, t_{RC} = 130 ns	I_{CC3}	— — —	1170 990 855	mA	1, 2
V_{CC} Power Supply Current During Fast Page Mode Cycle (RAS = V_{IL}) MCM36404–50, t_{PC} = 35 ns MCM36404–60, t_{PC} = 40 ns MCM36404–70, t_{PC} = 45 ns	$I_{CC4(P)}$	— — —	720 630 540	mA	1, 2
V_{CC} Power Supply Current (Standby) (RAS = CAS = V_{CC} – 0.2 V)	I_{CC5}	—	9	mA	
V_{CC} Power Supply Current During CAS Before RAS Refresh Cycle MCM36404–50, t_{RC} = 90 ns MCM36404–60, t_{RC} = 110 ns MCM36404–70, t_{RC} = 130 ns	I_{CC6}	— — —	1170 990 855	mA	1
Input Leakage Current (0 V ≤ V_{in} ≤ V_{CC})	$I_{lkg(I)}$	– 90	90	µA	
Output Leakage Current (0 V ≤ V_{out} ≤ V_{CC}, Output Disable)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	V	

NOTES:
1. Current is a function of cycle rate and output loading; maximum currents are specified cycle time (minimum) with the output open.
2. Address may be changed once or less while RAS = V_{IL}. In the case of I_{CC4}, it can be changed once or less during t_{PC}.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0 – A10 W, G, RAS0, CAS0	C_{in}	55 73	pF
I/O Capacitance	DQ0 – DQ39	$C_{I/O}$	17	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

READ, WRITE, AND READ–WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM36404–50		MCM36404–60		MCM36404–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	90	—	110	—	130	—	ns	5
Read–Write Cycle Time	t_{RELREL}	t_{RWC}	135	—	155	—	180	—	ns	5
Access Time from RAS	t_{RELQV}	t_{RAC}	—	50	—	60	—	70	ns	6, 7
Access Time from CAS	t_{CELQV}	t_{CAC}	—	13	—	15	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	25	—	30	—	35	ns	6, 9
Access Time from Precharge CAS	t_{CEHQV}	t_{CPA}	—	30	—	35	—	40	ns	6
CAS to Output in Low–Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn–Off Delay	t_{CEHQZ}	t_{OFF}	0	13	0	15	0	15	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
RAS Precharge Time	t_{REHREL}	t_{RP}	30	—	40	—	50	—	ns	
RAS Pulse Width	t_{RELREH}	t_{RAS}	50	10 k	60	10 k	70	10 k	ns	
RAS Hold Time	t_{CELREH}	t_{RSH}	13	—	15	—	20	—	ns	
CAS Hold Time	t_{RELCEH}	t_{CSH}	50	—	60	—	70	—	ns	
CAS Precharge to RAS Hold Time	t_{CEHREH}	t_{RHCP}	30	—	35	—	40	—	ns	
CAS Pulse Width	t_{CELCEH}	t_{CAS}	13	10 k	15	10 k	20	10 k	ns	
RAS to CAS Delay Time	t_{RELCEL}	t_{RCD}	17	37	20	45	20	50	ns	11
RAS to Column Address Delay Time	t_{RELAV}	t_{RAD}	12	25	15	30	15	35	ns	12
CAS to RAS Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
CAS Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	7	—	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	10	—	10	—	15	—	ns	
Column Address to RAS Lead Time	t_{AVREH}	t_{RAL}	25	—	30	—	35	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	

NOTES:

(continued)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power–up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

READ, WRITE, AND READ–WRITE CYCLES (Continued)

Parameter	Symbol		MCM36404–50		MCM36404–60		MCM36404–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Read Command Hold Time Referenced to CAS	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to RAS	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to CAS	t_{CELWH}	t_{WCH}	10	—	10	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	10	—	15	—	ns	
Write Command to RAS Lead Time	t_{WLREH}	t_{RWL}	15	—	15	—	20	—	ns	
Write Command to CAS Lead Time	t_{WLCEH}	t_{CWL}	15	—	15	—	20	—	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	14
Data In Hold Time	t_{CELDX}	t_{DH}	10	—	10	—	15	—	ns	14
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	15
CAS to Write Delay	t_{CELWL}	t_{CWD}	35	—	40	—	45	—	ns	15
RAS to Write Delay	t_{RELWL}	t_{RWD}	73	—	85	—	95	—	ns	15
Column Address to Write Delay	t_{AVWL}	t_{AWD}	48	—	55	—	60	—	ns	15
Refresh Period	t_{RVRV}	t_{RFSH}	—	32	—	32	—	32	ms	
CAS Setup Time for CAS Before RAS Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
CAS Hold Time for CAS Before RAS Refresh	t_{RELCEH}	t_{CHR}	10	—	10	—	10	—	ns	
RAS Precharge to CAS Active Time	t_{REHCEL}	t_{RPC}	5	—	5	—	5	—	ns	
CAS Precharge Time for CAS Before RAS Counter Time	t_{CEHCEL}	t_{CPT}	20	—	20	—	20	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	—	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	10	—	ns	
Write to RAS Precharge Time (CAS Before RAS Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	10	—	ns	
Write to RAS Hold Time (CAS Before RAS Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	10	—	ns	
RAS Hold Time Referenced to G	t_{GLREH}	t_{ROH}	10	—	10	—	10	—	ns	
G Access Time	t_{GLQV}	t_{GA}	—	13	—	15	—	15	ns	6
G to Data Delay	t_{GLHDX}	t_{GD}	13	—	15	—	15	—	ns	
Output Buffer Turn–Off Delay Time from G	t_{GHQZ}	t_{GZ}	0	13	0	15	0	15	ns	16
G Command Hold Time	t_{WLGL}	t_{GH}	15	—	15	—	15	—	ns	
Output Disable Setup Time	t_{GHCEL}	t_{ODS}	0	—	0	—	0	—	ns	

NOTES:

13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to CAS leading edge in early write cycles and to W leading edge in late write or read–write cycles.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read–write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
16. t_{OFF} (max) and/or t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

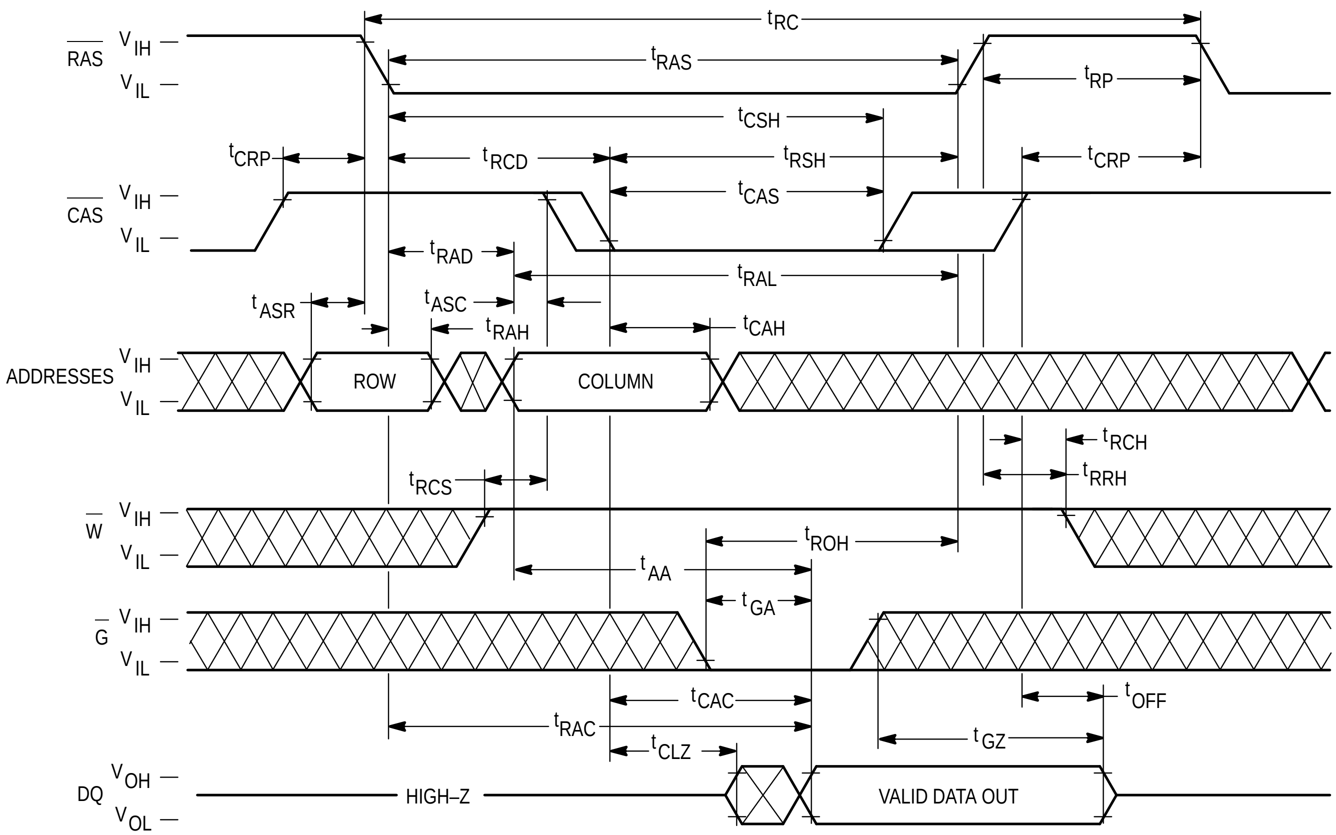
FAST PAGE MODE READ, WRITE, AND READ–WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM36404–50		MCM36404–60		MCM36404–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	35	—	40	—	45	—	ns	
CAS Precharge to RAS Hold Time (Fast Page Mode)	t_{CEHREH}	t_{RHCP}	30	—	35	—	40	—	ns	
Fast Page Mode Read–Write Cycle Time	t_{CELCEL}	t_{PRWC}	80	—	85	—	95	—	ns	
RAS Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	50	200 k	60	200 k	70	200 k	ns	
CAS Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	53	—	60	—	65	—	ns	5

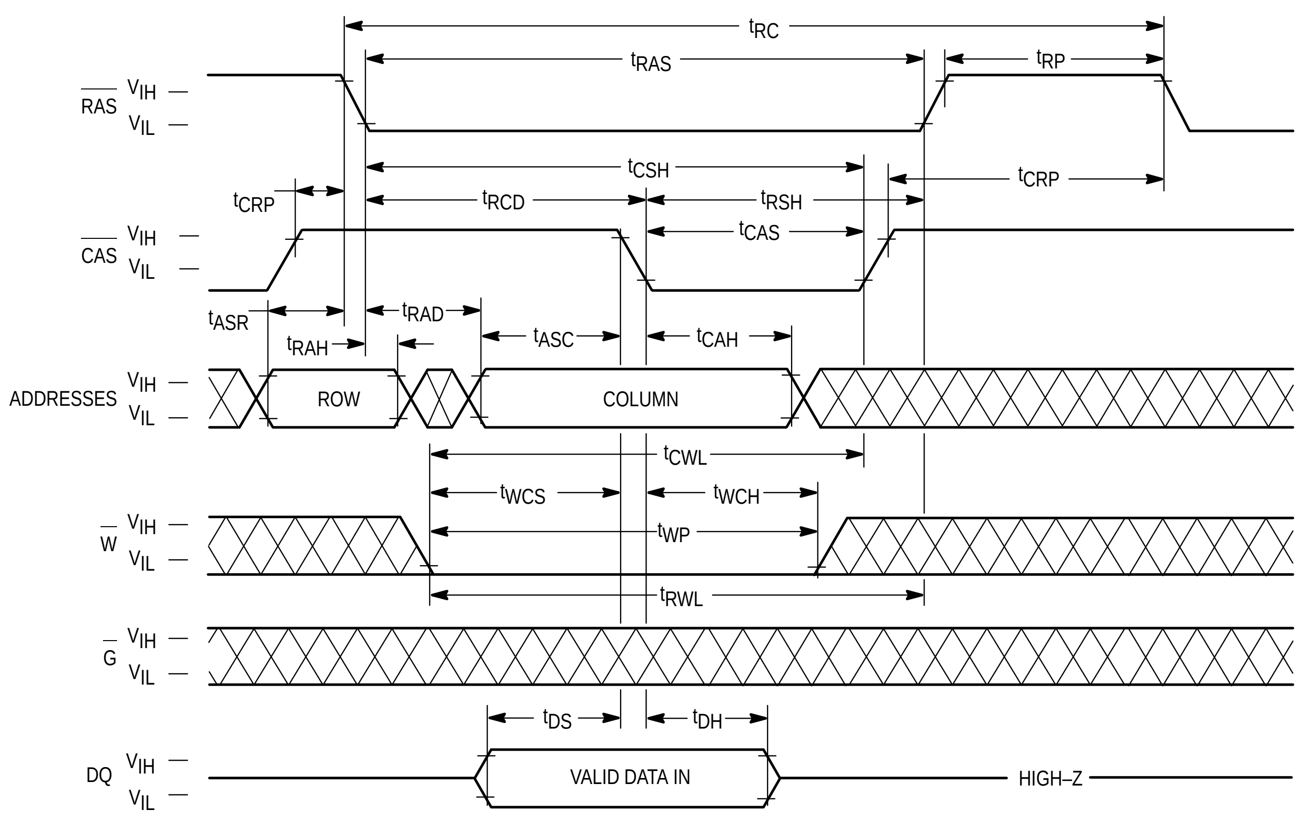
NOTES:

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power–up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through–out the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read–write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

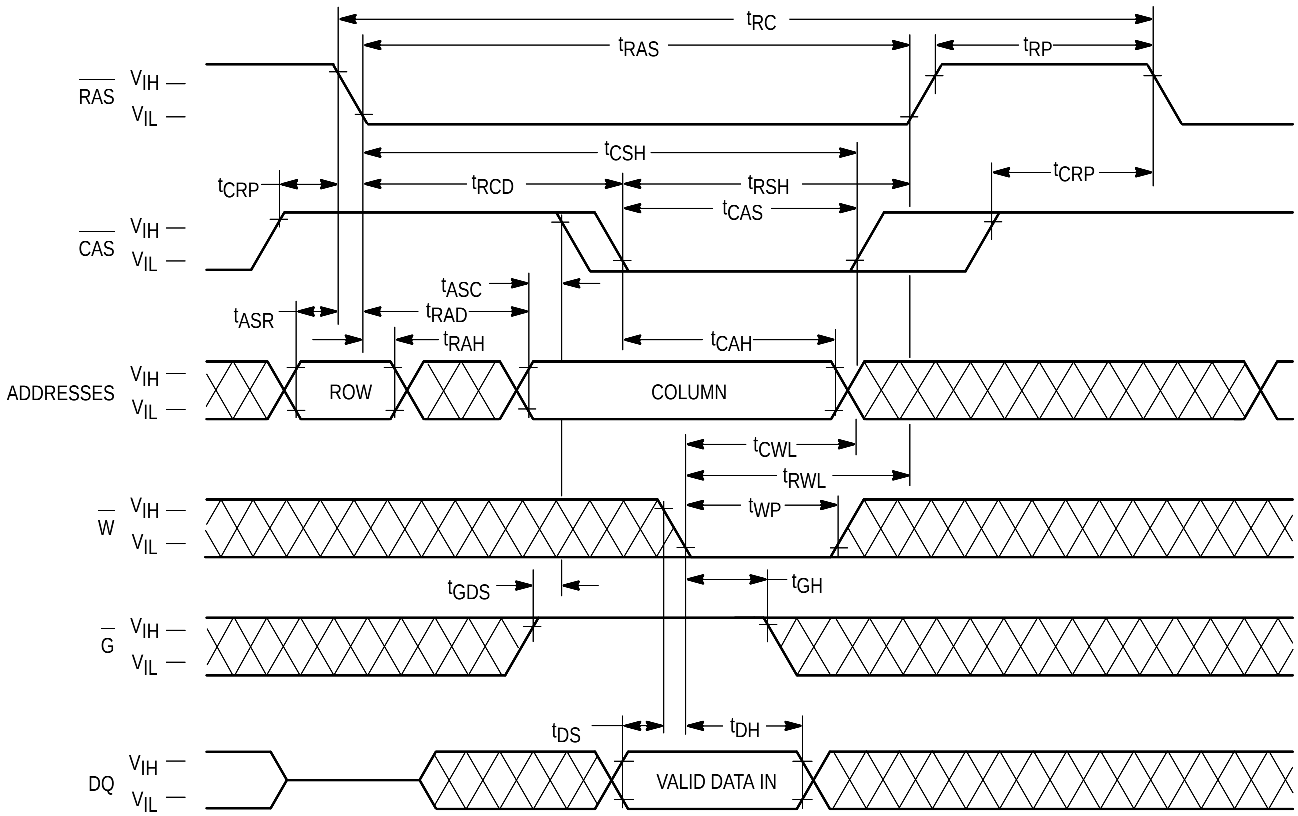
READ CYCLE (FAST PAGE MODE)



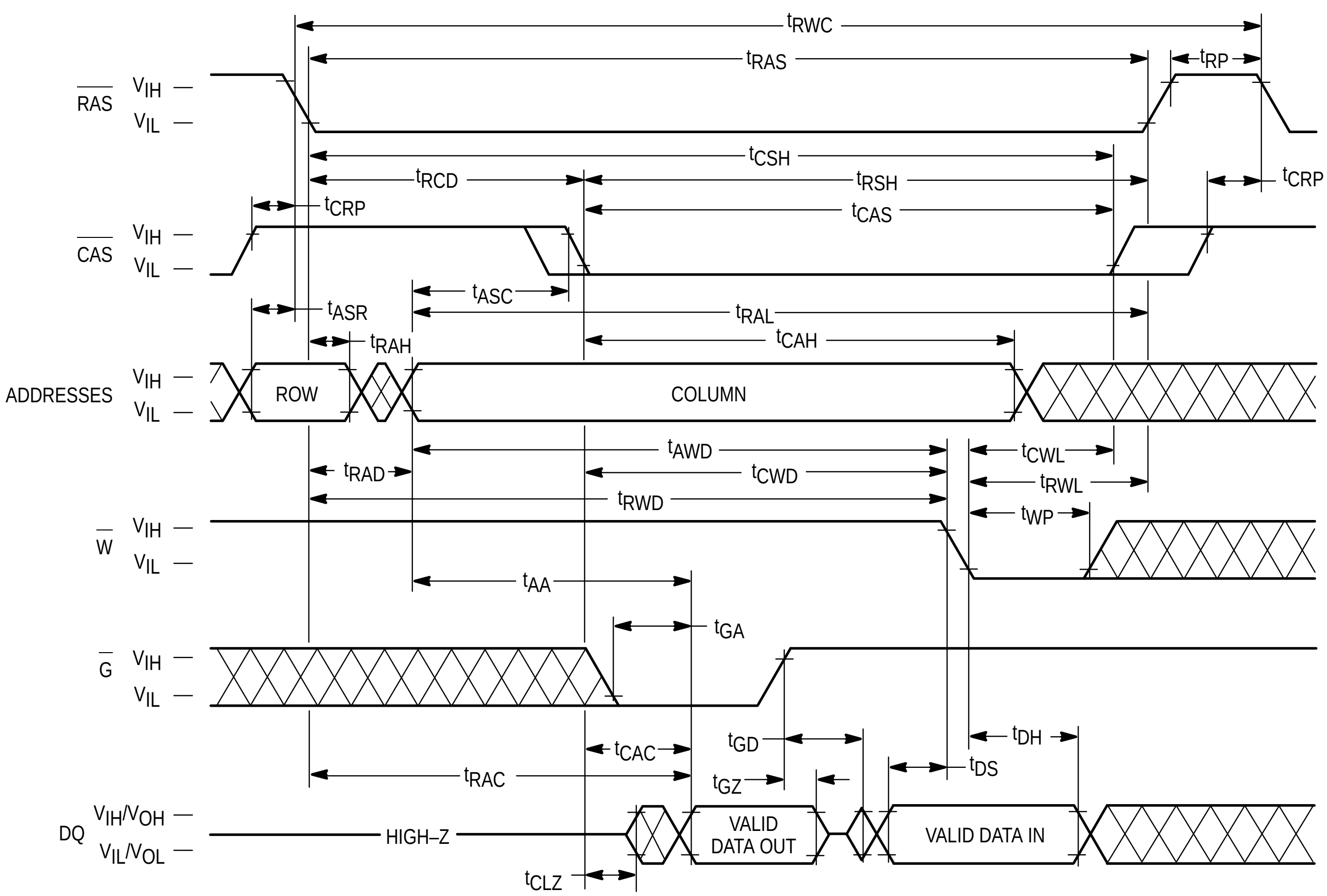
EARLY WRITE CYCLE



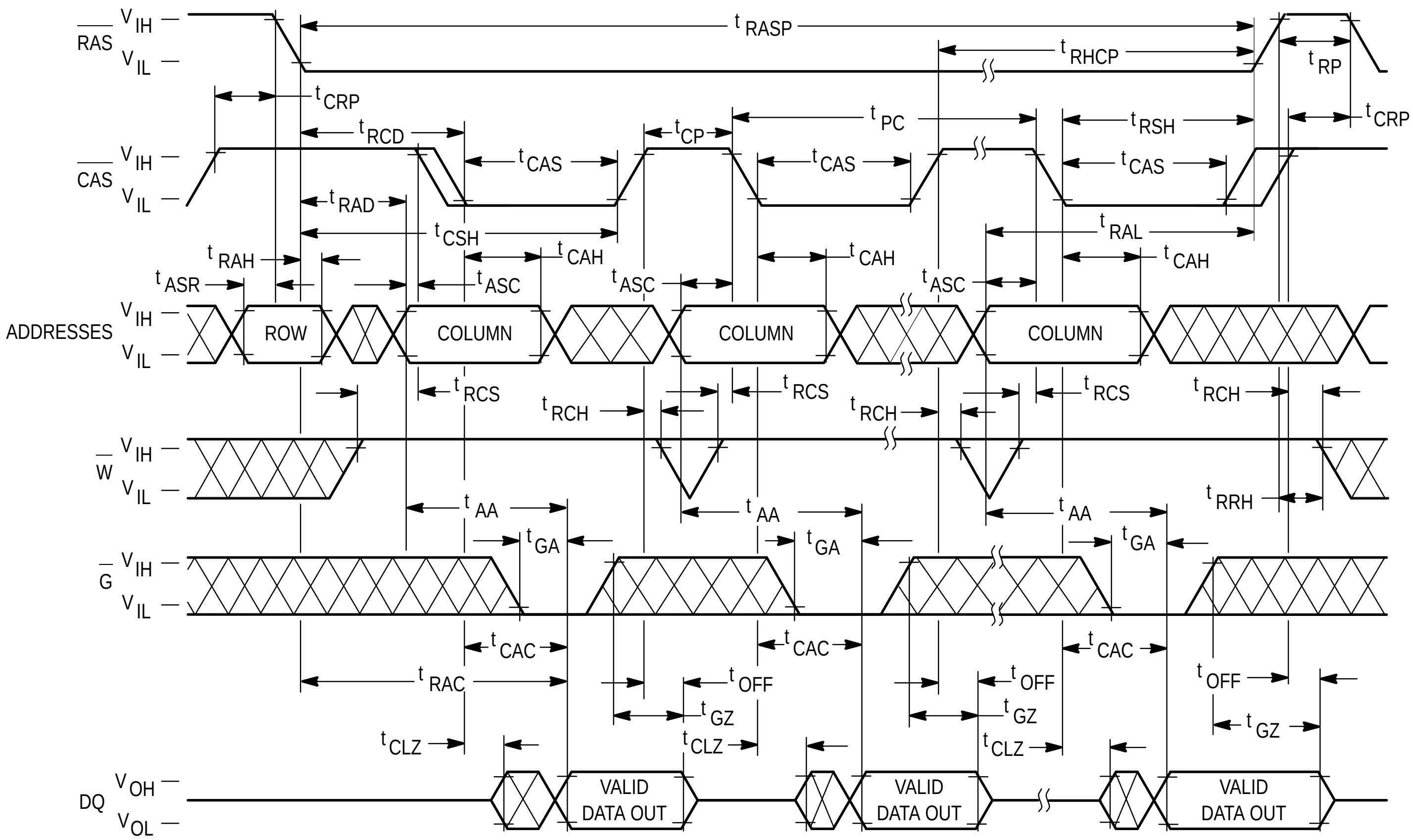
$\overline{G}$ CONTROLLED LATE WRITE CYCLE



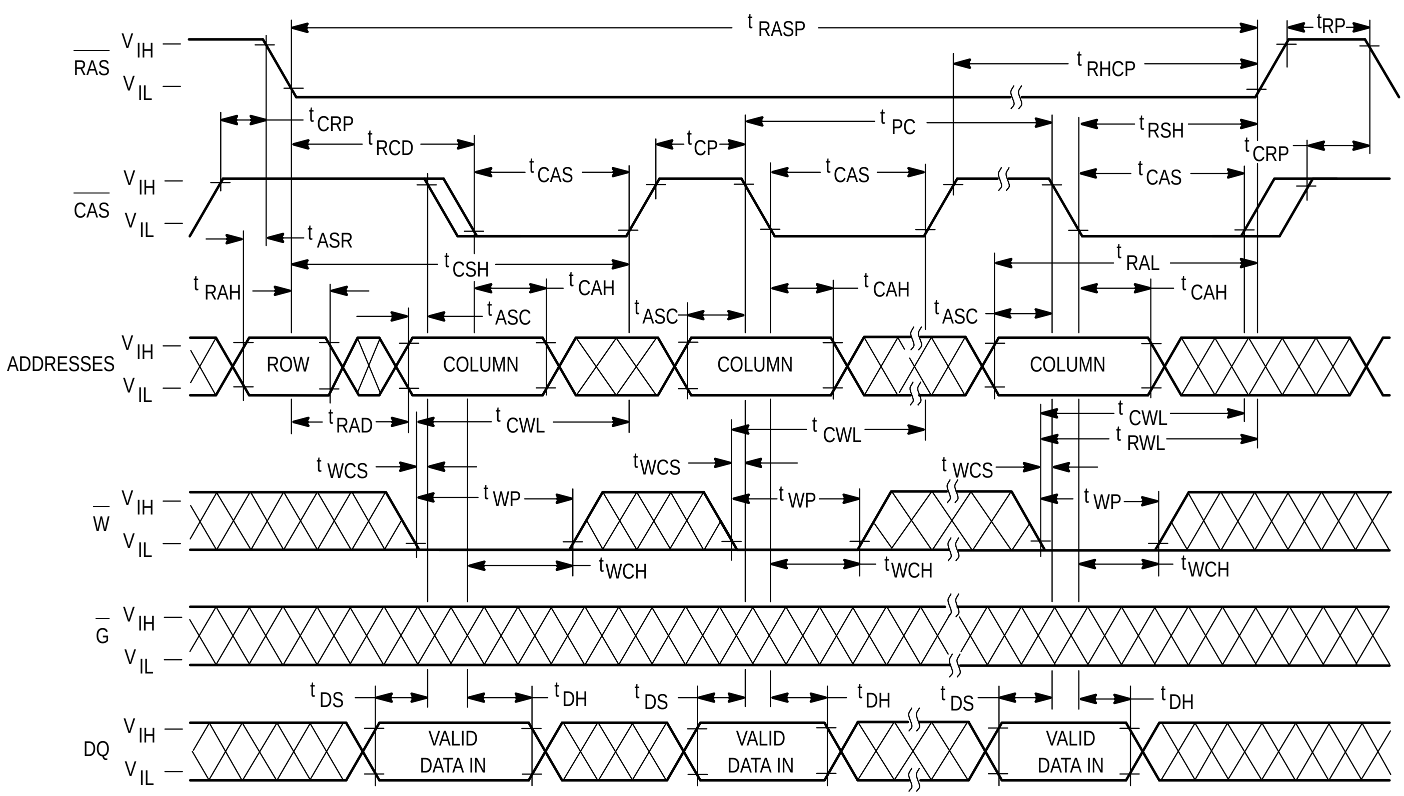
READ–WRITE CYCLE



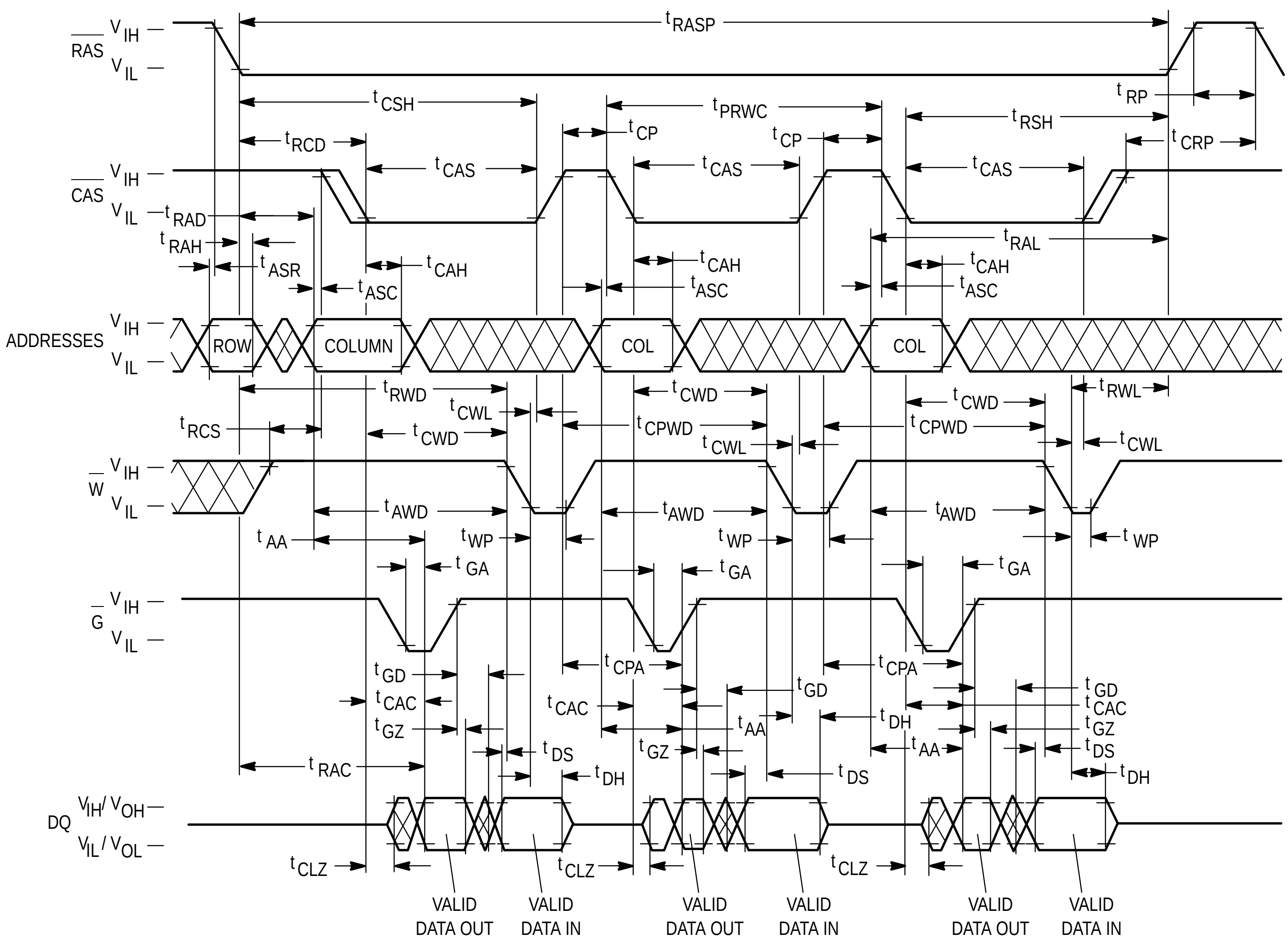
FAST PAGE MODE READ CYCLE



FAST PAGE MODE EARLY WRITE CYCLE

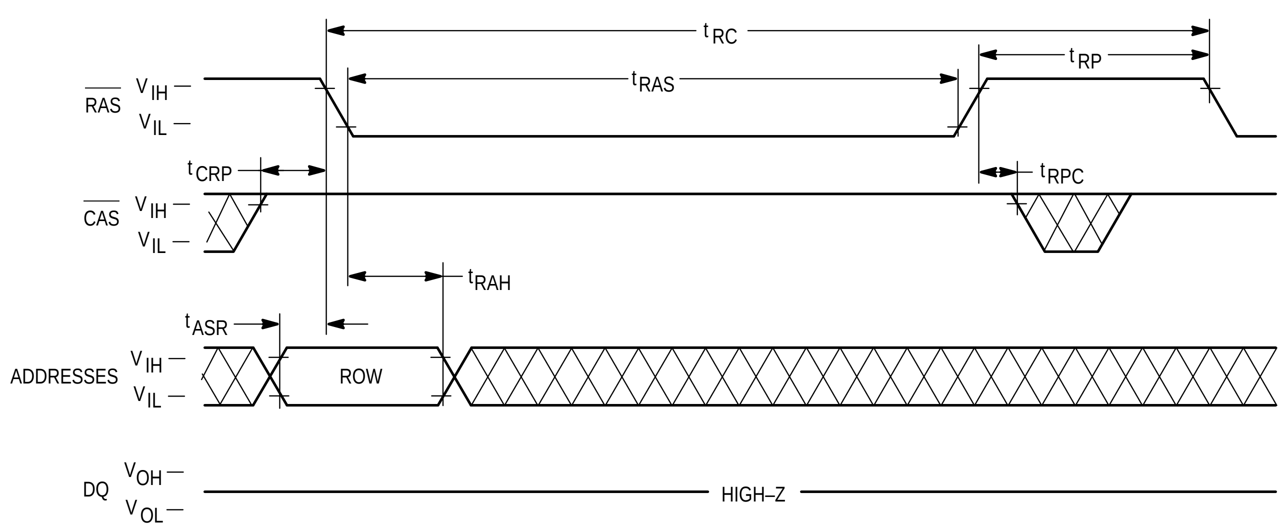


FAST PAGE MODE READ–WRITE CYCLE



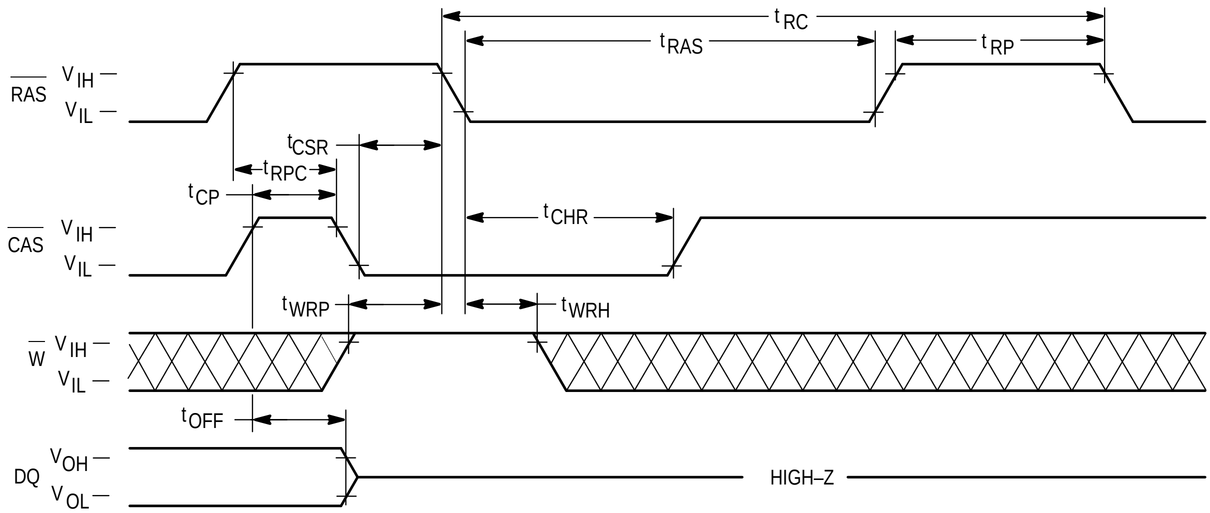
RAS–ONLY REFRESH CYCLE

(W and G are Don't Care)

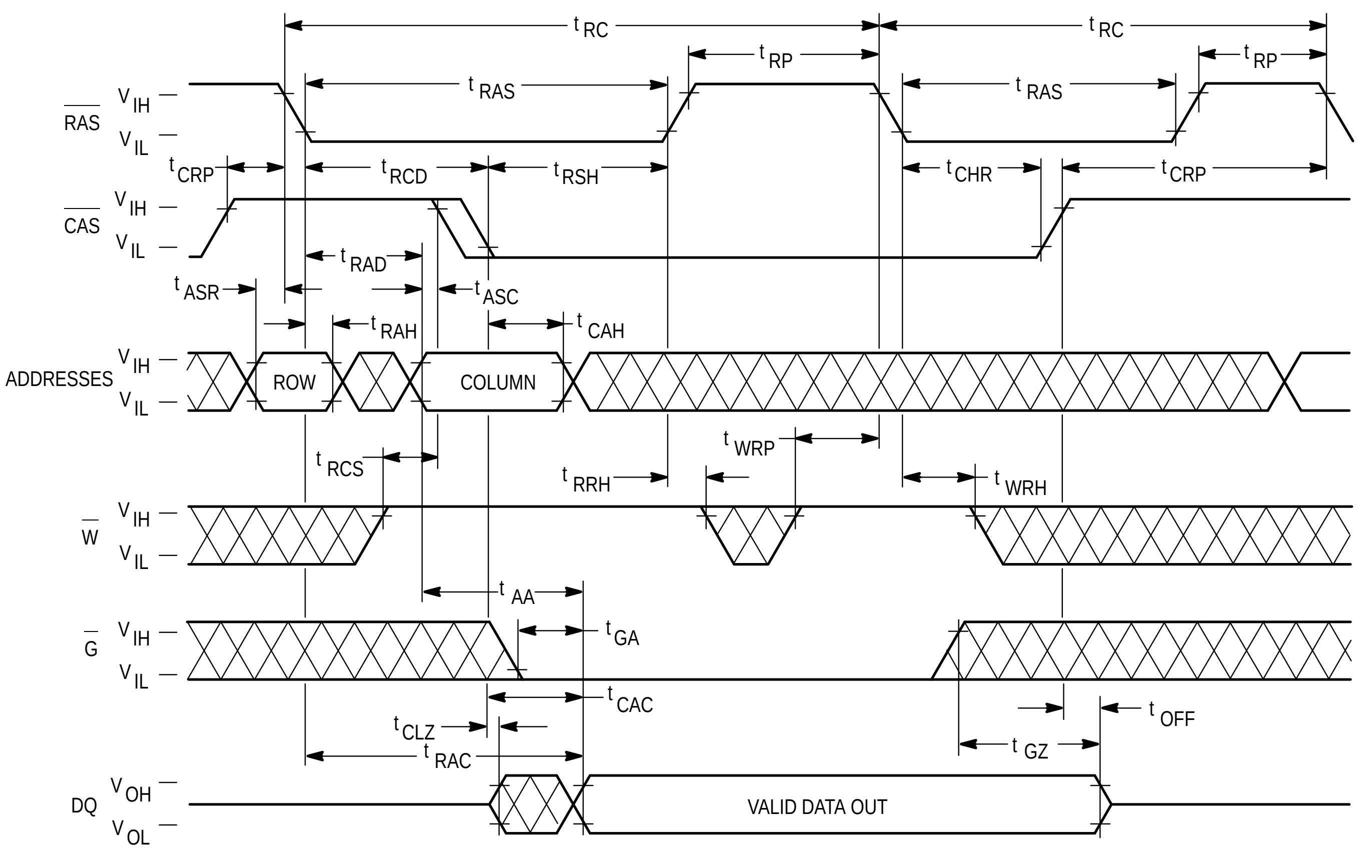


CAS BEFORE RAS REFRESH CYCLE

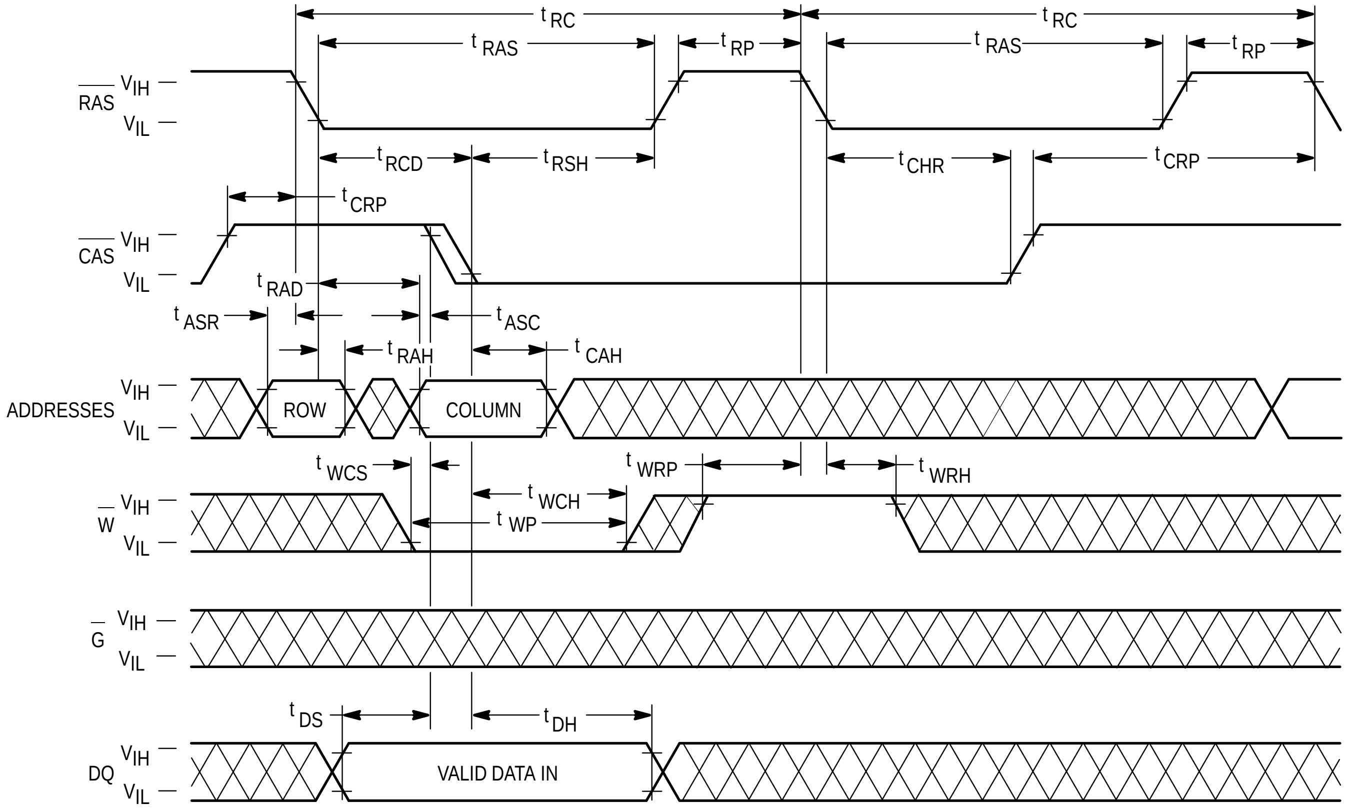
(G and A0 – A10 are Don't Care)



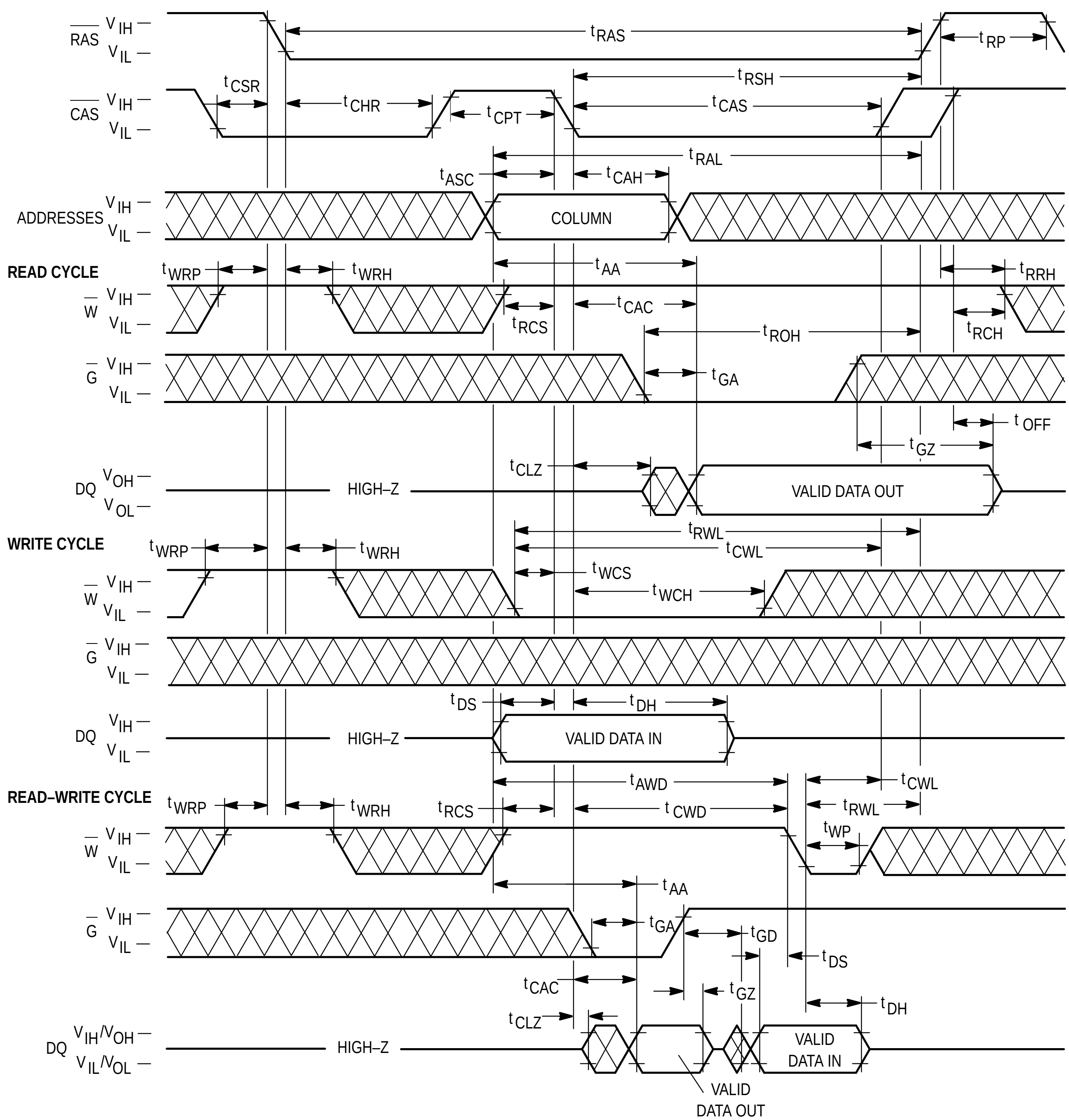
HIDDEN REFRESH CYCLE (READ) (FAST PAGE MODE)



HIDDEN REFRESH CYCLE (EARLY WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power–up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 32 milliseconds), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe (RAS) and column address strobe (CAS), into two separate 11–bit address fields. A total of twenty two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 word locations in the device. RAS active transition is followed by CAS active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between RAS and CAS active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external CAS signal is ignored until an internal RAS signal is available. This "gate" feature on the external CAS clock enables the internal CAS line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the CAS clock.

There are three other variations in addressing the 16M module family per device: RAS–only refresh cycle, CAS before RAS refresh cycle, and page mode. All are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, fast page mode read cycle, read–write cycle, and fast page mode read–write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with RAS and CAS active transitions latching the desired bit location. The write (W) input level must be high (V_{IH}), t_{RCS} (minimum) before the CAS or active transition, to enable read mode.

Both the RAS and CAS clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window.

Both CAS and output enable (G) control read access time: CAS must be active before or at t_{RCD} maximum and G must be active t_{RAC}–t_{GA} (both minimum) after RAS active transition to guarantee valid data out (Q) at t_{RAC}. If the t_{RCD} maximum is exceeded and/or G active transition does not occur in time, read access time is determined by either the CAS or G clock active transition (t_{CAC} or t_{GA}).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, fast page mode early write, and fast page mode read–write. Early and late write modes are discussed here, while fast page mode write operation is covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of W to active (V_{IL}). Early and late write modes are distinguished by the active transition of W, with respect to CAS. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP}, apply to write mode, as in the read mode.

An early write cycle is characterized by W active transition at minimum time t_{WCS} before CAS active transition. Column address setup and hold times (t_{ASC}, t_{CAH}) and data in (D) setup and hold times (t_{DS}, t_{DH}) are referenced to CAS in an early write cycle. RAS and CAS clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

Q remains in three–state condition throughout an early write cycle because W active transition precedes or coincides with CAS active transition, keeping data–out buffers disabled.

A late–write cycle (referred to as G–controlled write) occurs when W active transition is made after CAS active transition. W active transition could be delayed for almost 10 microseconds after CAS active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T$) $\le t_{RAS}$, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D timing parameters are referenced to W active transition in a late write cycle. Output buffers are enabled by CAS active transition. Outputs are switched off by G inactive transition, which is required to write to the device. Q may be indeterminate (see note 15 of AC Operating Conditions table). RAS and CAS must remain active for t_{RWL} and t_{CWL}, respectively, after W active transition to complete the write cycle. G must remain inactive for t_{GH} after W active transition to complete the write cycle.

READ–WRITE CYCLE

A read–write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except W must remain high for t_{CWD} and/or t_{AWD} minimum, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all column locations (2048 columns) on a selected row of the module family. Read access time in page mode (t_{CAC}) is typically half the regular RAS clock access time, t_{RAC}. Page mode operation consists of keeping RAS active while toggling CAS between V_{IH} and V_{IL}. The row is latched by RAS active transition, while each CAS active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read–write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, CAS transitions to inactive for minimum t_{CP}, while RAS remains low (V_{IL}). The second CAS active transition while RAS is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read–write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the module require refresh every 32 milliseconds.

This is accomplished by cycling through the 2048 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the module family. Burst refresh, a refresh of all rows consecutively, must be performed every 32 milliseconds.

A normal read, write, or read–write operation to the RAM will refresh all the bits associated with the particular row decoded. Three other methods of refresh, **RAS–only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS–Only Refresh

RAS–only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter should be employed to ensure that all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). W must be inactive for time t_{WRP} before and time t_{WRH} after RAS active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle while RAS cycles inactive for t_{RP} and back to active starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode entry) as in CAS before RAS refresh.

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **CAS before RAS refresh counter test**. This test is performed with a read–write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 2048 cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight **CAS before RAS** initialization cycles. Test procedure:

1. Write 0s into all memory cells with normal write mode.
2. Select a column address, read 0 out and write 1 into the cell by performing the **CAS before RAS refresh counter test, read–write cycle**. Repeat this operation 2048 times.
3. Read the 1s that were written in step two in normal read mode.
4. Using the same starting column address as in step two, read 1 out and write 0 into the cell by performing the **CAS before RAS refresh counter test, read–write cycle**. Repeat this operation 2048 times.
5. Read 0s which were written in step four in normal read mode.
6. Repeat steps one through five using complement data.

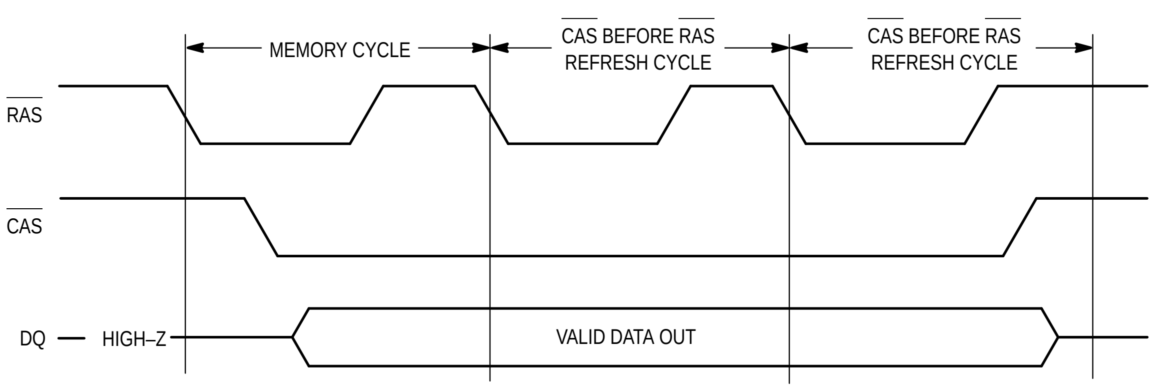
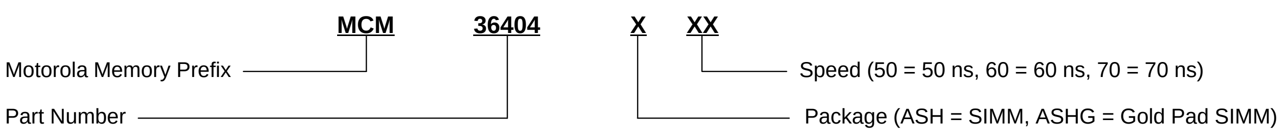


Figure 1. Hidden Refresh Cycle

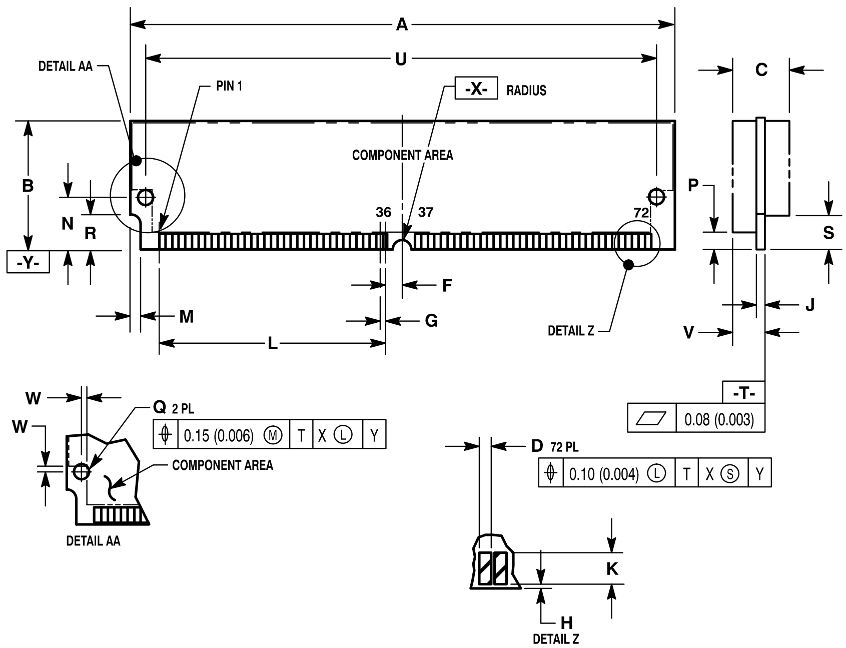
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM36404ASH50 MCM36404ASHG50
MCM36404ASH60 MCM36404ASHG60
MCM36404ASH70 MCM36404ASHG70

PACKAGE DIMENSIONS

ASH PACKAGE
SIMM MODULE
CASE 866–02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	107.82	108.08	4.245	4.255
B	25.27	25.53	0.995	1.005
C	—	9.14	—	0.360
D	1.02	1.07	0.040	0.042
F	3.18 BSC		0.125 BSC	
G	1.27 BSC		0.050 BSC	
H	—	0.25	—	0.010
J	1.19	1.37	0.047	0.054
K	0.25	—	0.100	—
L	44.45 REF		1.750 REF	
M	1.90	2.16	0.075	0.085
N	10.16 BSC		0.400 BSC	
P	3.18	—	0.125	—
Q	3.12	3.22	0.123	0.127
R	6.22	6.48	0.245	0.255
S	5.72	—	0.225	—
U	101.19 BSC		3.984 BSC	
V	—	5.28	—	0.208
W	1.12	—	0.044	—
X	1.52	1.63	0.060	0.064

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