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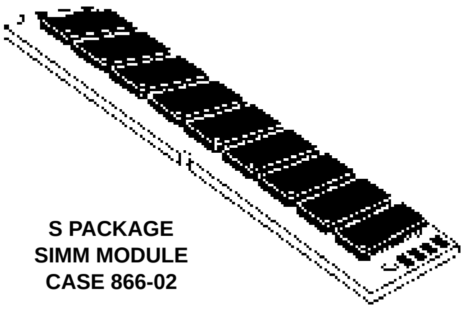
**SEMICONDUCTOR
TECHNICAL DATA**

**MCM36204**

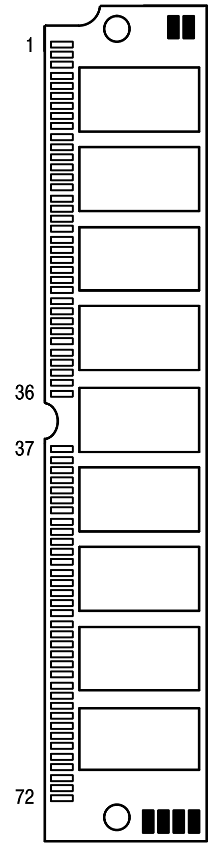
# 2M x 36 Bit ECC Dynamic Random Access Memory Module
## for Error Correction Applications


**S PACKAGE
SIMM MODULE
CASE 866-02**

The MCM36204 is a 72M dynamic random access memory (DRAM) module organized as 2,097,152 x 36 bits. The module is a double-sided 72-lead single-in-line memory module (SIMM) consisting of eighteen MCM54400AN DRAMs housed in 20/26 J-lead small outline packages (SOJ), mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted under each DRAM. The MCM54400AN is a CMOS high-speed dynamic random access memory organized as 1,048,576 four-bit words and fabricated with CMOS silicon-gate process technology.

- Three-State Data Output
- Early-Write Common I/O Capability
- Fast Page Mode Capability
- TTL-Compatible Inputs and Outputs
- $\overline{\text{RAS}}$-Only Refresh
- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: 16 ms (Max)
- Consists of Eighteen 1M x 4 DRAMs, and Eighteen 0.22 µF (Min) Decoupling Capacitors
- Unlatched Data Out at Cycle End Allows Two Dimensional Chip Selection
- Fast Access Time ($t_{RAC}$): MCM36204-60 = 60 ns (Max)
  MCM36204-70 = 70 ns (Max)
- Low Active Power Dissipation: MCM36204-60 = 6.04 W (Max)
  MCM36204-70 = 5.05 W (Max)
- Low Standby Power Dissipation: TTL Levels = 198 mW (Max)
  CMOS Levels= 99 mW (Max)

**TOP VIEW**



**PIN NAMES**

| | | | |
|---|---|---|---|
| A0 – A9 | Address Inputs | DQ0 – DQ35 | Data Input/Output |
| $\overline{\text{CAS0}}$, $\overline{\text{CAS1}}$ | Column Address Strobe | PD1 – PD5 | Presence Detect |
| $\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$ | Row Address Strobe | $\overline{\text{W}}$ | Read/Write Input |
| $\overline{\text{ECC}}$ | Configuration Detection | $\overline{\text{OE}}$ | Output Enable |
| $V_{CC}$ | Power (+ 5 V) | $V_{SS}$ | Ground |
| NC | No Connection | | |

All power supply and ground pins must be connected for proper operation of the device.

**PIN ASSIGNMENTS**

| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{SS}$ | 13 | A1 | 25 | DQ13 | 37 | DQ19 | 49 | DQ22 | 61 | DQ33 |
| 2 | DQ0 | 14 | A2 | 26 | DQ14 | 38 | DQ20 | 50 | DQ23 | 62 | DQ34 |
| 3 | DQ1 | 15 | A3 | 27 | DQ15 | 39 | $V_{SS}$ | 51 | DQ24 | 63 | DQ35 |
| 4 | DQ2 | 16 | A4 | 28 | A7 | 40 | $\overline{\text{CAS0}}$ | 52 | DQ25 | 64 | NC |
| 5 | DQ3 | 17 | A5 | 29 | DQ16 | 41 | NC | 53 | DQ26 | 65 | NC |
| 6 | DQ4 | 18 | A6 | 30 | $V_{CC}$ | 42 | NC | 54 | DQ27 | 66 | NC |
| 7 | DQ5 | 19 | $\overline{\text{OE}}$ | 31 | A8 | 43 | $\overline{\text{CAS1}}$ | 55 | DQ28 | 67 | PD1 |
| 8 | DQ6 | 20 | DQ8 | 32 | A9 | 44 | $\overline{\text{RAS0}}$ | 56 | DQ29 | 68 | PD2 |
| 9 | DQ7 | 21 | DQ9 | 33 | NC | 45 | $\overline{\text{RAS1}}$ | 57 | DQ30 | 69 | PD3 |
| 10 | $V_{CC}$ | 22 | DQ10 | 34 | NC | 46 | DQ21 | 58 | DQ31 | 70 | PD4 |
| 11 | PD5 | 23 | DQ11 | 35 | DQ17 | 47 | $\overline{\text{W}}$ | 59 | $V_{CC}$ | 71 | NC |
| 12 | A0 | 24 | DQ12 | 36 | DQ18 | 48 | $\overline{\text{ECC}}$ | 60 | DQ32 | 72 | $V_{SS}$ |

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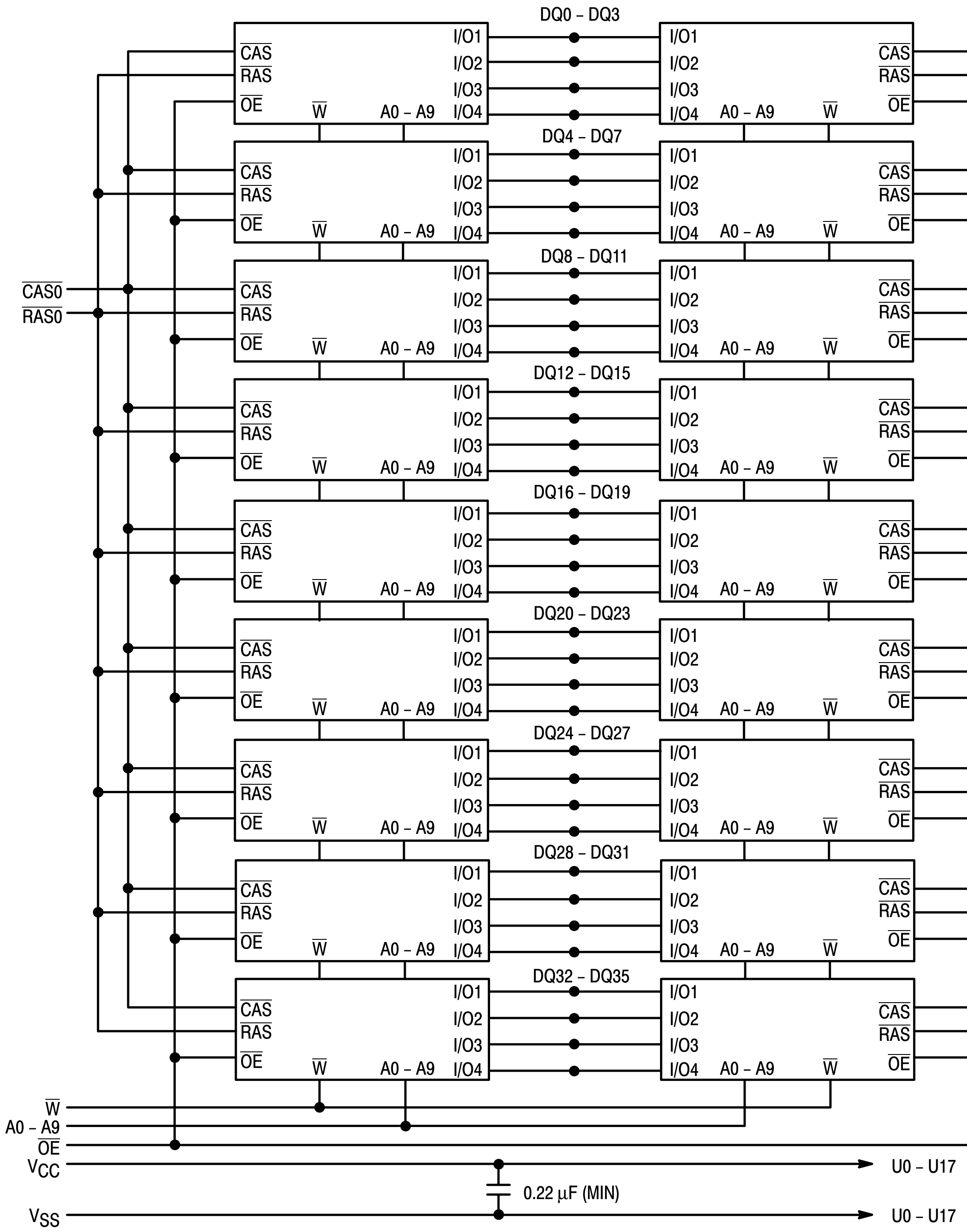
## BLOCK DIAGRAM



| PRESENCE DETECT PIN OUT | | |
|---|---|---|
| **Pin Name** | **60 ns** | **70 ns** |
| PD1 | NC | NC |
| PD2 | NC | NC |
| PD3 | NC | $V_{SS}$ |
| PD4 | NC | NC |
| PD5 | NC | NC |
| $\overline{\text{ECC}}$ | $V_{SS}$ | $V_{SS}$ |

### ABSOLUTE MAXIMUM RATINGS (See Note)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | – 1 to + 7 | V |
| Voltage Relative to $V_{SS}$ (For Any Pin Except $V_{CC}$) | $V_{in}$, $V_{out}$ | – 1 to + 7 | V |
| Data Output Current per DQ Pin | $I_{out}$ | 50 | mA |
| Power Dissipation | $P_D$ | 12.6 | W |
| Operating Temperature Range | $T_A$ | 0 to + 70 | °C |
| Storage Temperature Range | $T_{stg}$ | – 55 to + 125 | °C |

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high-impedance circuits.

## DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}$ = 5.0 V ± 10%, $T_A$ = 0 to 70°C, Unless Otherwise Noted)

### RECOMMENDED OPERATING CONDITIONS (All voltages referenced to $V_{SS}$)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage (Operating Voltage Range) | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
|  | $V_{SS}$ | 0 | 0 | 0 |  |
| Logic High Voltage, All Inputs | $V_{IH}$ | 2.4 | — | 6.5 | V |
| Logic Low Voltage, All Inputs | $V_{IL}$ | – 1.0 | — | 0.8 | V |

### DC CHARACTERISTICS AND SUPPLY CURRENTS

| Characteristic | | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{CC}$ Power Supply Current | MCM36204-60, $t_{RC}$ = 110 ns<br>MCM36204-70, $t_{RC}$ = 130 ns | $I_{CC1}$ | —<br>— | 1098<br>918 | mA | 1 |
| $V_{CC}$ Power Supply Current (Standby) ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ = $V_{IH}$) | | $I_{CC2}$ | — | 36 | mA | |
| $V_{CC}$ Power Supply Current During $\overline{\text{RAS}}$ only Refresh Cycles | MCM36204-60, $t_{RC}$ = 110 ns<br>MCM36204-70, $t_{RC}$ = 130 ns | $I_{CC3}$ | —<br>— | 1098<br>918 | mA | 1 |
| $V_{CC}$ Power Supply Current During Fast Page Mode Cycle | MCM36204-60, $t_{PC}$ = 45 ns<br>MCM36204-70, $t_{PC}$ = 45 ns | $I_{CC4}$ | —<br>— | 648<br>648 | mA | 1, 2, 3 |
| $V_{CC}$ Power Supply Current (Standby) ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ = $V_{CC}$ – 0.2 V) | | $I_{CC5}$ | — | 18 | mA | |
| $V_{CC}$ Power Supply Current During $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle | MCM36204-60, $t_{RC}$ = 110 ns<br>MCM36204-70, $t_{RC}$ = 130 ns | $I_{CC6}$ | —<br>— | 1098<br>918 | mA | 1 |
| Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$) | | $I_{lkg(I)}$ | – 180 | 180 | µA | |
| Output Leakage Current ($\overline{\text{CAS}}$ at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$) | | $I_{lkg(O)}$ | – 20 | 20 | µA | |
| Output High Voltage ($I_{OH}$ = – 5 mA) | | $V_{OH}$ | 2.4 | — | V | |
| Output Low Voltage ($I_{OL}$ = 4.2 mA) | | $V_{OL}$ | — | 0.4 | V | |

NOTES:

1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Measured with one address transition per page mode cycle.
3. Assumes both banks not refreshed simultaneously.

### CAPACITANCE (f = 1.0 MHz, $T_A$ = 25°C, $V_{CC}$ = 5 V, Periodically Sampled Rather Than 100% Tested)

| Characteristic | | Symbol | Max | Unit |
|---|---|---|---|---|
| Input Capacitance | A0 – A9<br>$\overline{\text{W}}$, $\overline{\text{OE}}$<br>$\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$, $\overline{\text{CAS0}}$, $\overline{\text{CAS1}}$ | $C_{in}$ | 100<br>136<br>73 | pF |
| I/O Capacitance | DQ0 – DQ35 | $C_{I/O}$ | 24 | pF |

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = I\,\Delta t/\Delta V$.

# AC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC}$ = 5.0 V ± 10%, $T_A$ = 0 to 70°C, Unless Otherwise Noted)

**READ, WRITE, AND READ-WRITE CYCLES** (See Notes 1, 2, 3, 4, and 5)

| Parameter | Symbol | | MCM36204-60 | | MCM36204-70 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | Std | Alt | Min | Max | Min | Max | | |
| Random Read or Write Cycle Time | $t_{RELREL}$ | $t_{RC}$ | 110 | — | 130 | — | ns | 6 |
| Read-Write Cycle Time | $t_{RELREL}$ | $t_{RWC}$ | 165 | — | 185 | — | ns | 6 |
| Fast Page Mode Cycle Time | $t_{CELCEL}$ | $t_{PC}$ | 45 | — | 45 | — | ns | |
| Fast Page Mode Read-Write Cycle Time | $t_{CELCEL}$ | $t_{PRWC}$ | 95 | — | 100 | — | ns | |
| Access Time from $\overline{\text{RAS}}$ | $t_{RELQV}$ | $t_{RAC}$ | — | 60 | — | 70 | ns | 7, 8 |
| Access Time from $\overline{\text{CAS}}$ | $t_{CELQV}$ | $t_{CAC}$ | — | 20 | — | 20 | ns | 7, 9 |
| Access Time from Column Address | $t_{AVQV}$ | $t_{AA}$ | — | 30 | — | 35 | ns | 7, 10 |
| Access Time from Precharge $\overline{\text{CAS}}$ | $t_{CEHQV}$ | $t_{CPA}$ | — | 40 | — | 40 | ns | 7 |
| $\overline{\text{CAS}}$ to Output in Low-Z | $t_{CELQX}$ | $t_{CLZ}$ | 0 | — | 0 | — | ns | 7 |
| Output Buffer and Turn-Off Delay | $t_{CEHQZ}$ | $t_{OFF}$ | 0 | 20 | 0 | 20 | ns | 11 |
| Transition Time (Rise and Fall) | $t_T$ | $t_T$ | 3 | 50 | 3 | 50 | ns | |
| $\overline{\text{RAS}}$ Precharge Time | $t_{REHREL}$ | $t_{RP}$ | 40 | — | 50 | — | ns | |
| $\overline{\text{RAS}}$ Pulse Width | $t_{RELREH}$ | $t_{RAS}$ | 60 | 10 k | 70 | 10 k | ns | |
| $\overline{\text{RAS}}$ Pulse Width (Fast Page Mode) | $t_{RELREH}$ | $t_{RASP}$ | 60 | 200 k | 70 | 200 k | ns | |
| $\overline{\text{RAS}}$ Hold Time | $t_{CELREH}$ | $t_{RSH}$ | 20 | — | 20 | — | ns | |
| $\overline{\text{CAS}}$ Hold Time | $t_{RELCEH}$ | $t_{CSH}$ | 60 | — | 70 | — | ns | |
| $\overline{\text{CAS}}$ Precharge to $\overline{\text{RAS}}$ Hold Time | $t_{CEHREH}$ | $t_{RHCP}$ | 40 | — | 40 | — | ns | |
| $\overline{\text{CAS}}$ Pulse Width | $t_{CELCEH}$ | $t_{CAS}$ | 20 | 10 k | 20 | 10 k | ns | |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time | $t_{RELCEL}$ | $t_{RCD}$ | 20 | 40 | 20 | 50 | ns | 12 |
| $\overline{\text{RAS}}$ to Column Address Delay Time | $t_{RELAV}$ | $t_{RAD}$ | 15 | 30 | 15 | 35 | ns | 13 |
| $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time | $t_{CEHREL}$ | $t_{CRP}$ | 5 | — | 5 | — | ns | |
| $\overline{\text{CAS}}$ Precharge Time | $t_{CEHCEL}$ | $t_{CP}$ | 10 | — | 10 | — | ns | |
| Row Address Setup Time | $t_{AVREL}$ | $t_{ASR}$ | 0 | — | 0 | — | ns | |
| Row Address Hold Time | $t_{RELAX}$ | $t_{RAH}$ | 10 | — | 10 | — | ns | |

NOTES:

(continued)

1. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}$ and $V_{IL}$.
2. An initial pause of 200 µs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between $V_{IH}$ and $V_{IL}$ (or between $V_{IL}$ and $V_{IH}$) in a monotonic manner.
4. AC measurements $t_T$ = 5.0 ns.
5. To avoid bus contention and potential damage to the module, $\overline{\text{RAS0}}$ and $\overline{\text{RAS1}}$ may not be active low simultaneously.
6. The specification for $t_{RC}$ (min) and $t_{RWC}$ (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ $T_A$ ≤ 70°C) is ensured.
7. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at $V_{OH}$ = 2.0 V and $V_{OL}$ = 0.8 V.
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max).
9. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max).
11. $t_{OFF}$ (max) and/or $t_{GZ}$ (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
12. Operation within the $t_{RCD}$ (max) limit ensures that $t_{RAC}$ (max) can be met. $t_{RCD}$ (max) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled exclusively by $t_{CAC}$.
13. Operation within the $t_{RAD}$ (max) limit ensures that $t_{RAC}$ (max) can be met. $t_{RAD}$ (max) is specified as a reference point only; if $t_{RAD}$ is greater than the specified $t_{RAD}$ (max), then access time is controlled exclusively by $t_{AA}$.

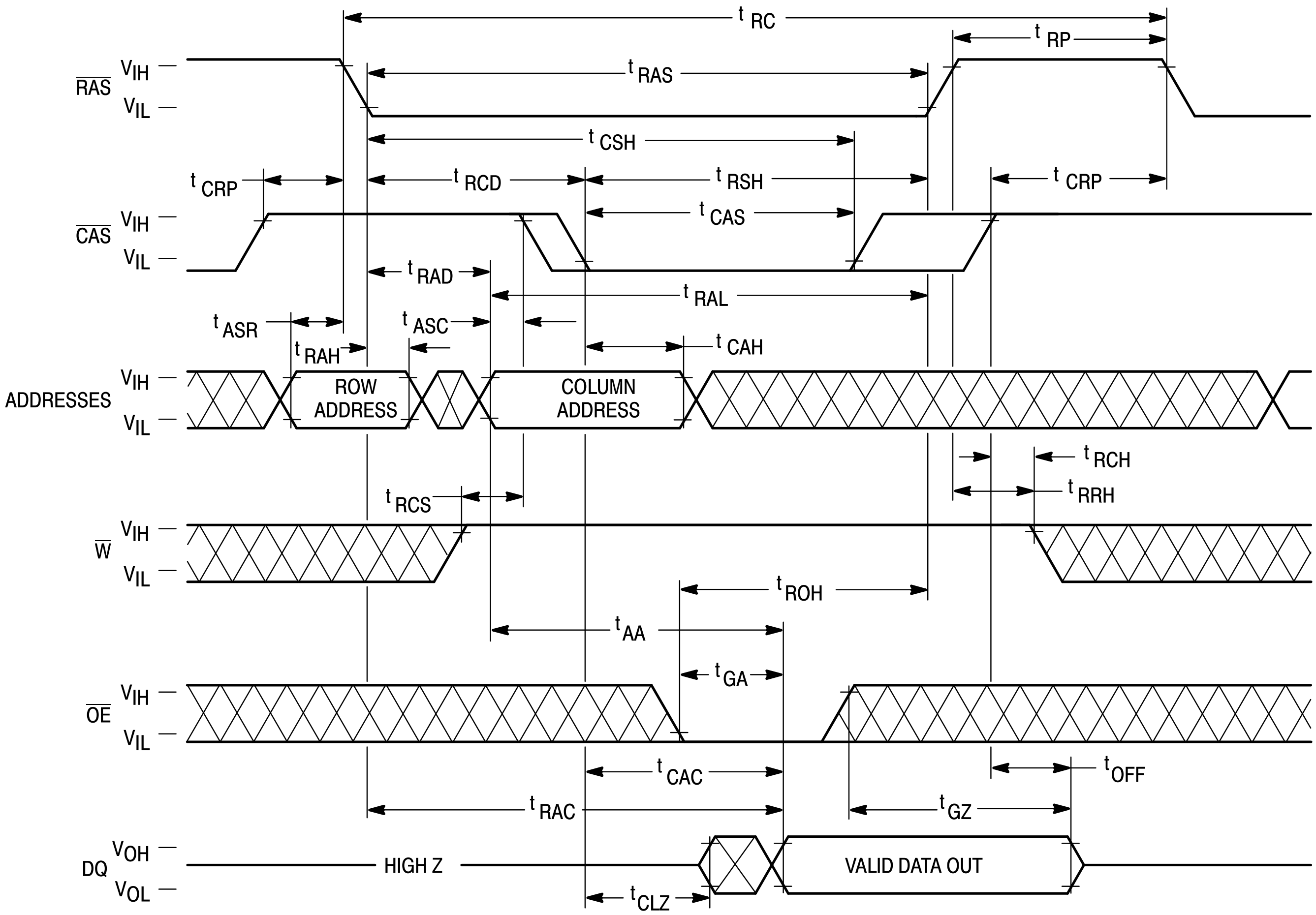
**READ, WRITE, AND READ-WRITE CYCLES** (Continued)

| Parameter | Symbol | | MCM36204-60 | | MCM36204-70 | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|
| | Std | Alt | Min | Max | Min | Max | | |
| Column Address Setup Time | $t_{AVCEL}$ | $t_{ASC}$ | 0 | — | 0 | — | ns | |
| Column Address Hold Time | $t_{CELAX}$ | $t_{CAH}$ | 15 | — | 15 | — | ns | |
| Column Address to $\overline{\text{RAS}}$ Lead Time | $t_{AVREH}$ | $t_{RAL}$ | 30 | — | 35 | — | ns | |
| Read Command Setup Time | $t_{WHCEL}$ | $t_{RCS}$ | 0 | — | 0 | — | ns | |
| Read Command Hold Time Referenced to $\overline{\text{CAS}}$ | $t_{CEHWX}$ | $t_{RCH}$ | 0 | — | 0 | — | ns | 14 |
| Read Command Hold Time Referenced to $\overline{\text{RAS}}$ | $t_{REHWX}$ | $t_{RRH}$ | 0 | — | 0 | — | ns | 14 |
| Write Command Hold Time Referenced to $\overline{\text{CAS}}$ | $t_{CELWH}$ | $t_{WCH}$ | 10 | — | 15 | — | ns | |
| Write Command Pulse Width | $t_{WLWH}$ | $t_{WP}$ | 10 | — | 15 | — | ns | |
| Write Command to $\overline{\text{RAS}}$ Lead Time | $t_{WLREH}$ | $t_{RWL}$ | 20 | — | 20 | — | ns | |
| Write Command to $\overline{\text{CAS}}$ Lead Time | $t_{WLCEH}$ | $t_{CWL}$ | 20 | — | 20 | — | ns | |
| Data in Setup Time | $t_{DVCEL}$ | $t_{DS}$ | 0 | — | 0 | — | ns | 15 |
| Data in Hold Time | $t_{CELDX}$ | $t_{DH}$ | 15 | — | 15 | — | ns | 15 |
| Refresh Period | $t_{RVRV}$ | $t_{RFSH}$ | — | 16 | — | 16 | ms | |
| Write Command Setup Time | $t_{WLCEL}$ | $t_{WCS}$ | 0 | — | 0 | — | ns | 16 |
| $\overline{\text{CAS}}$ to Write Delay | $t_{CELWL}$ | $t_{CWD}$ | 50 | — | 50 | — | ns | 16 |
| $\overline{\text{RAS}}$ to Write Delay | $t_{RELWL}$ | $t_{RWD}$ | 90 | — | 100 | — | ns | 16 |
| Column Address to Write Delay Time | $t_{AVWL}$ | $t_{AWD}$ | 60 | — | 65 | — | ns | 16 |
| $\overline{\text{CAS}}$ Precharge to Write Delay Time (Page Mode) | $t_{CEHWL}$ | $t_{CPWD}$ | 70 | — | 70 | — | ns | 16 |
| $\overline{\text{CAS}}$ Setup Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh | $t_{RELCEL}$ | $t_{CSR}$ | 5 | — | 5 | — | ns | |
| $\overline{\text{CAS}}$ Hold Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh | $t_{RELCEH}$ | $t_{CHR}$ | 15 | — | 15 | — | ns | |
| $\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Active Time | $t_{REHCEL}$ | $t_{RPC}$ | 0 | — | 0 | — | ns | |
| $\overline{\text{CAS}}$ Precharge Time for $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Counter Time | $t_{CEHCEL}$ | $t_{CPT}$ | 30 | — | 40 | — | ns | |
| $\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{OE}}$ | $t_{GLREH}$ | $t_{ROH}$ | 10 | — | 10 | — | ns | |
| $\overline{\text{OE}}$ Access Time | $t_{GLQV}$ | $t_{GA}$ | — | 20 | — | 20 | ns | |
| $\overline{\text{OE}}$ to Data Delay | $t_{GLHDX}$ | $t_{GD}$ | 20 | — | 20 | — | ns | |
| Output Buffer Turn-Off Delay Time from $\overline{\text{OE}}$ | $t_{GHQZ}$ | $t_{GZ}$ | 0 | 20 | 0 | 20 | ns | 11 |
| $\overline{\text{OE}}$ Command Hold Time | $t_{WLGL}$ | $t_{GH}$ | 20 | — | 20 | — | ns | |

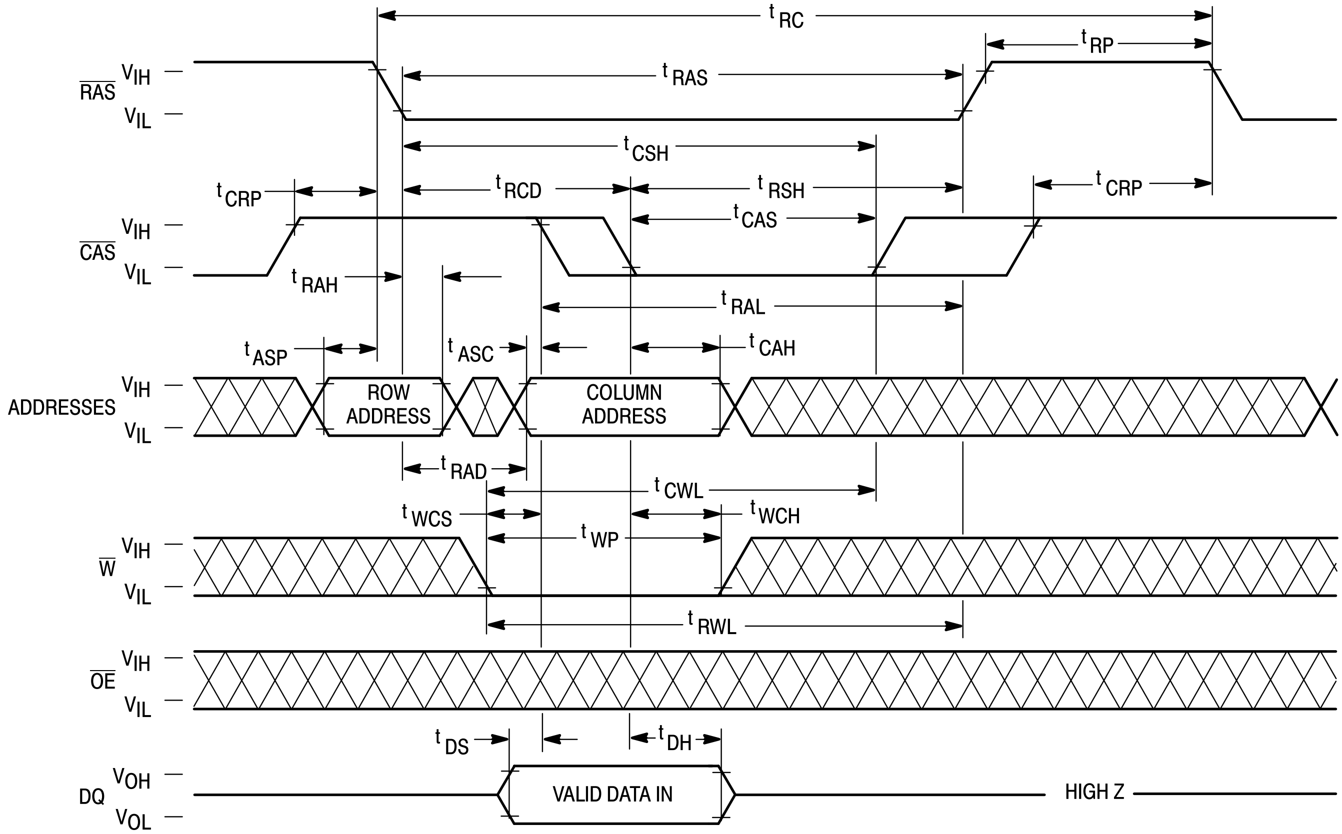
NOTES:

14. Either $t_{RRH}$ or $t_{RCH}$ must be satisfied for a read cycle.
15. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{W}}$ leading edge in late write or read-write cycles.
16. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{AWD}$, and $t_{CPWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

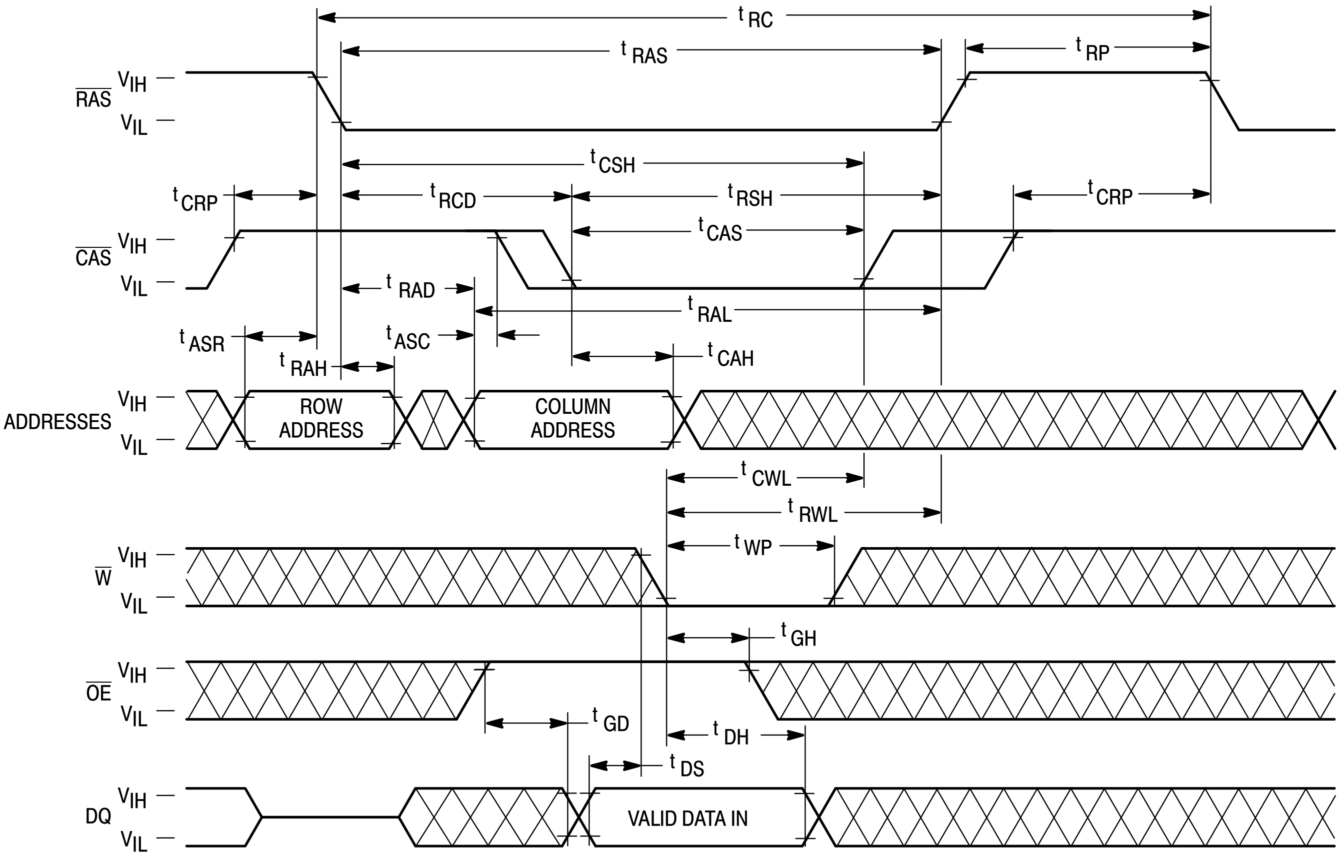
## READ CYCLE



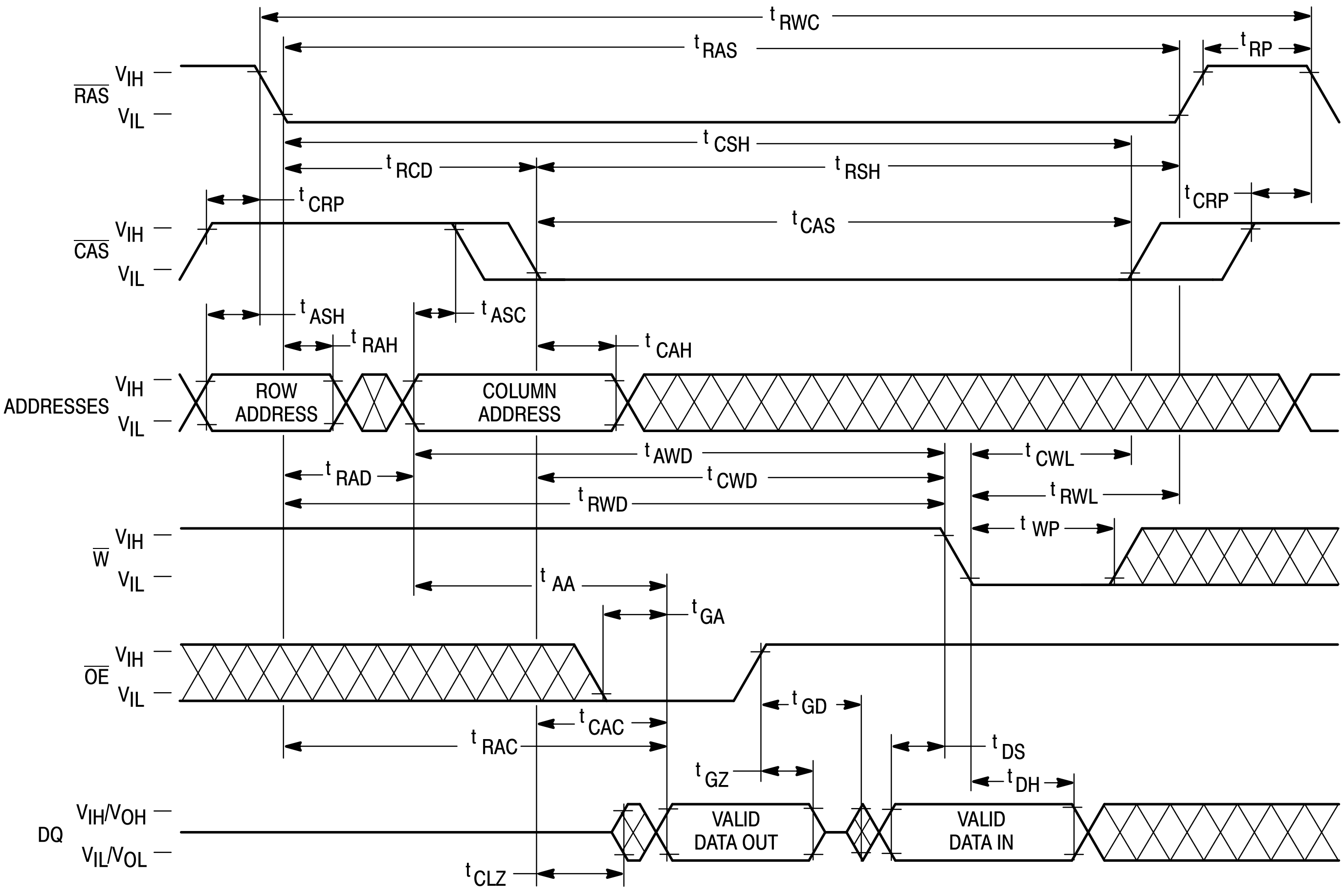
## EARLY WRITE CYCLE



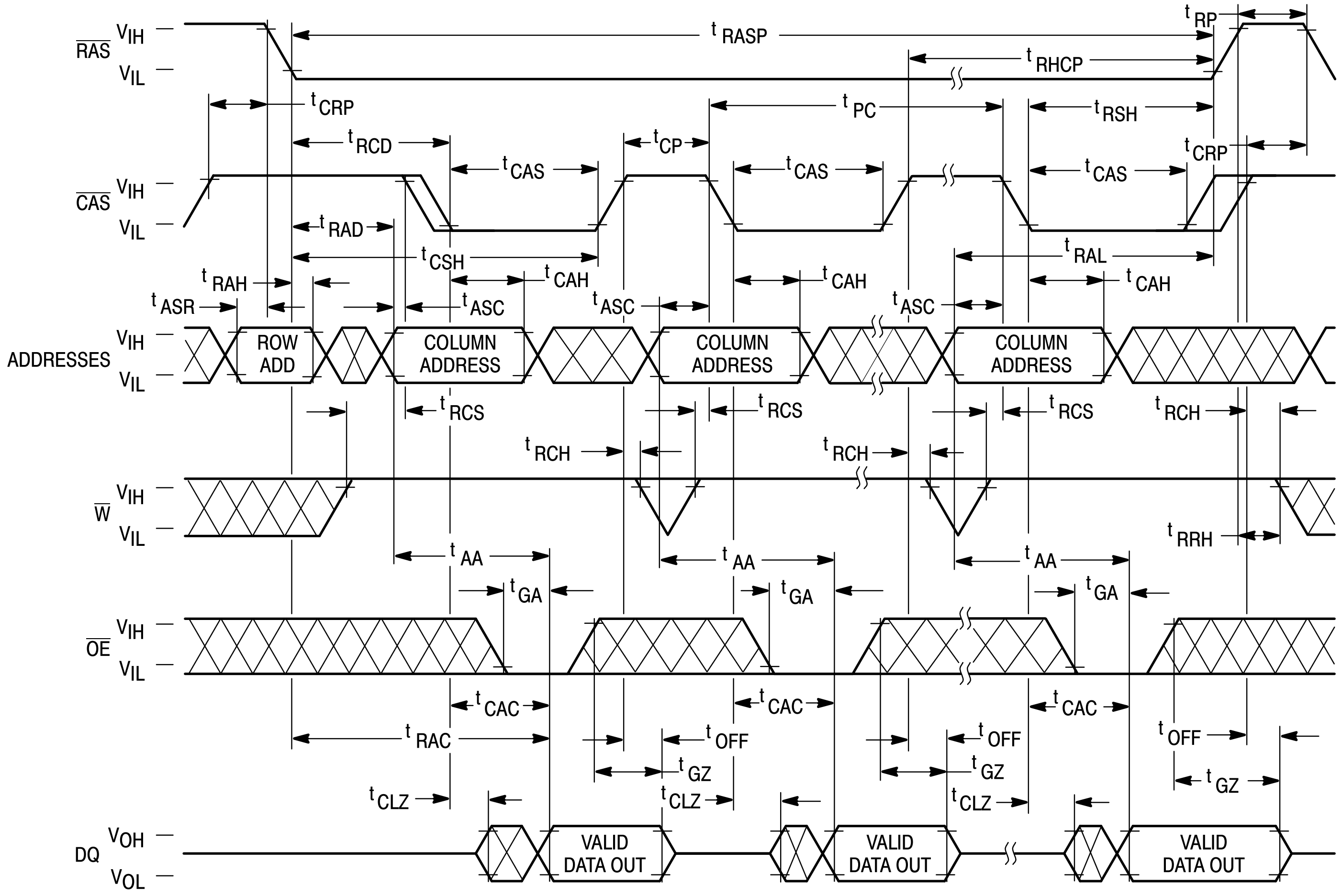
## $\overline{\text{OE}}$ CONTROLLED WRITE CYCLE



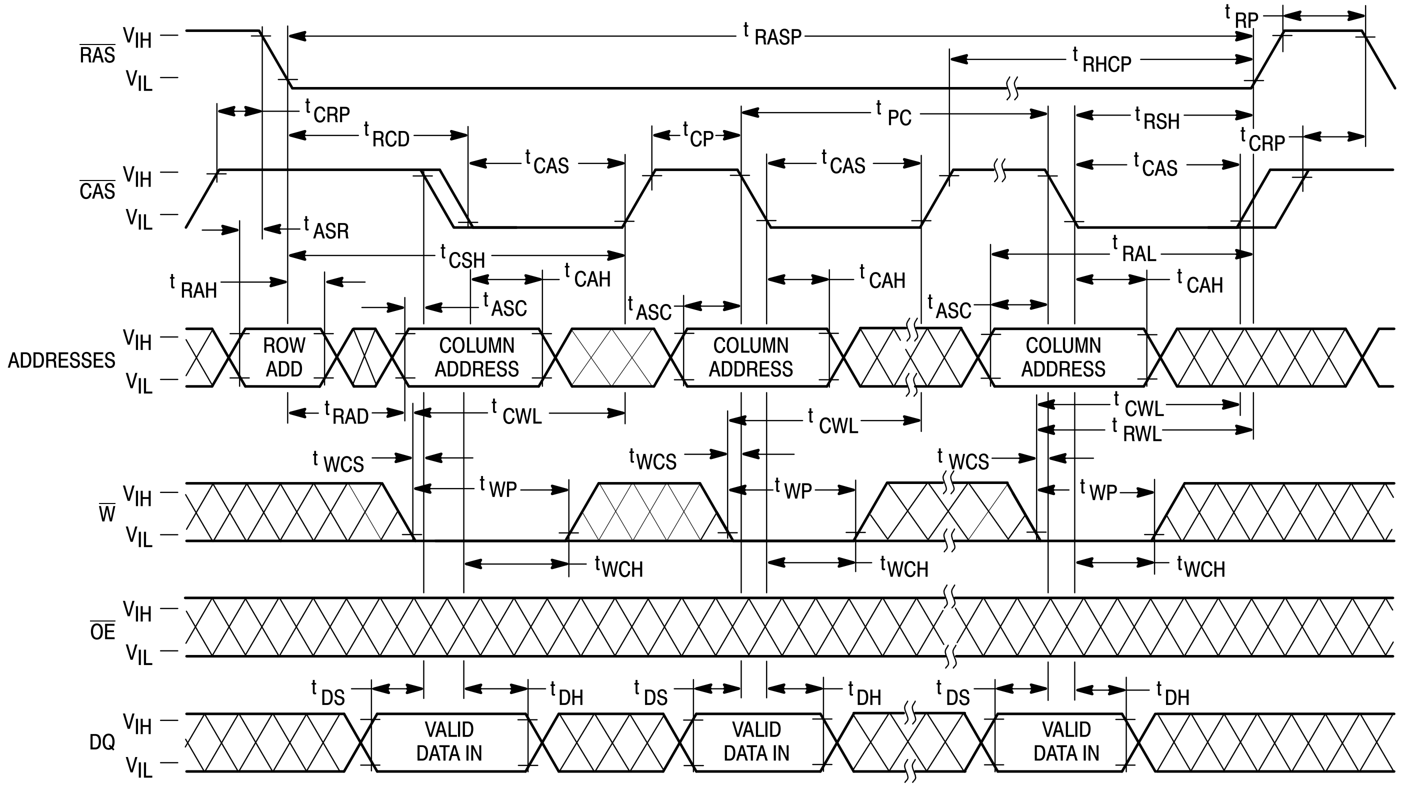
## READ-WRITE CYCLE



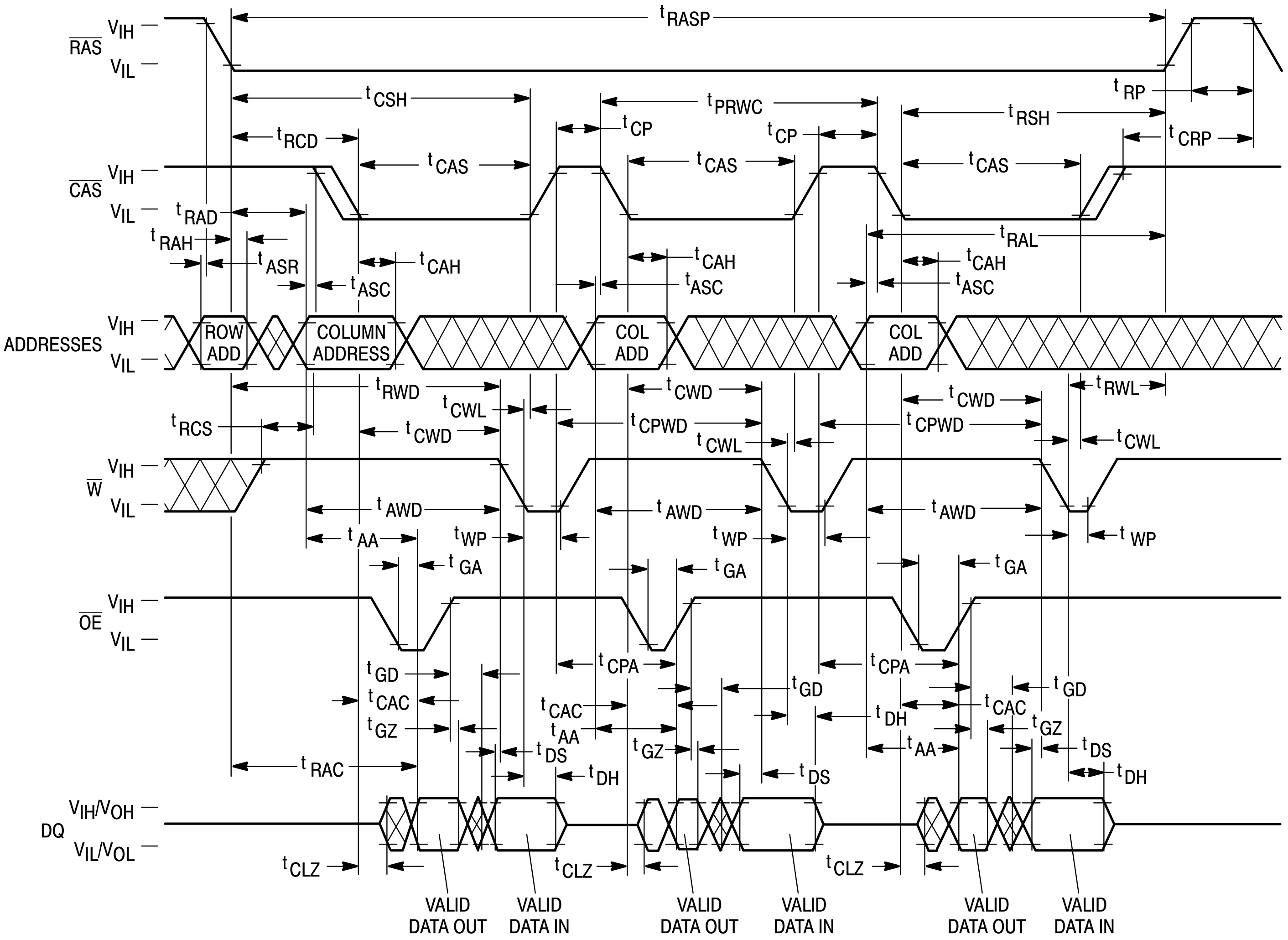
## FAST PAGE MODE READ CYCLE



## FAST PAGE MODE EARLY WRITE CYCLE

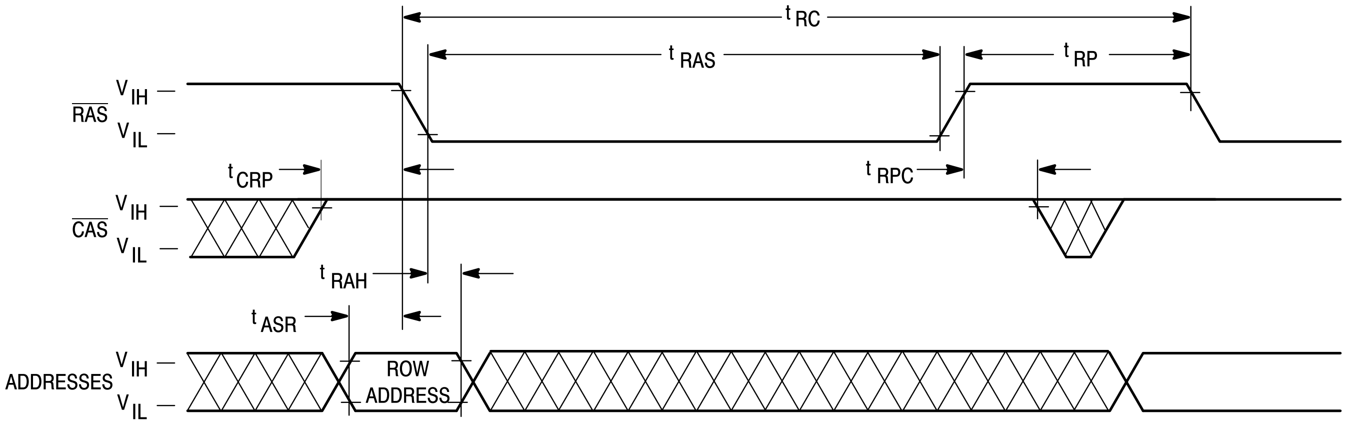


## FAST PAGE MODE READ-WRITE CYCLE



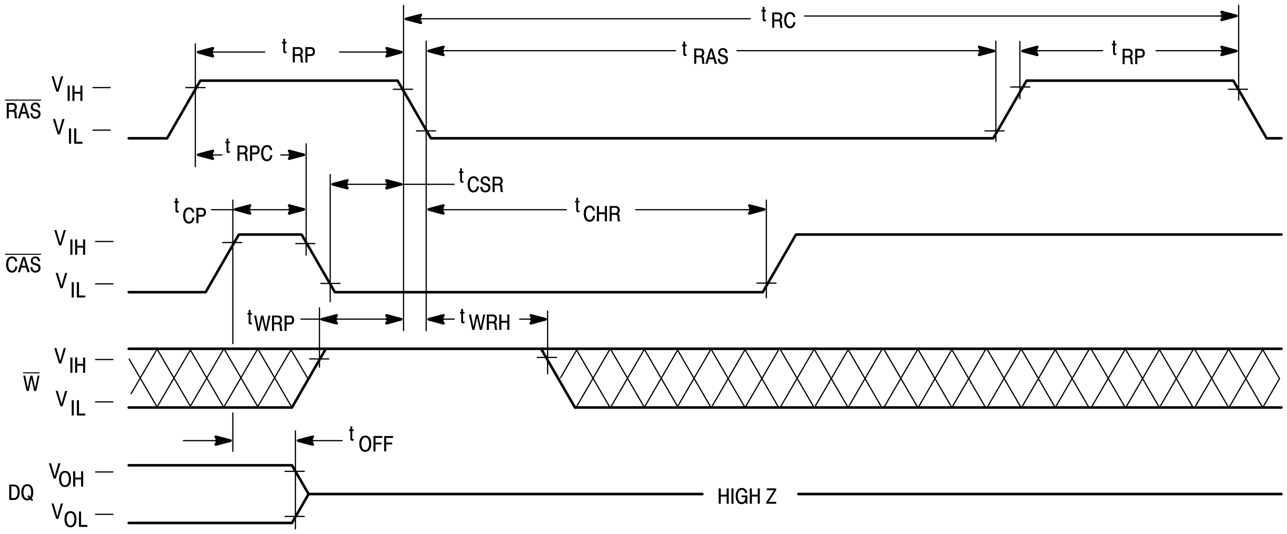
## RAS ONLY REFRESH CYCLE

**(W and OE are Don’t Care)**

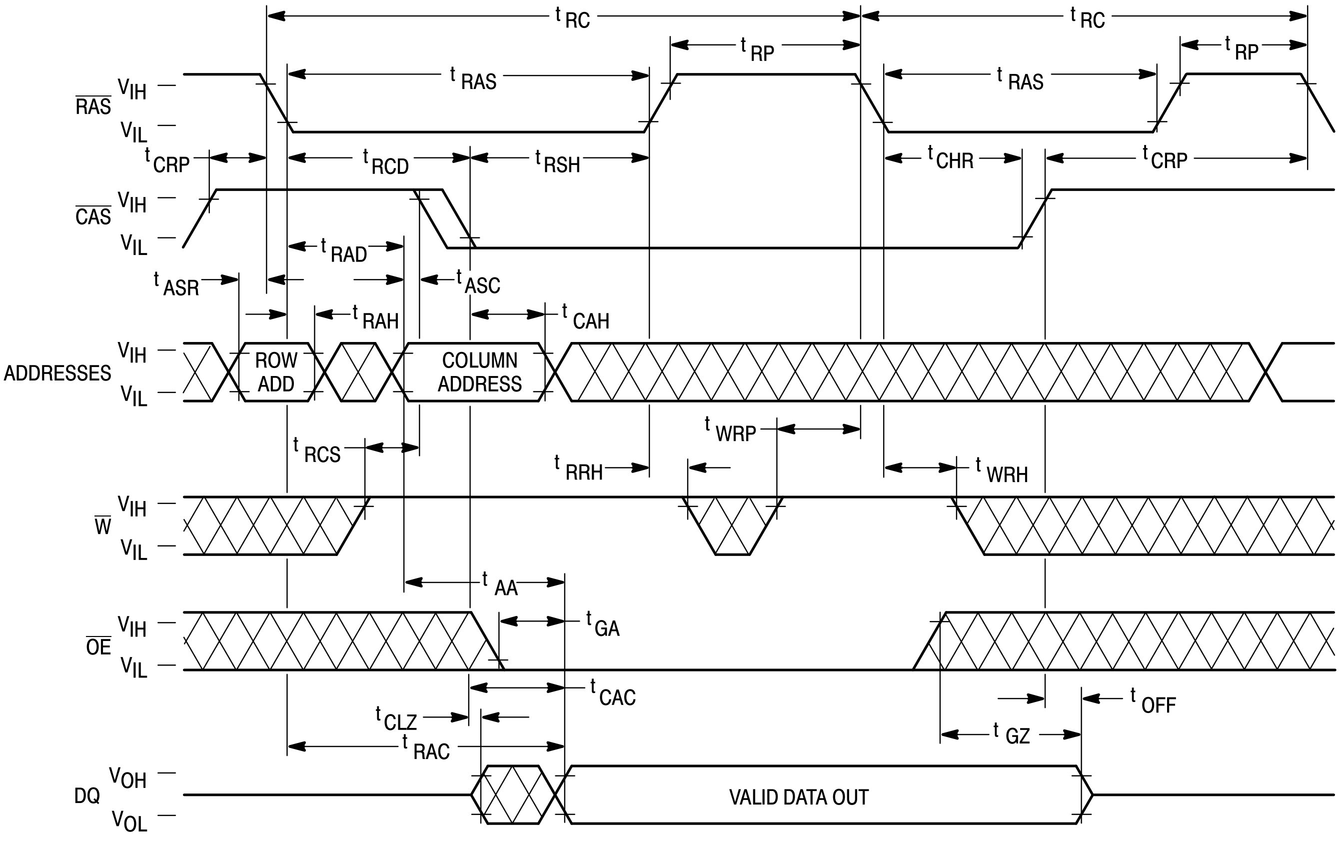


## CAS BEFORE RAS REFRESH CYCLE

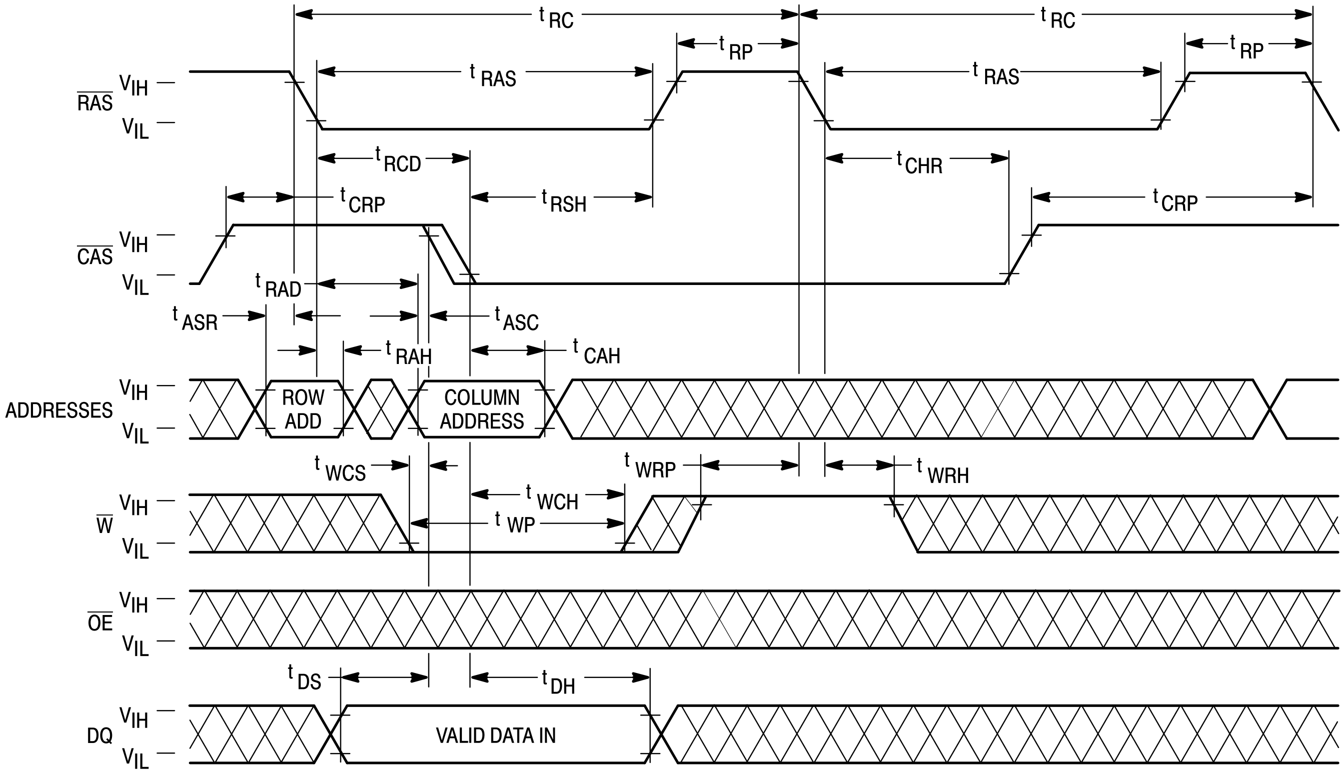
**(OE and A0 – A9 are Don’t Care)**



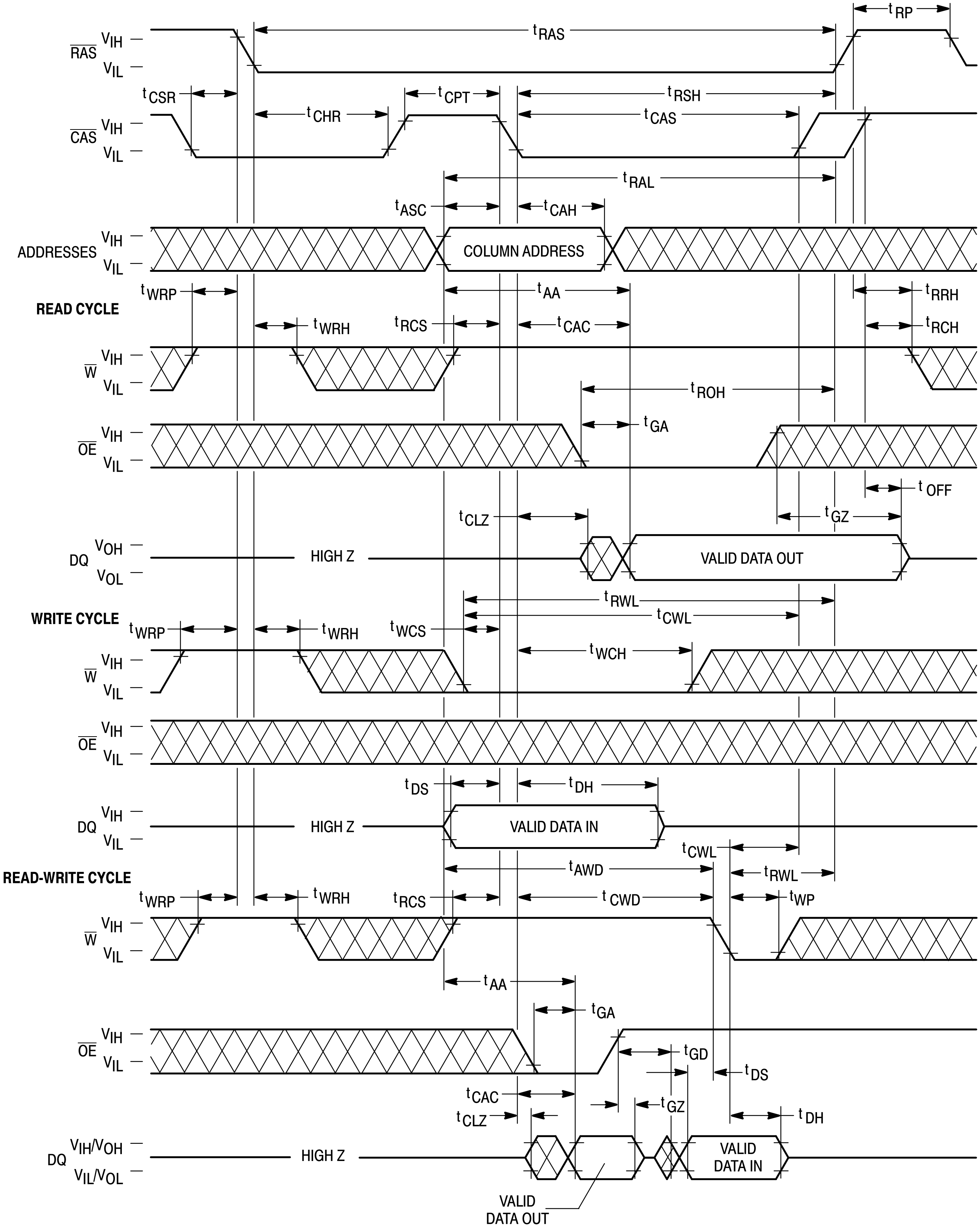
## HIDDEN REFRESH CYCLE (READ)



## HIDDEN REFRESH CYCLE (EARLY WRITE)



## $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE



## DEVICE INITIALIZATION

On power-up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 16 milliseconds or 128 milliseconds in case of low power device with the device powered up), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

## ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{\text{RAS}}$) and column address strobe ($\overline{\text{CAS}}$), into two separate 10-bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 word locations in one of the module banks. $\overline{\text{RAS}}$ active transition is followed by $\overline{\text{CAS}}$ active transition (active = $V_{IL}$, $t_{RCD}$ minimum) for all read or write cycles. The delay between $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{\text{CAS}}$ signal is ignored until an internal $\overline{\text{RAS}}$ signal is available. This "gate" feature on the external $\overline{\text{CAS}}$ clock enables the internal $\overline{\text{CAS}}$ line as soon as the row address hold time ($t_{RAH}$) specification is met (and defines $t_{RCD}$ minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{\text{CAS}}$ clock.

There are three other variations in addressing the module: **$\overline{\text{RAS}}$-only refresh cycle, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

## READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, page mode read cycle, read-write cycle, and page mode read-write cycle. The normal read cycle is outlined here, while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active transitions latching the desired bit location. The write ($\overline{\text{W}}$) input level must be high ($V_{IH}$), $t_{RCS}$ (minimum) before the $\overline{\text{CAS}}$ active transition, to enable read mode.

Both the $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. Both $\overline{\text{CAS}}$ and output enable ($\overline{\text{OE}}$) control read access time: $\overline{\text{CAS}}$ must be active before or at $t_{RCD}$ maximum and $\overline{\text{OE}}$ must be active $t_{RAC} - t_{GA}$ (both minimum) after $\overline{\text{RAS}}$ active transition to guarantee valid data out (Q) at $t_{RAC}$ (access time from $\overline{\text{RAS}}$ active transition). If the $t_{RCD}$ maximum is exceeded and/or $\overline{\text{OE}}$ active transition does not occur in time, read access time is determined by either the $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ clock active transition ($t_{CAC}$ or $t_{GA}$).

The $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must remain active for a minimum time of $t_{RAS}$ and $t_{CAS}$, respectively, to complete the read cycle. $\overline{\text{W}}$ must remain high throughout the cycle, and for time $t_{RRH}$ or $t_{RCH}$ after $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ inactive transition, respectively, to maintain the data at that bit location. Once $\overline{\text{RAS}}$ transitions to inactive, it must remain inactive for a minimum time of $t_{RP}$ to precharge the internal device circuitry for the next active cycle. Q is valid, but not latched, as long as the $\overline{\text{CAS}}$ and $\overline{\text{OE}}$ clocks are active. When either the $\overline{\text{CAS}}$ or $\overline{\text{OE}}$ clock transitions to inactive, the output will switch to High Z (three-state) $t_{OFF}$ or $t_{GZ}$ after the inactive transition.

## WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, page mode early write, and page mode read-write. Early and late write modes are discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{\text{W}}$ to active ($V_{IL}$). Early and late write modes are distinguished by the active transition of $\overline{\text{W}}$, with respect to $\overline{\text{CAS}}$. Minimum active time $t_{RAS}$ and $t_{CAS}$, and precharge time $t_{RP}$ apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{\text{W}}$ active transition at minimum time $t_{WCS}$ before $\overline{\text{CAS}}$ active transition. Data in (D) is referenced to $\overline{\text{CAS}}$ in an early write cycle. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ clocks must stay active for $t_{RWL}$ and $t_{CWL}$, respectively, after the start of the early write operation to complete the cycle.

Q remains in three-state condition throughout an early write cycle because $\overline{\text{W}}$ active transition precedes or coincides with $\overline{\text{CAS}}$ active transition, keeping data-out buffers and $\overline{\text{OE}}$ disabled.

A late write cycle (referred to as $\overline{\text{OE}}$-controlled write) occurs when $\overline{\text{W}}$ active transition is made after $\overline{\text{CAS}}$ active transition. $\overline{\text{W}}$ active transition could be delayed for almost 10 microseconds after $\overline{\text{CAS}}$ active transition, ($t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) \leq t_{RAS}$, if other timing minimums ($t_{RCD}$, $t_{RWL}$, and $t_T$) are maintained. D is referenced to $\overline{\text{W}}$ active transition in a late write cycle. Output buffers are enabled by $\overline{\text{CAS}}$ active transition but outputs are switched off by $\overline{\text{OE}}$ inactive transition, which is required to write to the device. Q may be indeterminate — see note 15 of AC Operating Conditions table. $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ must remain active for $t_{RWL}$ and $t_{CWL}$, respectively, after $\overline{\text{W}}$ active transition to complete the write cycle. $\overline{\text{OE}}$ must remain inactive for $t_{GH}$ after $\overline{\text{W}}$ active transition to complete the write cycle.

## READ-WRITE CYCLE

A read-write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{\text{W}}$ must remain high for $t_{CWD}$ minimum after the $\overline{\text{CAS}}$ active transition, to guarantee valid Q before writing the bit.

## PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the module. Read access time in page mode ($t_{CAC}$) is typically half the regular $\overline{\text{RAS}}$ clock access time, $t_{RAC}$. Page mode operation consists of keeping $\overline{\text{RAS}}$ active while toggling $\overline{\text{CAS}}$ between $V_{IH}$ and $V_{IL}$. The row is latched by $\overline{\text{RAS}}$ active transition, while each $\overline{\text{CAS}}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read-write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{\text{CAS}}$ transitions to inactive for minimum $t_{CP}$, while $\overline{\text{RAS}}$ remains low ($V_{IL}$). The second $\overline{\text{CAS}}$ active transition while $\overline{\text{RAS}}$ is low initiates the first page mode cycle ($t_{PC}$ or $t_{PRWC}$). Either a read, write, or read-write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by $t_{RASP}$. Page mode operation is ended when $\overline{\text{RAS}}$ transitions to inactive, coincident with or following $\overline{\text{CAS}}$ inactive transition.

## REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM36204 require refresh every 16 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM36204. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds on the MCM36204.

A normal read, write, or read-write operation to the RAM will refresh all the bits (4096) associated with the particular row decoded. Three other methods of refresh, **$\overline{\text{RAS}}$-only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

### $\overline{\text{RAS}}$-Only Refresh

$\overline{\text{RAS}}$-only refresh consists of $\overline{\text{RAS}}$ transition to active, latching the row address to be refreshed, while $\overline{\text{CAS}}$ remains high ($V_{IH}$) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

### $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh is enabled by bringing $\overline{\text{CAS}}$ active before $\overline{\text{RAS}}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{\text{W}}$ must be inactive for time $t_{WRP}$ before and time $t_{WRH}$ after $\overline{\text{RAS}}$ active transition to prevent switching the device into a **test mode cycle**.

### Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{\text{CAS}}$ active at the end of a read or write cycle, while $\overline{\text{RAS}}$ cycles inactive for $t_{RP}$ and back to active, starts the hidden refresh. This is essentially the execution of a $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh from a cycle in progress (see Figure 1). $\overline{\text{W}}$ is subject to the same conditions with respect to $\overline{\text{RAS}}$ active transition (to prevent test mode entry) as in $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh.

## $\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test**. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. See **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$** initialization cycles. Test procedure:

1. Write “0”s into all memory cells with normal write mode.
2. Select a column address, read “0” out and write “1” into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
3. Read the “1”s which were written in step 2 in normal read mode.
4. Using the same starting column address as in step 2, read “1” out and write “0” into the cell by performing the **$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh counter test, read-write cycle**. Repeat this operation 1024 times.
5. Read “0”s which were written in step 4 in normal read mode.
6. Repeat steps 1 to 5 using complement data.

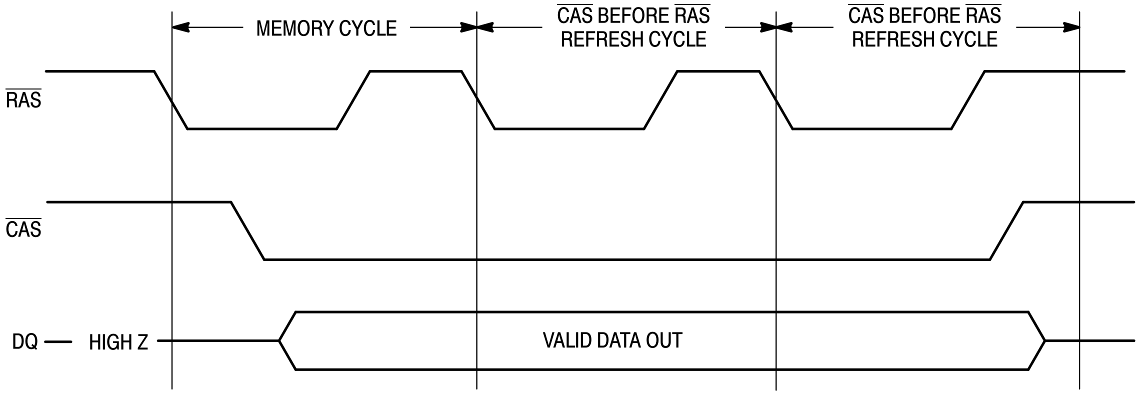


**Figure 1. Hidden Refresh Cycle**

## ORDERING INFORMATION
(Order by Full Part Number)

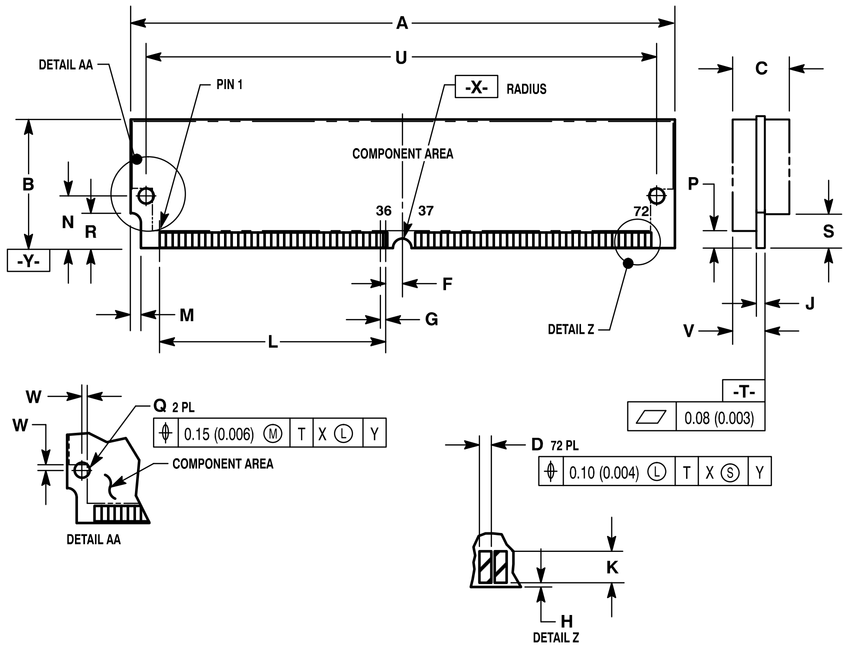
**MCM 36204 X XX**

Motorola Memory Prefix — MCM
Part Number — 36204
Package (S = SIMM, SG = Gold Pad SIMM) — X
Speed (60 = 60 ns, 70 = 70 ns) — XX

Full Part Numbers — MCM36204S60 MCM36204SG60
MCM36204S70 MCM36204SG70

## PACKAGE DIMENSIONS

### S PACKAGE
### SIMM MODULE
### CASE 866-02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 107.82 | 108.08 | 4.245 | 4.255 |
| B | 25.27 | 25.53 | 0.995 | 1.005 |
| C | — | 9.14 | — | 0.360 |
| D | 1.02 | 1.07 | 0.040 | 0.042 |
| F | 3.18 BSC | | 0.125 BSC | |
| G | 1.27 BSC | | 0.050 BSC | |
| H | — | 0.25 | — | 0.010 |
| J | 1.19 | 1.37 | 0.047 | 0.054 |
| K | 0.25 | — | 0.100 | — |
| L | 44.45 REF | | 1.750 REF | |
| M | 1.90 | 2.16 | 0.075 | 0.085 |
| N | 10.16 BSC | | 0.400 BSC | |
| P | 3.18 | — | 0.125 | — |
| Q | 3.12 | 3.22 | 0.123 | 0.127 |
| R | 6.22 | 6.48 | 0.245 | 0.255 |
| S | 5.72 | — | 0.225 | — |
| U | 101.19 BSC | | 3.984 BSC | |
| V | — | 5.28 | — | 0.208 |
| W | 1.12 | — | 0.044 | — |
| X | 1.52 | 1.63 | 0.060 | 0.064 |

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