MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

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by MCM32100D/D

MCM32100D
MCM32103D
MCM32L103D

Product Preview

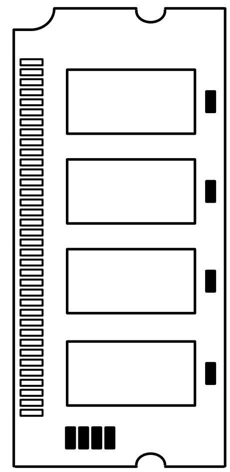
1M x 32 Bit DRAM Small Outline Memory Module

The MCM32100D is a dynamic random access memory (DRAM) module organized as 1,048,576 x 32 bits. The module is a JEDEC–standard 72–lead member of the small outline dual–in–line memory module (SO–DIMM) class of products with 36 separate contacts per side, consisting of eight MCM54400A DRAMs housed in 300 mil thin small outline packages (TSOP), mounted on a substrate along with a 0.22 µF (min) decoupling capacitor mounted adjacent to each DRAM. The MCM54400A is a 0.7µ CMOS high–speed, DRAM organized as 1,048,576 four–bit words and fabricated with CMOS silicon–gate process technology.

- Ideal for Portable System Applications
- MCM32100 Designed for Industry Standard 5 V Operation
- MCM32103 and MCM32L103 Designed for Low Voltage 3.3 V Operation
- Reduced Size (2.35″ Length) Achieved by Using Separate Front/Back Contacts
- Allows 0.227″ Three–Tiered Memory Solution When Using Horizontal Sockets
- Three–State Data Output
- Early–Write Common I/O Capability
- Fast Page Mode Capability
- TTL–Compatible Inputs and Outputs
- RAS–Only Refresh
- CAS Before RAS Refresh
- Hidden Refresh
- 1024 Cycle Refresh: 16 ms for MCM32100D and MCM32103D, 128 ms for MCM32L103D
- Consists of Eight 1M x 4 DRAMs and Eight 0.22 µF (Min) Decoupling Capacitors
- Fast Access Time (t_{RAC}): MCM32100D–60 = 60 ns (Max)
  MCM32100D–70 = 70 ns (Max)
  MCM32(L)103D–80 = 80 ns (Max)
- Low Active Power Dissipation: MCM32100D–60 = 5.28 W (Max)
  MCM32100D–70 = 4.40 W (Max)
  MCM32(L)103D–80 = 1.73 W (Max)
- Low Standby Power Dissipation:
  MCM32100D TTL Levels = 88 mW (Max)
  CMOS Levels = 44 mW (Max)
  MCM32(L)103D TTL Levels = 26.4 mW (Max)
  MCM32103D CMOS Levels = 13.2 mW (Max)
  MCM32L103D CMOS Levels = 6.6 mW (Max)

D PACKAGE
SMALL OUTLINE DIMM MODULE
MCM32100D, CASE 992–01

MCM32103D, MCM32L103D
CASE 992A–01



PIN ASSIGNMENTS

Front Side				Back Side			
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	V_{SS}	37	DQ16	2	DQ0	38	DQ17
3	DQ1	39	V_{SS}	4	DQ2	40	CAS0
5	DQ3	41	CAS2	6	DQ4	42	CAS3
7	DQ5	43	CAS1	8	DQ6	44	RAS0
9	DQ7	45	NC	10	V_{CC}	46	NC
11	PD1	47	W	12	A0	48	NC
13	A1	49	DQ18	14	A2	50	DQ19
15	A3	51	DQ20	16	A4	52	DQ21
17	A5	53	DQ22	18	A6	54	DQ23
19	NC	55	NC	20	NC	56	DQ24
21	DQ8	57	DQ25	22	DQ9	58	DQ26
23	DQ10	59	DQ28	24	DQ11	60	DQ27
25	DQ12	61	V_{CC}	26	DQ13	62	DQ29
27	DQ14	63	DQ30	28	A7	64	DQ31
29	NC	65	NC	30	V_{CC}	66	PD2
31	A8	67	PD3	32	A9	68	PD4
33	NC	69	PD5	34	RAS2	70	PD6
35	DQ15	71	PD7	36	NC	72	V_{SS}

PIN NAMES

A0 – A9 . . . . Address Inputs	DQ0 – DQ31 . Data Input/Output
CAS0 – CAS3 . . Column Address Strobe	PD1 – PD7 . . . Presence Detect
RAS0, RAS2 . . . . Row Address Strobe	W . . . . Read/Write Input
V_{CC} . . . . Power Supply	V_{SS} . . . . Ground
NC . . . . No Connection	

All power supply and ground pins must be connected for proper operation of the device.

This document contains information on a new product under development. Motorola reserves the right to change or discontinue this product without notice.

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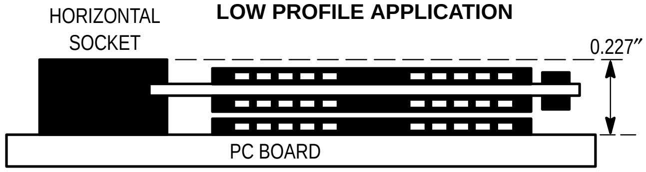
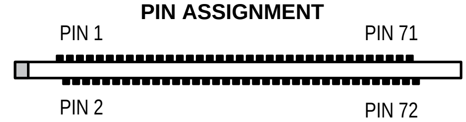
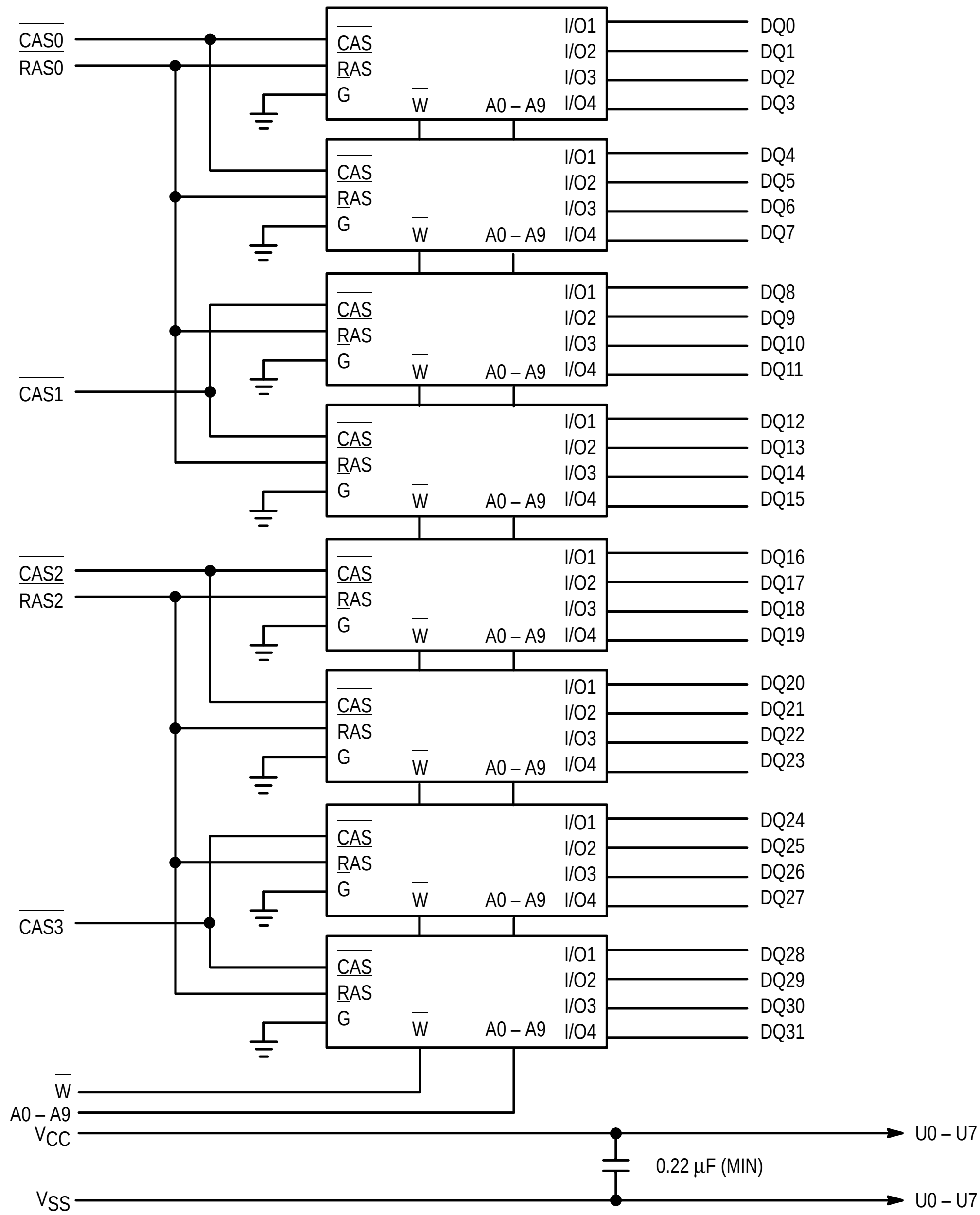
SIDE VIEW
LOW PROFILE APPLICATION



72–LEAD SMALL OUTLINE
MEMORY MODULE (SOMM)
PIN ASSIGNMENT



BLOCK DIAGRAM



PRESENCE DETECT PIN OUT			
Pin Name	**60 ns**	**70 ns**	**80 ns**
PD1	NC	NC	NC
PD2	V_{SS}	V_{SS}	V_{SS}
PD3	V_{SS}	V_{SS}	V_{SS}
PD4	NC	NC	NC
PD5	NC	V_{SS}	NC
PD6	NC	NC	V_{SS}
PD7	NC	NC	NC

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage MCM32100D MCM32103D, MCM32L103D	V_{CC}	– 1 to + 7 – 0.5 to + 4.6	V
Voltage Relative to V_{SS} (For Any Pin Except V_{CC}) MCM32100D MCM32103D, MCM32L103D	V_{in}, V_{out}	– 1 to + 7 – 0.5 to V_{CC}+ 0.5	V
Data Output Current per DQ Pin	I_{out}	50	mA
Power Dissipation	P_D	7.2	W
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high–impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(MCM32100D V_{CC} = 5.0 V ± 10%, MCM32103D, MCM32L103D V_{CC} = 3.3 V ± 0.3 V)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range) MCM32100D MCM32103D, MCM32L103D	V_{CC}	4.5 3.0	5.0 3.3	5.5 3.6	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs MCM32100D MCM32103D, MCM32L103D	V_{IH}	2.4 2.2	— —	6.5 V_{CC} + 0.3	V
Logic Low Voltage, All Inputs MCM32100D MCM32103D, MCM32L103D	V_{IL}	– 1.0 – 0.3	— —	0.8 0.6	V

DC CHARACTERISTICS AND SUPPLY CURRENTS

Characteristic	Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current MCM32100D–60, t_{RC} = 110 ns MCM32100D–70, t_{RC} = 130 ns MCM32103D–80, MCM32L103D–80, t_{RC} = 150 ns	I_{CC1}	— — —	960 800 480	mA	1, 2
V_{CC} Power Supply Current (Standby) (RAS = CAS = V_{IH}) MCM32100D MCM32103D, MCM32L103D	I_{CC2}	— —	16 8	mA	
V_{CC} Power Supply Current During RAS only Refresh Cycles MCM32100D–60, t_{RC} = 110 ns MCM32100D–70, t_{RC} = 130 ns MCM32103D–80, MCM32L103D–80, t_{RC} = 150 ns	I_{CC3}	— — —	960 800 480	mA	1, 2
V_{CC} Power Supply Current MCM32100D–60, t_{PC} = 45 ns MCM32103D–80, MCM32L103D–80, t_{PC} = 50 ns	I_{CC4}	— —	560 320	mA	1, 2
V_{CC} Power Supply Current (Standby) (RAS = CAS = V_{CC} – 0.2 V) MCM32100D MCM32103D MCM32L103D	I_{CC5}	— — —	8 4 2	mA	
V_{CC} Power Supply Current During CAS Before RAS Refresh Cycle MCM32100D–60, t_{RC} = 110 ns MCM32100D–70, t_{RC} = 130 ns MCM32103D–80, MCM32L103D–80, t_{RC} = 150 ns	I_{CC6}	— — —	960 800 480	mA	1
Input Leakage Current ($V_{SS} \le V_{in} \le V_{CC}$)	$I_{lkg(I)}$	– 80	+ 80	µA	
Output Leakage Current (CAS at Logic 1, $V_{SS} \le V_{out} \le V_{CC}$)	$I_{lkg(O)}$	– 10	10	µA	
Output High Voltage MCM32100D (I_{OH} = – 5 mA) MCM32103D, MCM32L103D (I_{OH} = – 2 mA)	V_{OH}	2.4	—	V	
Output Low Voltage MCM32100D (I_{OL} = 4.2 mA) MCM32103D, MCM32L103D (I_{OH} = 2 mA)	V_{OL}	—	0.4	V	

NOTES:
1. Current is a function of cycle rate and output loading; maximum current is measured at the fastest cycle rate with the output open.
2. Column Address can be changed once or less while RAS = V_{IL} and CAS = V_{IH}.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, MCM32100D V_{CC} = 5 V,
MCM32103D, MCM32L103D V_{CC} = 3.3 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0 – A9	C_{in}	50	pF
	W		66	
	RAS0, RAS2		38	
	CAS0 – CAS3		24	
I/O Capacitance (CAS = V_{IH} to Disable Output)	DQ0 – DQ31	$C_{I/O}$	17	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(MCM32100D V_{CC} = 5.0 V ± 10%, MCM32103D and MCM32L103D V_{CC} = 3.3 V ± 0.3 V,
T_A = 0 to 70°C, Unless Otherwise Noted)

READ AND WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM32100D–60		MCM32100D–70		MCM32103D–80 MCM32L103D–80		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	150	—	ns	5
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	45	—	45	—	50	—	ns	
Access Time from RAS	t_{RELQV}	t_{RAC}	—	60	—	70	—	80	ns	6, 7
Access Time from CAS	t_{CELQV}	t_{CAC}	—	20	—	20	—	20	ns	6, 8
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	6, 9
Access Time from Precharge CAS	t_{CEHQV}	t_{CPA}	—	40	—	40	—	45	ns	6
CAS to Output in Low–Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	6
Output Buffer and Turn–Off Delay	t_{CEHQZ}	t_{OFF}	0	20	0	20	0	20	ns	10
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	
RAS Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	60	—	ns	
RAS Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	80	10 k	ns	
RAS Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	60	200 k	70	200 k	80	200 k	ns	
RAS Hold Time	t_{CELREH}	t_{RSH}	20	—	20	—	20	—	ns	
CAS Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	80	—	ns	
CAS Precharge to RAS Hold Time	t_{CEHREH}	t_{RHCP}	40	—	40	—	45	—	ns	
CAS Pulse Width	t_{CELCEH}	t_{CAS}	20	10 k	20	10 k	20	10 k	ns	
RAS to CAS Delay Time	t_{RELCEL}	t_{RCD}	20	40	20	50	20	60	ns	11
RAS to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	15	40	ns	12

NOTES: (continued)

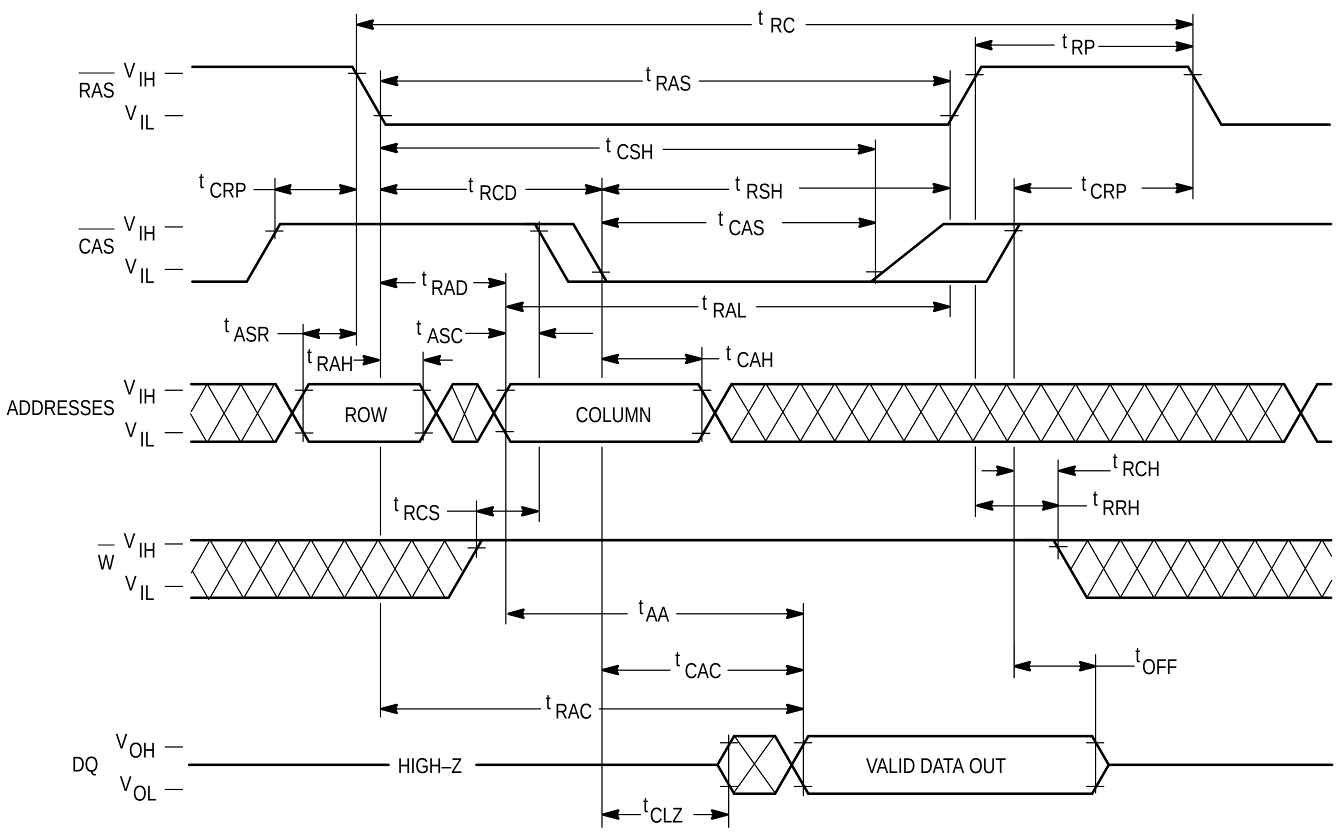
1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs for the MCM32100D and 2 ms for the MCM32103D or MCM32l102D is required after power–up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. The specification for t_{RC} (min) is used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is ensured.
6. MCM32100D measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and MCM32103D and MCM32L103D measured with a load equivalent to 100 pF and V_{OH} = 2.0 V (I_{out} = –2 mA) and V_{OL} = 0.8 V, (I_{out} = 2 mA).
7. Assumes that $t_{RCD} \le t_{RCD}$ (max).
8. Assumes that $t_{RCD} \ge t_{RCD}$ (max).
9. Assumes that $t_{RAD} \ge t_{RAD}$ (max).
10. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
11. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
12. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

READ AND WRITE CYCLES (Continued)

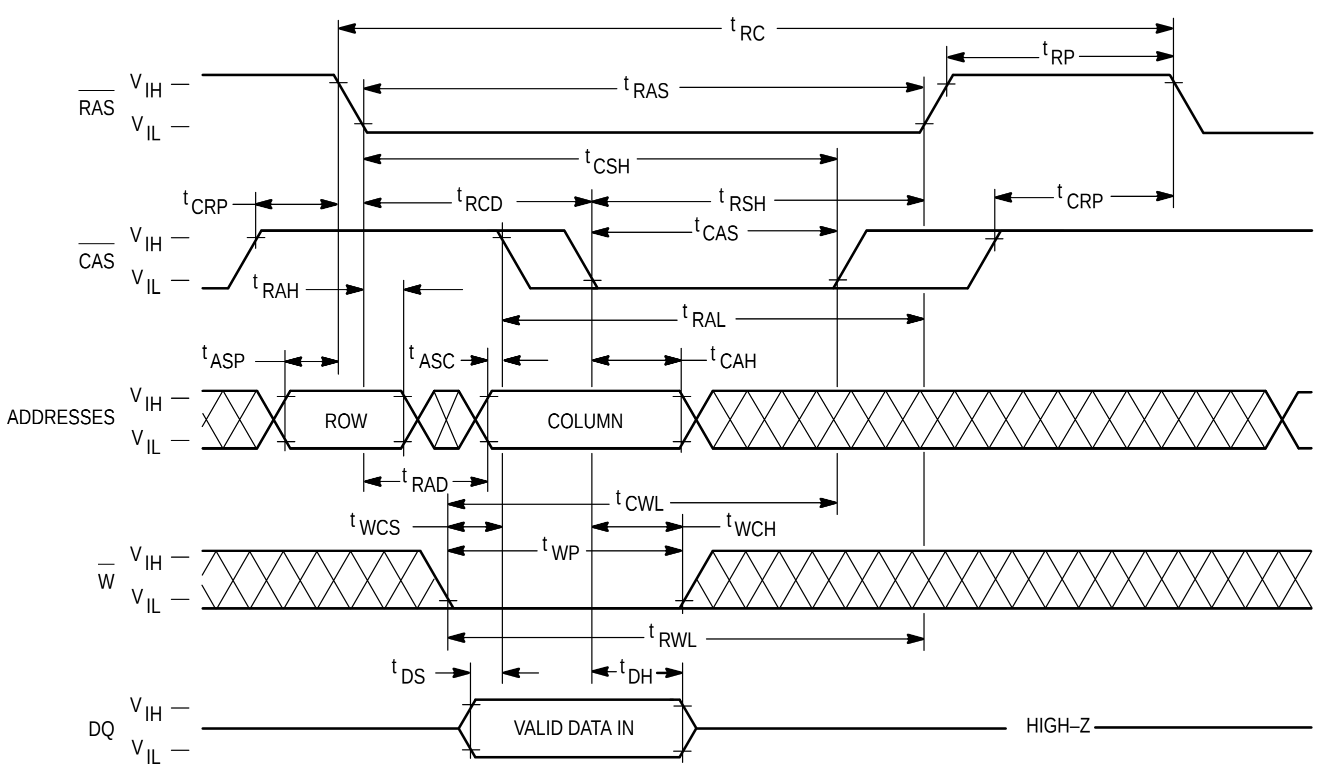
Parameter	Symbol Std	Symbol Alt	MCM32100D–60 Min	MCM32100D–60 Max	MCM32100D–70 Min	MCM32100D–70 Max	MCM32103D–80 MCM32L103D–80 Min	MCM32103D–80 MCM32L103D–80 Max	Unit	Notes
CAS to RAS Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
CAS Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	15	—	15	—	15	—	ns	
Column Address to RAS Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to CAS	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	13
Read Command Hold Time Referenced to RAS	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	13
Write Command Hold Time Referenced to CAS	t_{CELWH}	t_{WCH}	10	—	15	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	15	—	15	—	ns	
Write Command to RAS Lead Time	t_{WLREH}	t_{RWL}	20	—	20	—	20	—	ns	
Write Command to CAS Lead Time	t_{WLCEH}	t_{CWL}	20	—	20	—	20	—	ns	
Data in Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	14
Data in Hold Time	t_{CELDX}	t_{DH}	15	—	15	—	15	—	ns	14
Refresh Period MCM32L103D	t_{RVRV}	t_{RFSH}	— —	16 —	— —	16 —	— —	16 128	ms	
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	15
CAS Setup Time for CAS Before RAS Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
CAS Hold Time for CAS Before RAS Refresh	t_{RELCEH}	t_{CHR}	15	—	15	—	15	—	ns	
RAS Precharge to CAS Active Time	t_{REHCEL}	t_{RPC}	0	—	0	—	0	—	ns	
CAS Precharge Time for CAS Before RAS Counter Time	t_{CEHCEL}	t_{CPT}	30	—	40	—	40	—	ns	
Write to RAS Precharge Time (CAS Before RAS Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	10	—	ns	
Write to RAS Hold Time (CAS Before RAS Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	10	—	ns	

NOTES:
13. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
14. These parameters are referenced to CAS leading edge in random write cycles.
15. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as an electrical characteristic only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If this condition is not satisifed, the condition of the data out (at access time) is indeterminate.

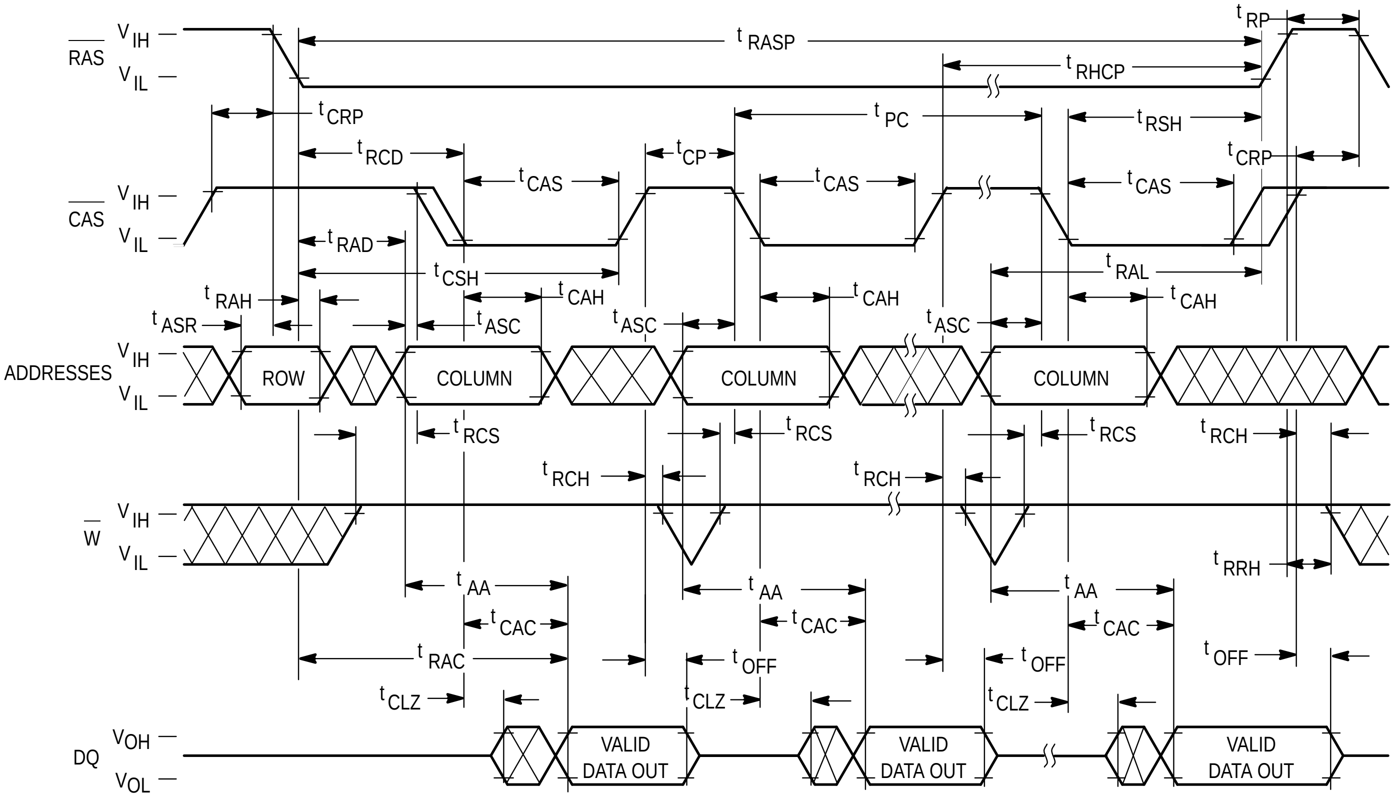
READ CYCLE



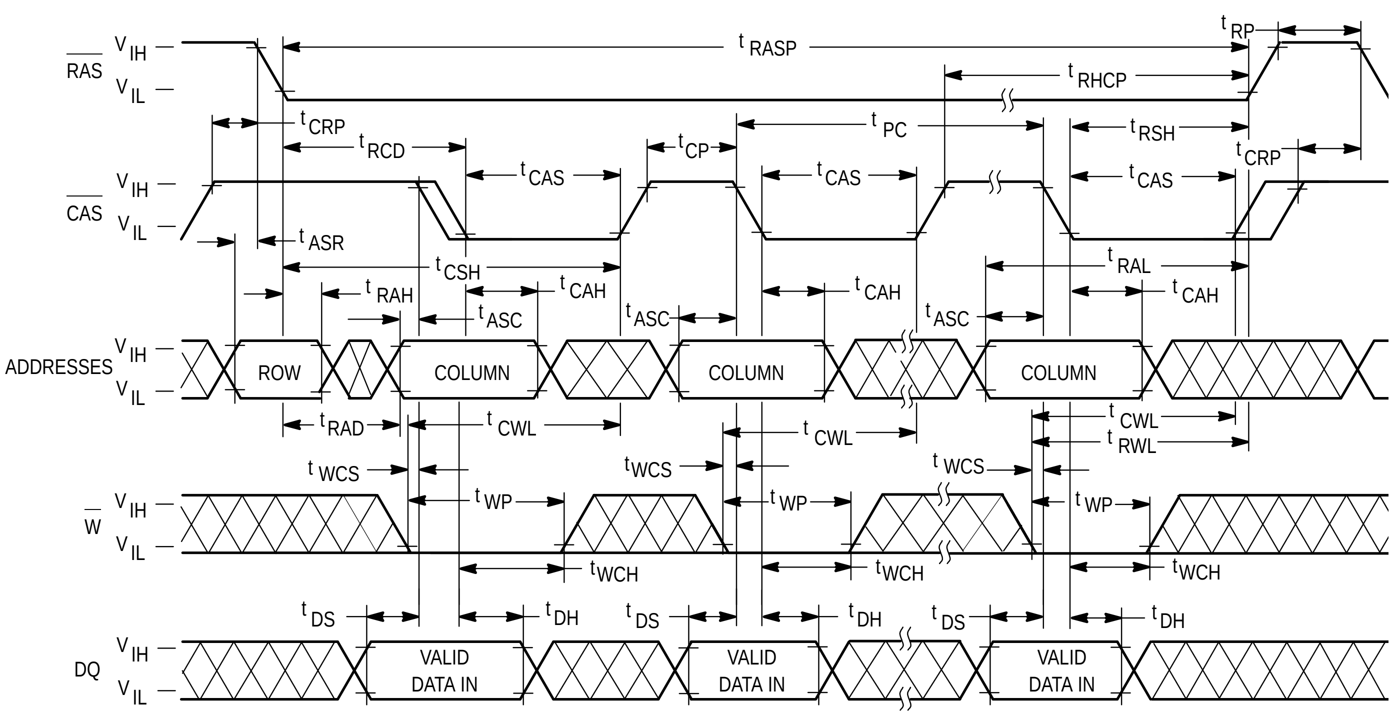
EARLY WRITE CYCLE



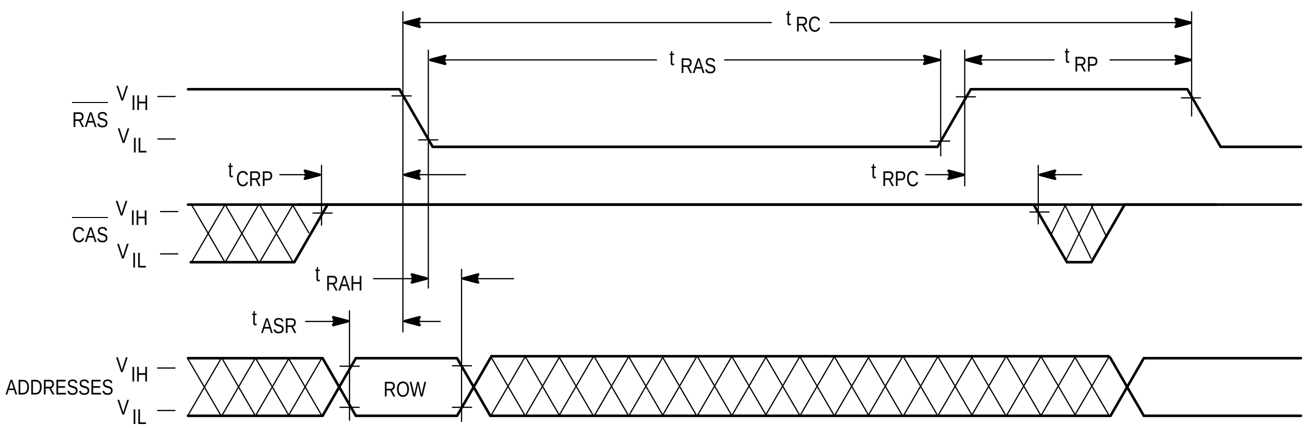
FAST PAGE MODE READ CYCLE



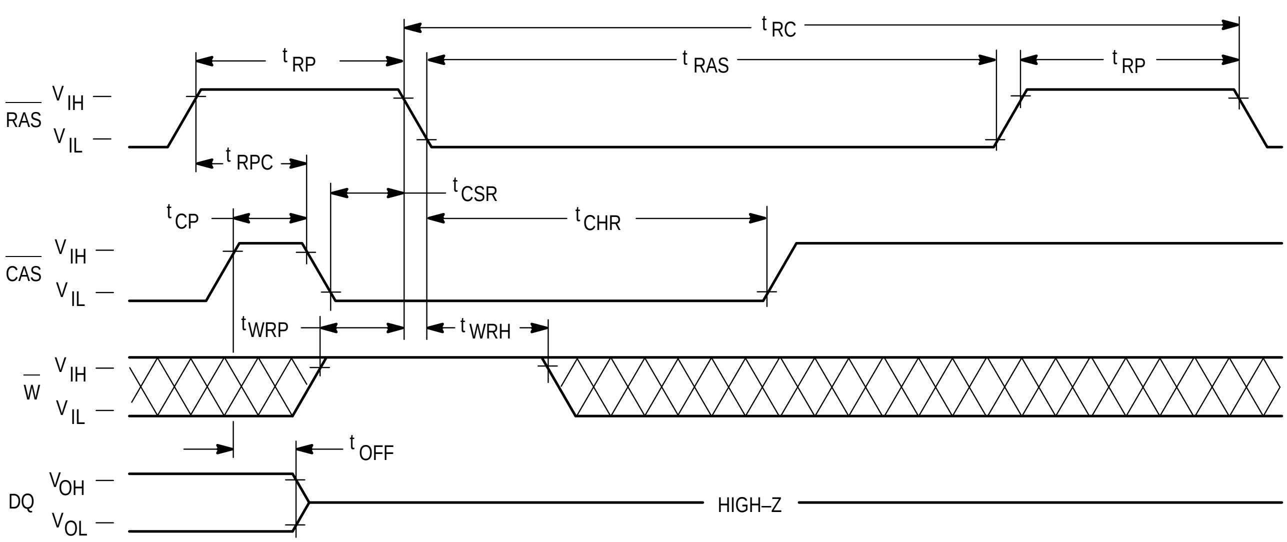
FAST PAGE MODE EARLY WRITE CYCLE



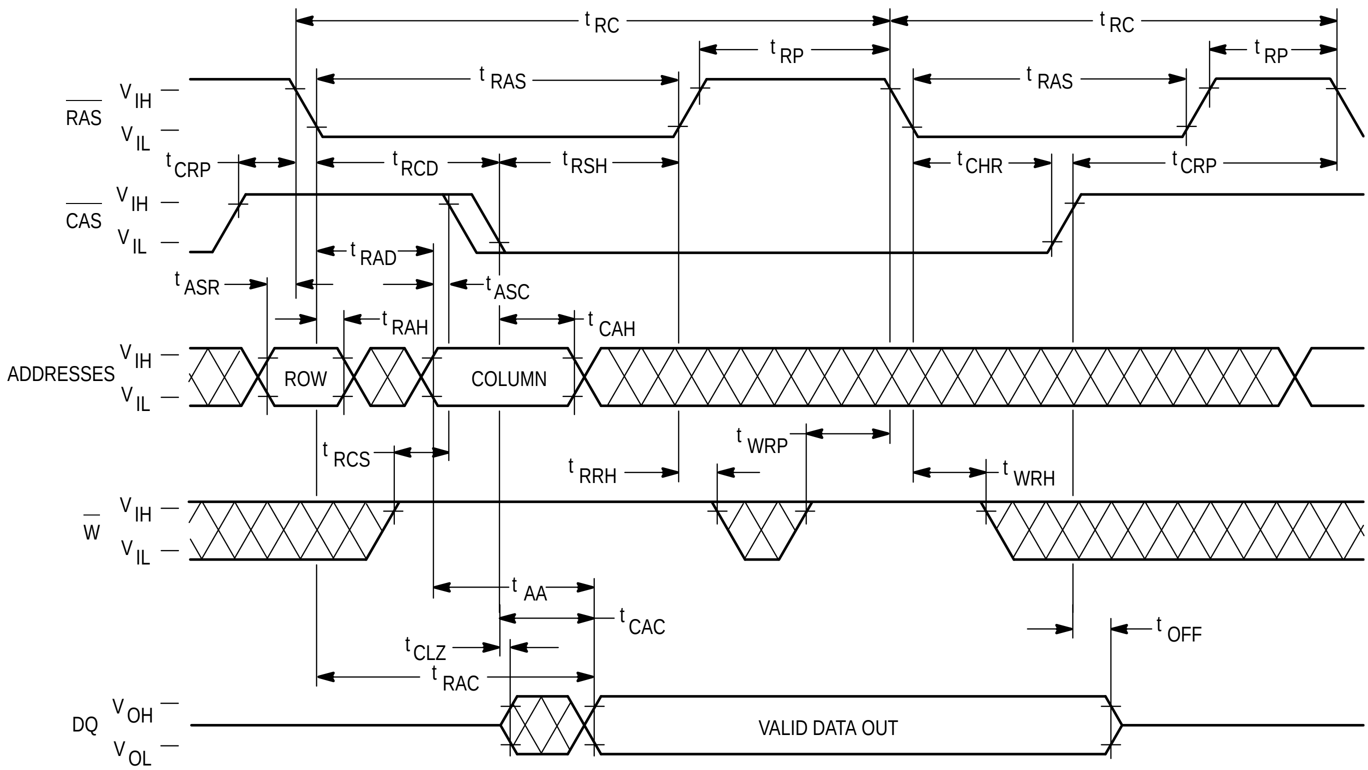
RAS ONLY REFRESH CYCLE
(W is Don't Care)



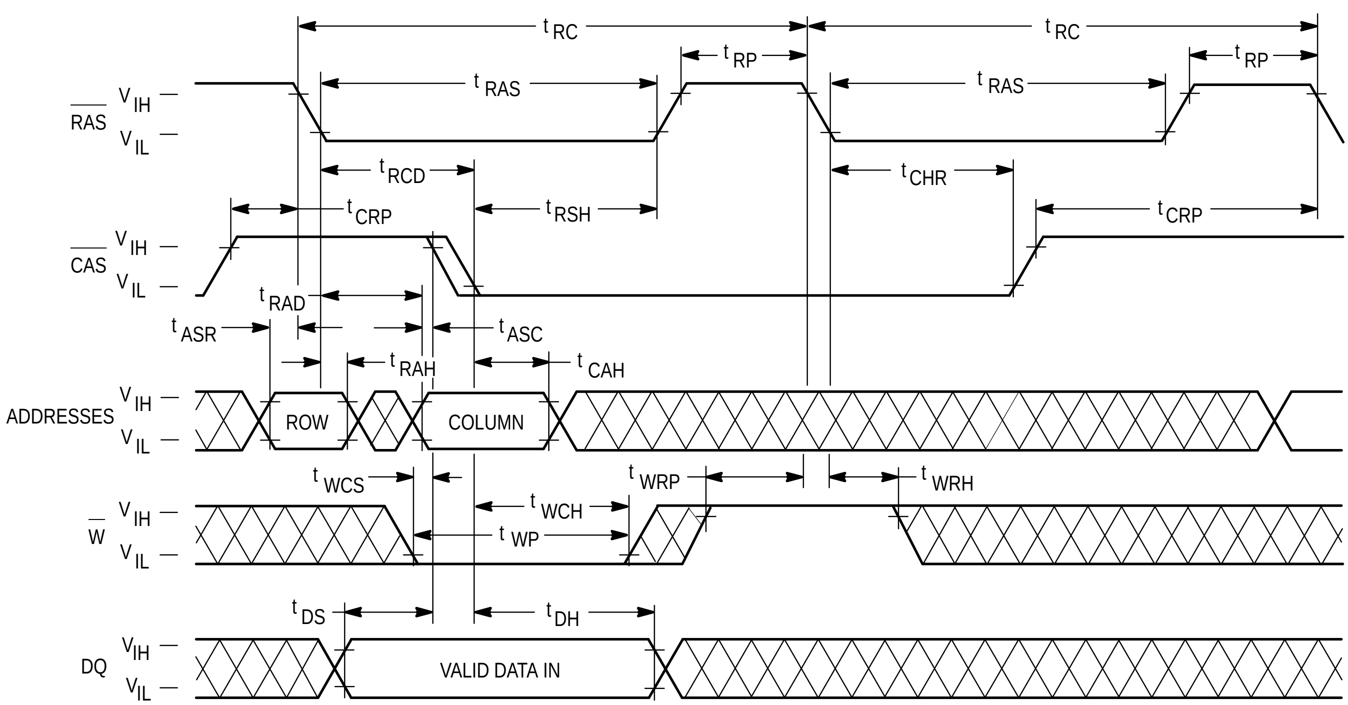
CAS BEFORE RAS REFRESH CYCLE
(A0 – A9 are Don't Care)



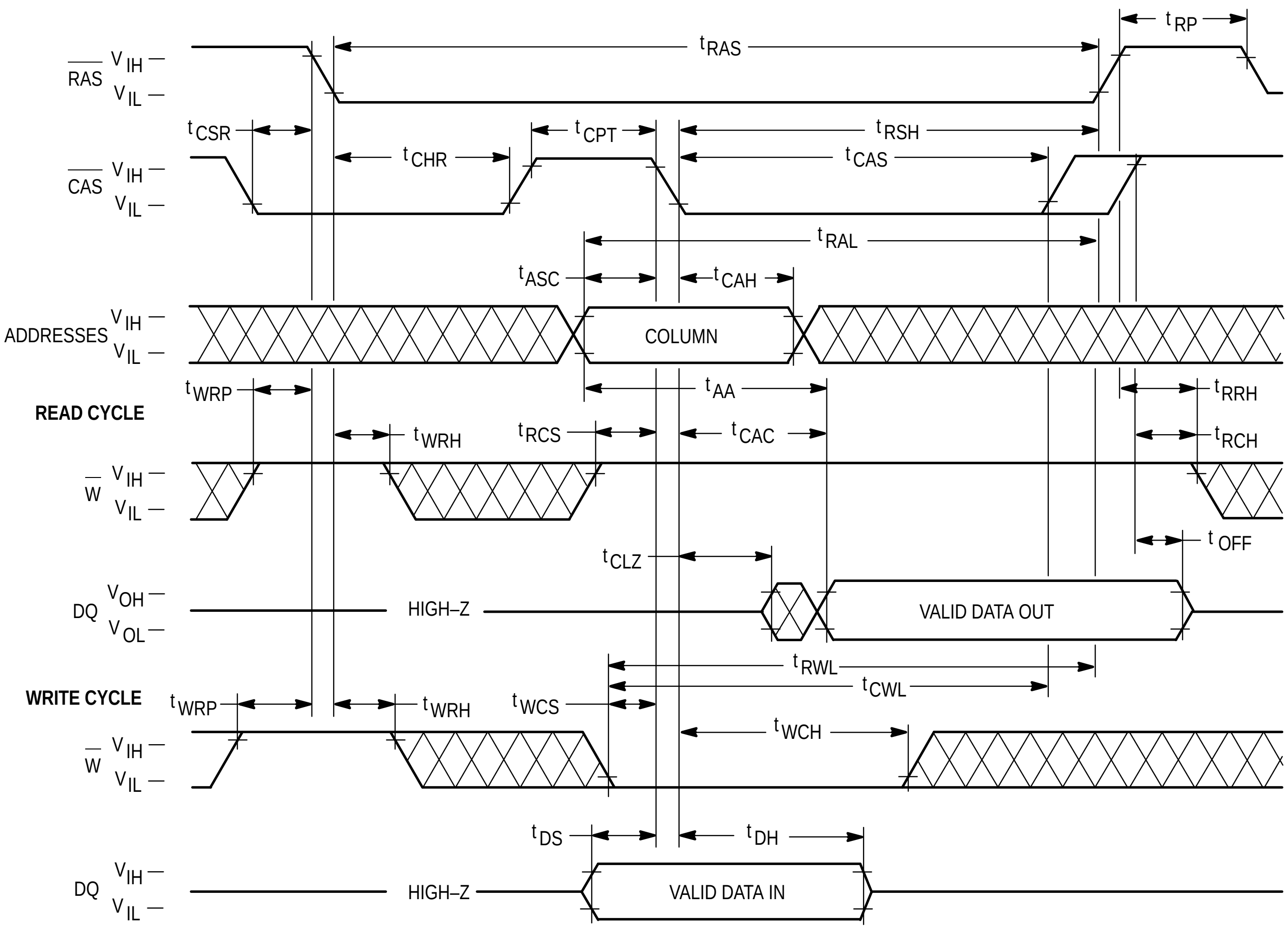
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power–up, an initial pause of 200 microseconds for the MCM32100D or two milliseconds for the MCM32103D and MCM32L103D is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the module. During an extended inactive state (greater than 16 milliseconds for the MCM32100D or MCM32103D and greater than 128 milliseconds for MCM32L103D with the device powered up), a wake up sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

The ten address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe (RAS) and column address strobe (CAS), into two separate 10–bit address fields. A total of twenty address bits, ten rows and ten columns, will decode one of the 1,048,576 word locations in the device. RAS active transition is followed by CAS active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between RAS and CAS active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external CAS signal is ignored until an internal RAS signal is available. This "gate" feature on the external CAS clock enables the internal CAS line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the CAS clock.

There are three other variations in addressing the module: **RAS only refresh cycle, CAS before RAS refresh cycle,** and **page mode**. All three are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with either a "normal" random read cycle or a page mode read cycle. The normal read cycle is outlined here, while the page mode cycle is discussed in a separate section.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with RAS and CAS active transitions latching the desired bit location. The write (W) input level must be high (V_{IH}), t_{RCS} (minimum) before the CAS active transition, to enable read mode.

Both the RAS and CAS clocks trigger a sequence of events which are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window. CAS controls read access time: CAS must be active before or at t_{RCD} maximum to guarantee valid data out (DQ) at t_{RAC} (access time from RAS active transition). If the t_{RCD} maximum is exceeded, read access time is determined by the CAS clock active transition (t_{CAC}).

The RAS and CAS clocks must remain active for a minimum time of t_{RAS} and t_{CAS} respectively, to complete the read cycle. W must remain high throughout the cycle, and for time t_{RRH} or t_{RCH} after RAS or CAS inactive transition, re–spectively, to maintain the data at that bit location. Once RAS transitions to inactive, it must remain inactive for a minimum time of t_{RP} to precharge the internal device circuitry for the next active cycle. DQ is valid, but not latched, as long as the CAS clock is active. When the CAS clock transitions to inactive, the output will switch to High–Z (three–state) t_{OFF} after the inactive transition.

WRITE CYCLE

The user can write to the DRAM with either an early write or a page mode early write cycle. Early write mode is discussed here, while page mode write operations are covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of W to active (V_{IL}). Early write mode is distinguished by the active transition of W, with respect to CAS. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP} apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before CAS active transition. Data in (DQ) is referenced to CAS in an early write cycle. RAS and CAS clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all 1024 column locations on a selected row of the module. Read access time in page mode (t_{CAC}) is typically half the regular RAS clock access time, t_{RAC}. Page mode operation consists of keeping RAS active while toggling CAS between V_{IH} and V_{IL}. The row is latched by RAS active transition, while each CAS active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read or write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, CAS transitions to inactive for minimum t_{CP}, while RAS remains low (V_{IL}). The second CAS active transition while RAS is low initiates the first page mode cycle (t_{PC}). Either a read or write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when RAS transitions to inactive, coincident with or following CAS inactive transition.

REFRESH CYCLES

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM32100D or MCM32103D require refresh every 16 milliseconds. Bits in the MCM32L103D require refresh every 128 milliseconds.

This is accomplished by cycling through the 1024 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the MCM32100D or MCM32103D and every 124.8 microseconds for the MCM32L103D. Burst refresh, a refresh of all 1024 rows consecutively, must be performed every 16 milliseconds for the MCM32100D or

MCM32103D and every 128 milliseconds for the MCM32L103D.

A normal read or write operation to the RAM will refresh all the bits associated with the particular row decoded. Three other methods of refresh, **RAS–only refresh, CAS before RAS refresh,** and **hidden refresh** are available on this device for greater system flexibility.

RAS–Only Refresh

RAS–only refresh consists of RAS transition to active, latching the row address to be refreshed, while CAS remains high (V_{IH}) throughout the cycle. An external counter is employed to ensure all rows are refreshed within the specified limit.

CAS Before RAS Refresh

CAS before RAS refresh is enabled by bringing CAS active before RAS. This clock order actives an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). W must be inactive for time t_{WRP} before and time t_{WRH} after RAS active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding CAS active at the end of a read or write cycle, while RAS cycles inactive for t_{RP} and back to active, starts the hidden refresh. This is essentially the execution of a CAS before RAS refresh from a cycle in progress (see Figure 1). W is subject to the same conditions with respect to RAS active transition (to prevent test mode cycle) as in CAS before RAS refresh.

CAS BEFORE RAS REFRESH COUNTER TEST

The internal refresh counter of the device can be tested with a **CAS before RAS refresh counter test**. This refresh counter test is performed with read and write operations. During this test, the internal refresh counter generates the row address, while the external address input supplies the column address. The entire array is refreshed after 1024 test cycles, as indicated by the check data written in each row. See **CAS before RAS refresh counter test cycle** timing diagram.

The test can be performed only after a minimum of **8 CAS before RAS** initialization cycles. The test procedure is as follows:

1. Write 0s into all memory cells (normal write mode).
2. Select a column address, and read 0 out of the cell by performing **CAS before RAS refresh counter test, read cycle**. Repeat this operation 1024 times.
3. Select a column address, and write 1 into the cell by performing **CAS before RAS refresh counter test, write cycle**. Repeat this operation 1024 times.
4. Read 1s (normal read mode), which were written at step three.
5. Repeat steps one through four using complement data.

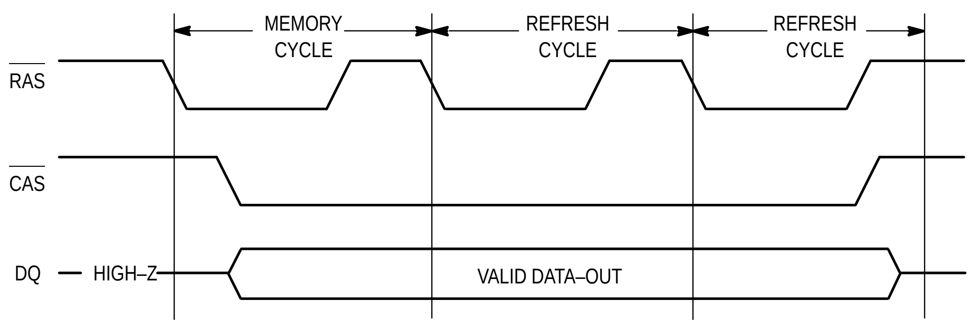
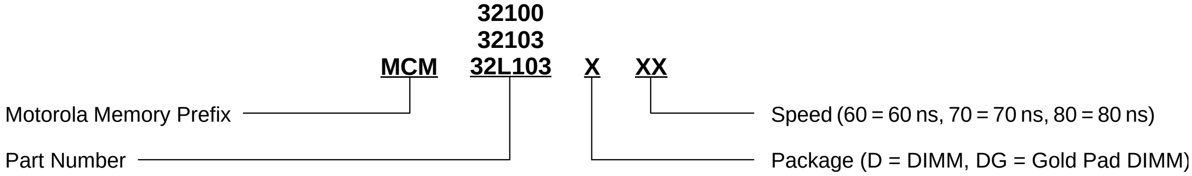


Figure 1. Hidden Refresh Cycle

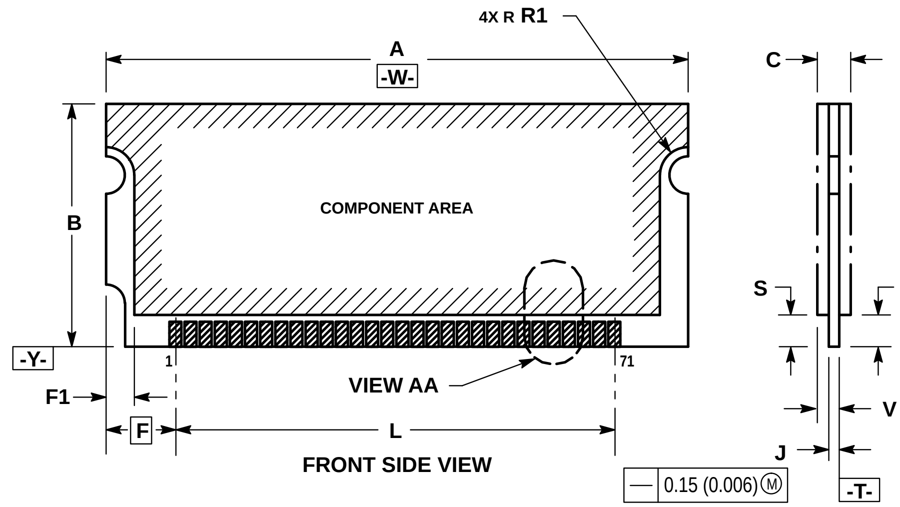
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM32100D60 MCM32100DG60
MCM32100D70 MCM32100DG70
MCM32103D80 MCM32103DG80
MCM32L103D80 MCM32L103DG80

PACKAGE DIMENSIONS

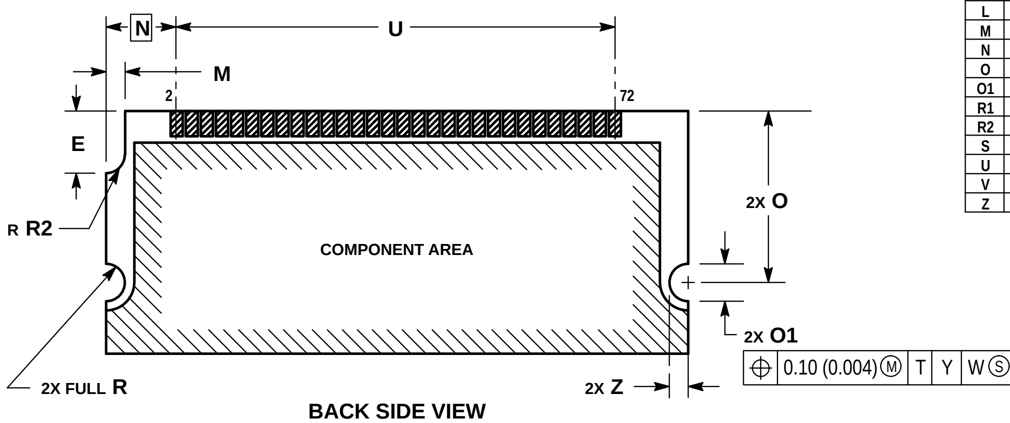
D PACKAGE
SMALL OUTLINE DIMM MODULE
CASE 992–01



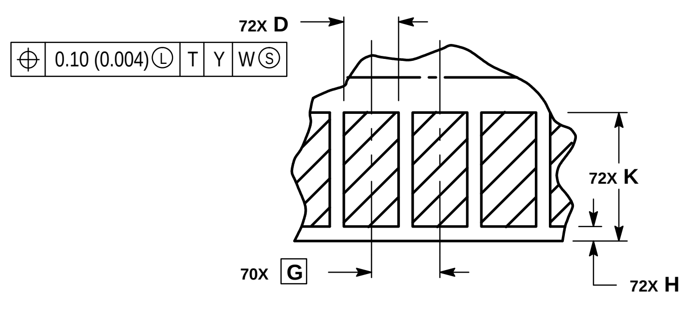
FRONT SIDE VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALIZATION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	59.56	59.82	2.346	2.355
B	25.27	25.53	0.995	1.005
C	—	3.80	—	0.150
D	0.95	1.05	0.037	0.041
E	6.22	6.48	0.245	0.255
F	7.62 BSC		0.300 BSC	
F1	3.00	—	0.118	—
G	1.27 BSC		0.050 BSC	
H	—	0.25	—	0.010
J	0.90	1.10	0.035	0.043
K	2.54	—	0.100	—
L	44.45 REF		1.750 REF	
M	1.87	2.13	0.074	0.084
N	8.25 BSC		0.325 BSC	
O	17.78 BSC		0.700 BSC	
O1	3.90	4.10	0.154	0.161
R1	2.87	3.13	0.113	0.123
R2	1.87	2.13	0.074	0.084
S	3.18	—	0.125	—
U	44.45 REF		1.750 REF	
V	—	2.45	—	0.096
Z	2.00	—	0.079	—



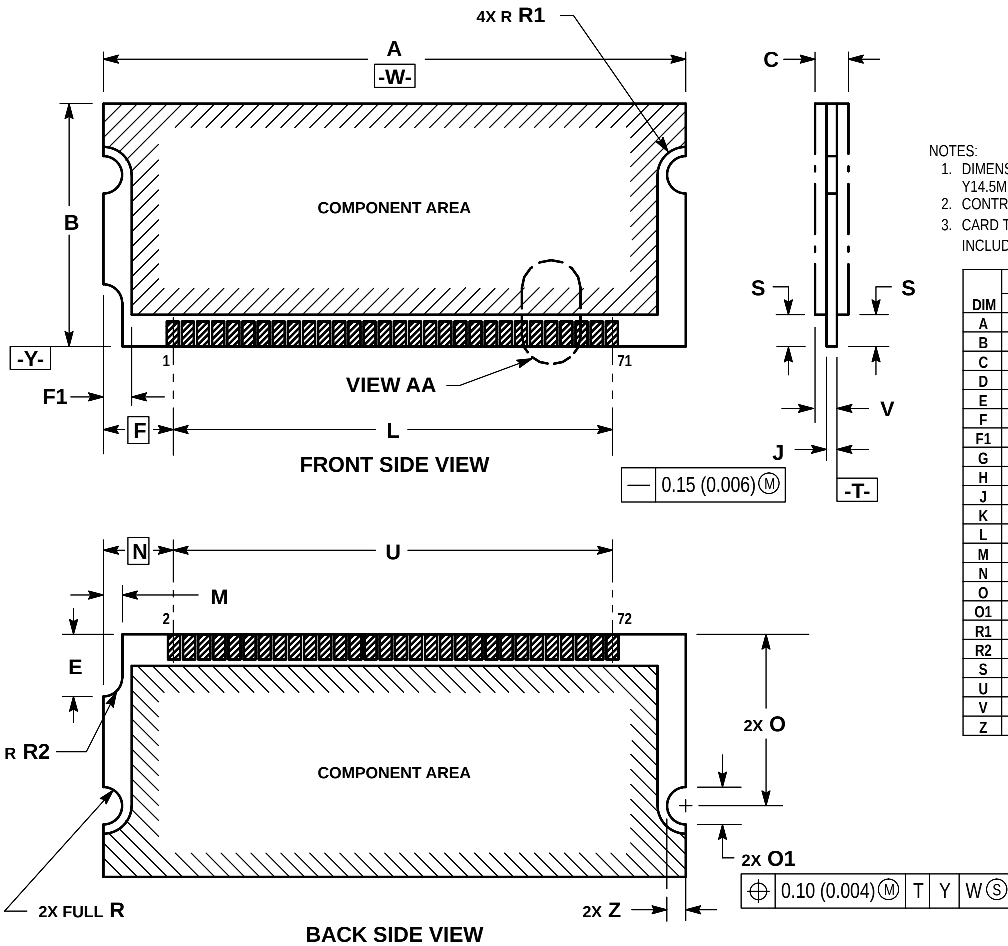
BACK SIDE VIEW



VIEW AA

PACKAGE DIMENSIONS

DG PACKAGE
SMALL OUTLINE DIMM MODULE
CASE 992A–01



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F1	3.00	—	0.118	—
G	1.27 BSC		0.050 BSC	
H	—	0.25	—	0.010
J	0.90	1.10	0.035	0.043
K	2.54	—	0.100	—
L	44.45 REF		1.750 REF	
M	1.87	2.13	0.074	0.084
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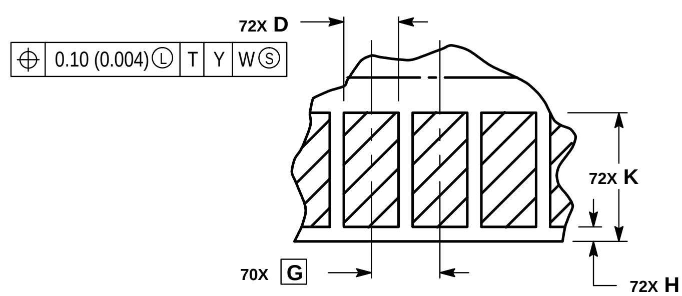

VIEW AA

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