Phase-Frequency Detector

MCH12140
MCK12140

PHASE–FREQUENCY DETECTOR

The MCH/K12140 is a phase frequency-detector intended for phase-locked loop applications which require a minimum amount of phase and frequency difference at lock. When used in conjunction with the MC12147, MC12148 or MC12149 VCO, a high bandwidth PLL can be realized. The device is functionally compatible with the MC12040 phase-frequency detector, however the MOSAIC™ III process is used to push the maximum frequency to 800MHz and significantly reduce the dead zone of the detector. When the Reference (R) and VCO (V) inputs are unequal in frequency and/or phase, the differential UP (U) and DOWN (D) outputs will provide pulse streams which when subtracted and integrated provide an error voltage for control of a VCO.

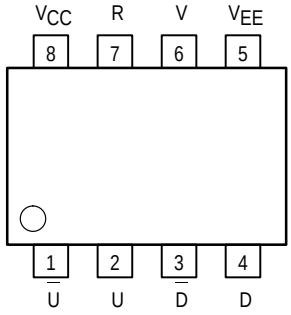
The device is packaged in a small outline, surface mount 8-lead SOIC package. There are two versions of the device to provide I/O compatibility to the two existing ECL standards. The MCH12140 is compatible with MECL10H™ logic levels while the MCK12140 is compatible to 100K ECL logic levels. This device can also be used in +5V systems. Please refer to Motorola Application Note AN1406/D, “Designing with PECL (ECL at +5.0V)” for more information.

- 800MHz Typical Bandwidth
- Small Outline 8-Lead SOIC Package
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection

For proper operation, the input edge rate of the R and V inputs should be less than 5ns.

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-05

Pinout: 8-Lead SOIC (Top View)



TRUTH TABLE*

Input		Output				Input		Output			
R	**V**	**U**	**D**	$\overline{\textbf{U}}$	$\overline{\textbf{D}}$	**R**	**V**	**U**	**D**	$\overline{\textbf{U}}$	$\overline{\textbf{D}}$
0	0	X	X	X	X	1	1	0	0	1	1
0	1	X	X	X	X	1	0	0	0	1	1
1	1	X	X	X	X	1	1	0	1	1	0
0	1	X	X	X	X	1	0	0	1	1	0
1	1	1	0	0	1	1	1	0	1	1	0
0	1	1	0	0	1	0	1	0	1	1	0
1	1	1	0	0	1	1	1	0	0	1	1
1	0	1	0	0	1						

* This is not strictly a functional table; i.e., it does not cover all possible modes of operation. However, it gives a sufficient number of tests to ensure that the device will function properly.

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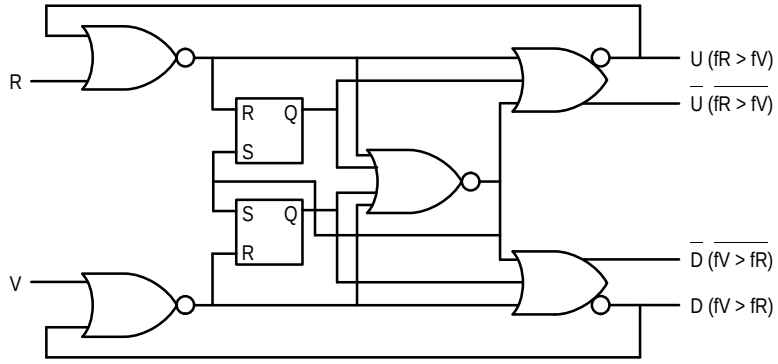
LOGIC DIAGRAM



H–SERIES DC CHARACTERISTICS (V_{EE} = V_{EE}(min) – V_{EE}(max); V_{CC} = GND[1])

Symbol	Characteristic	–40°C		0°C		25°C		70°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	–1080	–890	–1020	–840	–980	–810	–910	–720	mV
V_{OL}	Output LOW Voltage	–1950	–1650	–1950	–1630	–1950	–1630	–1950	–1595	mV
V_{IH}	Input HIGH Voltage	–1230	–890	–1170	–840	–1130	–810	–1060	–720	mV
V_{IL}	Input LOW Voltge	–1950	–1500	–1950	–1480	–1950	–1480	–1950	–1445	mV
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	0.3	—	µA

1. 10H circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.

K–SERIES DC CHARACTERISTICS (V_{EE} = V_{EE}(min) – V_{EE}(max); V_{CC} = GND[1])

Symbol	Characteristic	–40°C			0°C to 70°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max		
V_{OH}	Output HIGH Voltage	–1085	–1005	–880	–1025	–955	–880	mV	V_{IN} = V_{IH}(max)
V_{OL}	Output LOW Voltage	–1830	–1695	–1555	–1810	–1705	–1620	mV	or V_{IL}(min)
V_{OHA}	Output HIGH Voltage	–1095	—	—	–1035	—	—	mV	V_{IN} = V_{IH}(min)
V_{OLA}	Output LOW Voltage	—	—	–1555	—	—	–1610	mV	or V_{IL}(max)
V_{IH}	Input HIGH Voltage	–1165	—	–880	–1165	—	–880	mV	
V_{IL}	Input LOW Voltge	–1810	—	–1475	–1810	—	–1475	mV	
I_{IL}	Input LOW Current	0.5	—	—	0.5	—	—	µA	V_{IN} = V_{IL}(max)

1. This table replaces the three tables traditionally seen in ECL 100K data books. The same DC parameter values at V_{EE} = –4.5V now apply across the full V_{EE} range of –4.2V to –5.5V. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.

ABSOLUTE MAXIMUM RATINGS[1]

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0V)	V_{EE}	–8.0 to 0	VDC
Input Voltage (V_{CC} = 0V)	V_I	0 to –6.0	VDC
Output Current Continuous Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	–40 to +70	°C
Operating Range[1,2]	V_{EE}	–5.7 to –4.2	V

1. Absolute maximum rating, beyond which, device life may be impaired, unless otherwise specified on an individual data sheet.
2. Parametric values specified at: H–Series: –4.20V to –5.50V
   K–Series: –4.94V to –5.50V

DC CHARACTERISTICS (V_{EE} = V_{EE}(min) – V_{EE}(max); V_{CC} = GND)

Symbol	Characteristic		–40°C			0°C			25°C			70°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	H		45		38	45	52	38	45	52	38	45	52	mA
		K		45		38	45	52	38	45	52	42	50	58	
V_{EE}	Power Supply Voltage	H	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	–4.75	–5.2	–5.5	V
		K	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	–4.20	–4.5	–5.5	
I_{IH}	Input HIGH Current				150			150			150			150	μA

AC CHARACTERISTICS (V_{EE} = V_{EE}(min) – V_{EE}(max); V_{CC} = GND)

Symbol	Characteristic		–40°C			0°C			25°C			70°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
F_{MAX}	Maximum Toggle Frequency			800		650	800		650	800		650	800		
t_{PLH}	Propagation Delay	R to D		440		320	440	580	320	440	580	360	480	620	ps
t_{PHL}	to Output	R to U		330		210	330	470	210	330	470	240	360	500	
		V to D		330		210	330	470	210	330	470	240	360	500	
		V to U		440		320	440	580	320	440	580	360	480	620	
t_r	Output Rise/Fall Times														ps
t_f	Q (20 to 80%)			225		100	225	350	100	225	350	100	225	350	

APPLICATIONS INFORMATION

The 12140 is a high speed digital circuit used as a phase comparator in an analog phase-locked loop. The device determines the “lead” or “lag” phase relationship and time difference between the leading edges of a VCO (V) signal and a Reference (R) input. Since these edges occur only once per cycle, the detector has a range of ±2π radians.

The operation of the 12140 can best be described using the plots of Figure 1. Figure 1 plots the average value of U, D and the difference between U and D versus the phase difference between the V and R inputs.

There are four potential relationships between V and R: R lags or leads V and the frequency of R is less than or greater than the frequency of V. Under these four conditions the 12140 will function as follows:

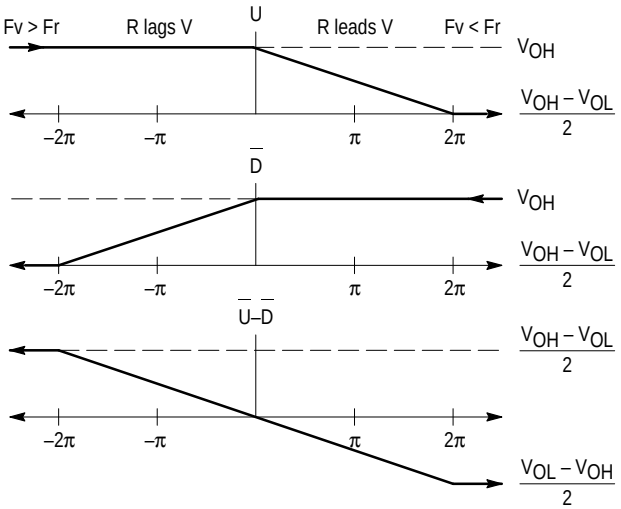


Figure 1. Average Output Voltage versus Phase Difference

R lags V in phase

When the R and V inputs are equal in frequency and the phase of R lags that of V the U output will stay HIGH while the D output will pulse from HIGH to LOW. The magnitude of the pulse will be proportional to the phase difference between the V and R inputs reaching a minimum 50% duty cycle under a 180° out of phase condition. The signal on D indicates to the VCO to decrease in frequency to bring the loop into lock.

V frequency > R frequency

When the frequency of V is greater than that of R the 12140 behaves in a simlar fashion as above. Again the signal on D indicates that the VCO frequency must be decreased to bring the loop into lock.

R leads V in phase

When the R and V inputs are equal in frequency and the phase of R leads that of V the D output will stay HIGH while the U output pulses from HIGH to LOW. The magnitude of the pulse will be proportional to the phase difference between the V and R inputs reaching a minimum 50% duty cycle under a 180° out of phase condition. The signal on U indicates to the VCO to increase in frequency to bring the loop into lock.

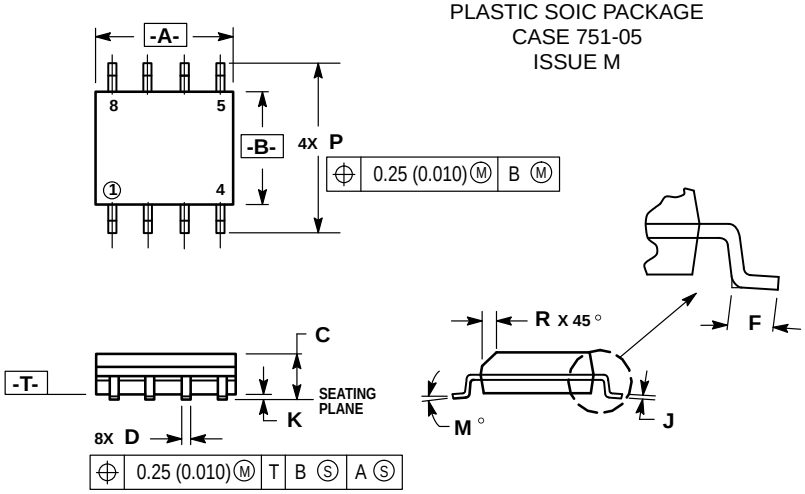
V frequency < R frequency

When the frequency of V is less than that of R the 12140 behaves in a simlar fashion as above. Again the signal on U indicates that the VCO frequency must be decreased to bring the loop into lock.

From Figure 1 when V and R are at the same frequency and in phase the value of U – D is zero thus providing a zero error voltage to the VCO. This situation indicates the loop is in lock and the 12140 action will maintain the loop in its locked state.

OUTLINE DIMENSIONS

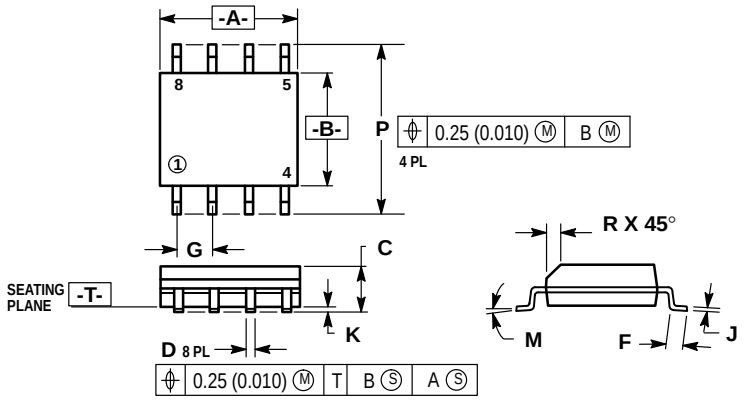
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-05
ISSUE M



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

D SUFFIX
SOIC PACKAGE
CASE 751-03



NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. CONTROLLING DIM: MILLIMETER.
4 DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
6. 751-01 AND -02 OBSOLETE, NEW STANDARD 751-03.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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