

Motorola Semiconductor Technical Data

Addendum to **MC68HC908GP20** **Advance Information**

This addendum provides corrections to:

MC68HC908GP20 Advance Information (Motorola document number
MC68HC908GP20/D Rev. 2.0)

Page 338 Correct the SPRIE description under **20.14.1 SPI Control Register**

From: SPRIE — SPI Receiver Interrupt Enable Bit

This read/write bit enables CPU interrupt requests generated by the SPRF bit. The SPRF bit is set when a byte transfers from the shift register to the receive data register. Reset clears the SPRIE bit.

1 = SPRF CPU interrupt requests

0 = SPRF CPU interrupt requests

To: SPRIE — SPI Receiver Interrupt Enable Bit


This read/write bit enables CPU interrupt requests generated by the SPRF bit. The SPRF bit is set when a byte transfers from the shift register to the receive data register. Reset clears the SPRIE bit.

1 = SPRF CPU interrupt requests enabled

0 = SPRF CPU interrupt requests disabled



Addendum

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