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Technical Supplement

MC68HC812A4 Electrical Characteristics

The MC68HC812A4 microcontroller unit (MCU) is a 16-bit device composed of standard on-chip peripheral modules connected by an intermodule bus. Modules include a 16-bit central processing unit (CPU12), a Lite integration module (LIM), two asynchronous serial communications interfaces (SCI0 and SCI1), a serial peripheral interface (SPI), a timer and pulse accumulation module, an 8-bit analog-to-digital converter (ATD), 1-Kbyte RAM, 4-Kbyte EEPROM, and memory expansion logic with chip selects, key wakeup ports, and a phase-locked loop (PLL).

This supplement contains the most accurate electrical information for the MC68HC812A4 microcontroller available at the time of publication. The information should be considered preliminary and is subject to change. The following characteristics are contained in this document:

Table 1 Maximum Ratings

Table 2 Thermal Characteristics

Table 3 DC Electrical Characteristics

Table 4 Supply Current

Table 5 ATD DC Electrical Characteristics

Table 6 Analog Converter Characteristics (Operating)

Table 7 ATD AC Characteristics (Operating)

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Table 9 EEPROM Characteristics

Table 10 Control Timing

Table 11 Peripheral Port Timing

Table 12 Non-Multiplexed Expansion Bus Timing

Table 13 SPI Timing

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Table 1 Maximum Ratings¹

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}, V_{DDA}, V_{DDX}	-0.3 to +6.5	V
Input voltage	V_{IN}	-0.3 to +6.5	V
Operating temperature range ² MC68HC812A4PV8 MC68HC812A4CPV8 MC68HC812A4VPV8 MC68HC812A4MPV8	T_A	T_L to T_H 0 to +70 -40 to +85 -40 to +105 -40 to +125	°C
Storage temperature range	T_{stg}	-55 to +150	°C
Current drain per pin ³ Excluding V_{DD} and V_{SS}	I_{IN}	±25	mA
V_{DD} differential voltage	$V_{DD}-V_{DDX}$	6.5	V

NOTES:

1. Permanent damage can occur if maximum ratings are exceeded. Exposures to voltages or currents in excess of recommended values affects device reliability. Device modules may not operate normally while being exposed to electrical extremes.
2. Refer to MC68HC812A4TS/D Technical Summary for complete part numbers.
3. One pin at a time, observing maximum power dissipation limits. Internal circuitry protects the inputs against damage caused by high static voltages or electric fields; however, normal precautions are necessary to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Extended operation at the maximum ratings can adversely affect device reliability. Tying unused inputs to an appropriate logic voltage level (either GND or V_{DD}) enhances reliability of operation.

Table 2 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Average junction temperature	T_J	$T_A + (P_D \times \Theta_{JA})$	°C
Ambient temperature	T_A	User-determined	°C
Package thermal resistance (junction-to-ambient) 112-pin thin quad flat pack (TQFP)	Θ_{JA}	39	°C/W
Total power dissipation ¹	P_D	$\frac{P_{INT} + P_{I/O}}{K}$ $\overline{T_J + 273^\circ\text{C}}$	W
Device internal power dissipation	P_{INT}	$I_{DD} \times V_{DD}$	W
I/O pin power dissipation ²	$P_{I/O}$	User-determined	W
A constant ³	K	$P_D \times (T_A + 273^\circ\text{C}) + \Theta_{JA} \times P_D^2$	W · °C

NOTES:

1. This is an approximate value, neglecting $P_{I/O}$.
2. For most applications $P_{I/O} \ll P_{INT}$ and can be neglected.
3. K is a constant pertaining to the device. Solve for K with a known T_A and a measured P_D (at equilibrium). Use this value of K to solve for P_D and T_J iteratively for any value of T_A .

Table 3 DC Electrical Characteristics
 $V_{DD} = 5.0 \text{ Vdc} \pm 10\%$, $V_{SS} = 0 \text{ Vdc}$, $T_A = T_L$ to T_H , unless otherwise noted

Characteristic	Symbol	Min	Max	Unit
Input high voltage, all inputs	V_{IH}	$0.7 \times V_{DD}$	$V_{DD} + 0.3$	V
Input low voltage, all inputs	V_{IL}	$V_{SS} - 0.3$	$0.2 \times V_{DD}$	V
Output high voltage All I/O and output pins Normal drive strength $I_{OH} = -10.0 \mu\text{A}$ $I_{OH} = -0.8 \text{ mA}$ Reduced drive strength $I_{OH} = -4.0 \mu\text{A}$ $I_{OH} = -0.3 \text{ mA}$	V_{OH}	$V_{DD} - 0.2$ $V_{DD} - 0.8$ $V_{DD} - 0.2$ $V_{DD} - 0.8$	— — — —	V V V V
Output low voltage, All I/O and output pins, normal drive strength $I_{OL} = 10.0 \mu\text{A}$ $I_{OL} = 1.6 \text{ mA}$ EXTAL, PAD[7:0], V_{RH} , V_{RL} , V_{FP} , \overline{XIRQ} , reduced drive strength $I_{OL} = 3.6 \mu\text{A}$ $I_{OL} = 0.6 \text{ mA}$	V_{OL}	— — — —	$V_{SS} + 0.2$ $V_{SS} + 0.4$ $V_{SS} + 0.2$ $V_{SS} + 0.4$	V V V V
Input leakage current, ¹ all input pins except \overline{IRQ} , XFC, ATD ² $V_{in} = V_{DD}$ or V_{SS} V_{RL}, V_{RH} , PAD[6:0] $V_{in} = V_{DD}$ or V_{SS} \overline{IRQ} , PAD7 $V_{in} = V_{DD}$ or V_{SS} XFC	I_{in}	— — —	± 1 ± 10 TBD	μA μA μA
Three-state leakage, I/O ports, BKGD, and \overline{RESET}	I_{OZ}	—	± 2.5	μA
Input capacitance All input pins and ATD pins (non-sampling) ATD pins (sampling) All I/O pins	C_{in}	— — —	10 15 20	pF pF pF
Output load capacitance All outputs except PS[7:4] PS[7:4]	C_L	— —	90 200	pF pF
Active pull-up, pull-down current \overline{IRQ} , \overline{XIRQ} , \overline{DBE} , ECLK, \overline{LSTRB} , R/\overline{W} , BKGD, Ports A, B, C, D, F, G, H, J, P, S, T	I_{APU}	50	500	μA
Resistive pull-up current, \overline{IRQ}/V_{PP} ³ Pin voltage = 0V Pin voltage = 18V	I_{RPU}	50 250	500 1000	μA μA
RAM standby voltage, power down	V_{SB}	1.5	—	V
RAM standby current	I_{SB}	—	30	μA

NOTES:

1. Specification is for parts in the -40 to $+85^\circ\text{C}$ range. Higher temperature ranges will result in increased current leakage.
2. See **Table 5 ATD DC Electrical Characteristics**.
3. V_{PP} function of this pin is used for factory test purposes only.

Table 4 Supply Current
 $V_{DD} = 5.0 \text{ Vdc} \pm 10\%$, $V_{SS} = 0 \text{ Vdc}$, $T_A = T_L$ to T_H , unless otherwise noted

Characteristic	Symbol	2 MHz	4 MHz	8 MHz	Unit
Maximum total supply current					
RUN:					
Single-chip mode	I_{DD}	8	15	27	mA
Expanded mode		14	27	35	mA
WAIT: (All peripheral functions shut down)					
Single-chip mode	W_{IDD}	3	6	15	mA
Expanded mode		5	10	20	mA
STOP:					
Single-chip mode, no clocks	S_{IDD}				
-40 to +85		10	10	10	μA
+85 to +105		25	25	25	μA
+105 to +125		50	50	50	μA
Maximum power dissipation ¹					
Single-chip mode	P_D	TBD	TBD	TBD	mW
Expanded mode		TBD	TBD	TBD	mW

NOTES:

1. Includes I_{DD} and I_{DDA} .**Table 5 ATD DC Electrical Characteristics**
 $V_{DD} = 5.0 \text{ Vdc} \pm 10\%$, $V_{SS} = 0 \text{ Vdc}$, $T_A = T_L$ to T_H , ATD Clock = 2 MHz, unless otherwise noted

Characteristic	Symbol	Min	Max	Unit
Analog supply voltage	V_{DDA}	4.5	5.5	V
Analog supply current				
Normal operation	I_{DDA}		1.0	mA
STOP			10	μA
Reference voltage, low	V_{RL}	V_{SSA}	$V_{DDA}/2$	V
Reference voltage, high	V_{RH}	$V_{DDA}/2$	V_{DDA}	V
V_{REF} differential reference voltage ¹	$V_{RH} - V_{RL}$	4.5	5.5	V
Input voltage ²	V_{INDC}	V_{SSA}	V_{DDA}	V
Input current, off channel ³	I_{OFF}		100	nA
Reference supply current	I_{REF}		250	μA
Input capacitance				
Not Sampling	C_{INN}		10	pF
Sampling	C_{INS}		15	pF

NOTES:

1. Accuracy is guaranteed at $V_{RH} - V_{RL} = 5.0\text{V} \pm 10\%$.
2. To obtain full-scale, full-range results, $V_{SSA} \leq V_{RL} \leq V_{INDC} \leq V_{RH} \leq V_{DDA}$.
3. Maximum leakage occurs at maximum operating temperature. Current decreases by approximately one-half for each 10°C decrease from maximum temperature.

Table 6 Analog Converter Characteristics (Operating)

$V_{DD} = 5.0 \text{ Vdc} \pm 10\%$, $V_{SS} = 0 \text{ Vdc}$, $T_A = T_L$ to T_H , ATD Clock = 2 MHz, unless otherwise noted

Characteristic	Symbol	Min	Typical	Max	Unit
8-bit resolution ¹	1 count		20		mV
Differential non-linearity ²	DNL	-0.5		+0.5	count
Integral non-linearity ²	INL	-1		+1	count
Absolute error ^{2,3} 2, 4, 8, and 16 ATD sample clocks	AE	-1		+1	count
Maximum source impedance	R_S		20	See note ⁴	K Ω

NOTES:

- $V_{RH} - V_{RL} \geq 5.12\text{V}$; $V_{DDA} - V_{SSA} = 5.12\text{V}$
- At $V_{REF} = 5.12\text{V}$, one 8-bit count = 20 mV.
- Eight-bit absolute error of 1 count (20 mV) includes 1/2 count (10 mV) inherent quantization error and 1/2 count (10 mV) circuit (differential, integral, and offset) error.
- Maximum source impedance is application-dependent. Error resulting from pin leakage depends on junction leakage into the pin and on leakage due to charge-sharing with internal capacitance. Error from junction leakage is a function of external source impedance and input leakage current. Expected error in result value due to junction leakage is expressed in voltage (V_{ERRJ}):

$$V_{ERRJ} = R_S \times I_{OFF}$$

where I_{OFF} is a function of operating temperature. Charge-sharing effects with internal capacitors are a function of ATD clock speed, the number of channels being scanned, and source impedance. For 8-bit conversions, charge pump leakage is computed as follows:

$$V_{ERRJ} = .25\text{pF} \times V_{DDA} \times R_S \times \text{ATDCLK} / (8 \times \text{number of channels})$$

Table 7 ATD AC Characteristics (Operating)

$V_{DD} = 5.0 \text{ Vdc} \pm 10\%$, $V_{SS} = 0 \text{ Vdc}$, $T_A = T_L$ to T_H , ATD Clock = 2 MHz, unless otherwise noted

Characteristic	Symbol	Min	Max	Unit
Maximum source impedance	R_S		20	K Ω
ATD operating clock frequency	f_{ATDCLK}	0.5	2.0	MHz
Conversion time per channel 0.5 MHz $\leq f_{\text{ATDCLK}} \leq$ 2 MHz 16 ATD clocks 30 ATD clocks	t_{CONV}	8.0 15.0	32.0 60.0	μs μs
Stop recovery time $V_{DDA} = 5.0\text{V}$	t_{SR}		10	μs

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Table 8 ATD Maximum Ratings

Characteristic	Symbol	Value	Units
ATD reference voltage $V_{RH} \leq V_{DDA}$ $V_{RL} \geq V_{SSA}$	V_{RH} V_{RL}	-0.3 to +6.5 -0.3 to +6.5	V V
V_{SS} differential voltage	$ V_{SS}-V_{SSA} $	0.1	V
V_{DD} differential voltage	$ V_{DD}-V_{DDA} $ $V_{DD}-V_{DDX}$	6.5 6.5	V V
V_{REF} differential voltage	$ V_{RH}-V_{RL} $	6.5	V
Reference to supply differential voltage	$ V_{RH}-V_{DDA} $ $ V_{RL}-V_{SSA} $	6.5 6.5	V V
ATD input voltage, series resistance = 16 K Ω Time = 5 minutes Time = 1 minute Total current \leq 8 mA	V_{MAXAD}	-16.0 24.0	V V

Table 9 EEPROM Characteristics

$V_{DD} = 5.0 \text{ Vdc} \pm 10\%$, $V_{SS} = 0 \text{ Vdc}$, $T_A = T_L$ to T_H , unless otherwise noted

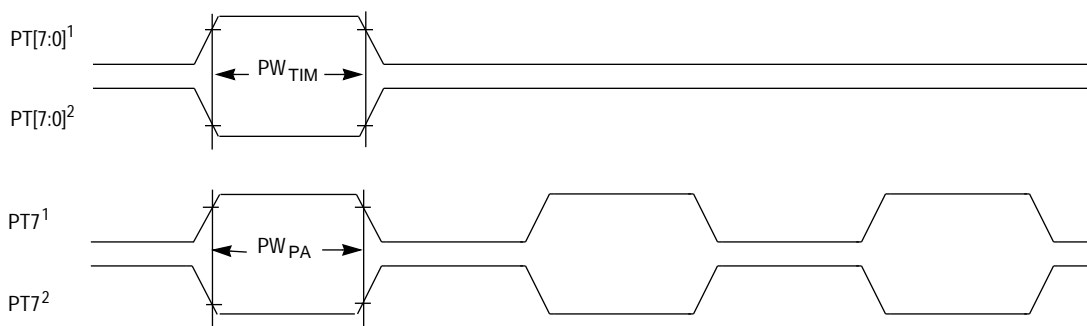
Characteristic	Symbol	Min	Typical	Max	Unit
Minimum programming clock frequency ¹	f_{PROG}	1.0			MHz
Programming time	t_{PROG}			10	ms
Clock recovery time following STOP, to continue programming	t_{CRSTOP}			$t_{PROG} + 1$	ms
Erase time	t_{ERASE}			10	ms
Write/erase endurance		10,000	30,000 ²		cycles
Data retention		10			years

NOTES:

1. RC oscillator must be enabled if programming is desired and $f_{SYS} < f_{PROG}$.
2. If average T_H is below 85° C.

Table 10 Control Timing

Characteristic	Symbol	8.0 MHz		Unit
		Min	Max	
Frequency of operation	f_o	dc	8.0	MHz
E-clock period	t_{cyc}	125	—	ns
Crystal frequency	f_{XTAL}	—	16.0	MHz
External oscillator frequency	$2f_o$	dc	16.0	MHz
Processor control setup time $t_{PCSU} = t_{cyc}/4 + 20$	t_{PCSU}	51	—	ns
Reset input pulse width To guarantee external reset vector Minimum input time (can be preempted by internal reset)	PW_{RSTL}	32 2	— —	t_{cyc} t_{cyc}
Mode programming setup time	t_{MPS}	4	—	t_{cyc}
Mode programming hold time	t_{MPH}	10	—	ns
Interrupt pulse width, \overline{IRQ} , edge-sensitive mode, KWU $PW_{IRQ} = 2t_{cyc} + 20$	PW_{IRQ}	TBD	—	ns
Wait recovery startup time	t_{WRS}	—	TBD	t_{cyc}
Timer pulse width, input capture pulse accumulator input $PW_{TIM} = 2t_{cyc} + 20$	PW_{TIM}	TBD	—	ns

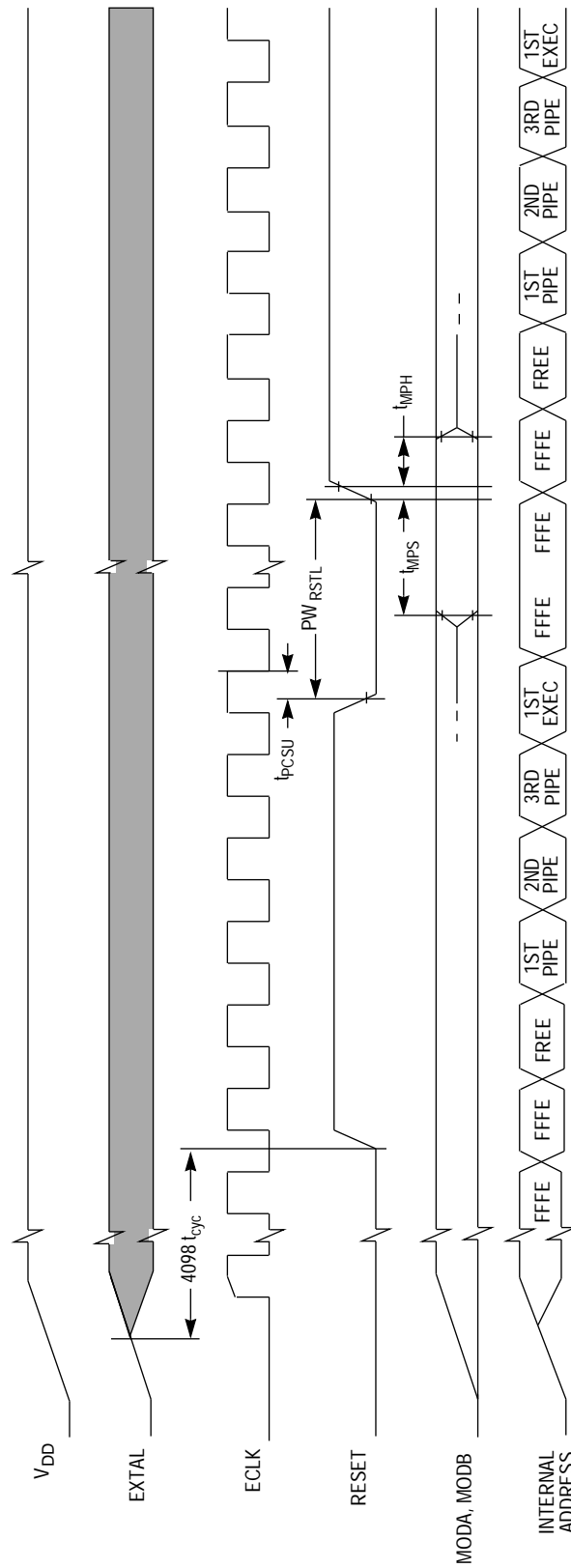


NOTES :

1. Rising edge sensitive input
2. Falling edge sensitive input

TIMER INPUT TIMING

Figure 1 Timer Inputs



POR EXT RESET TIM

NOTE: Reset timing is subject to change.

Figure 2 POR and External Reset Timing Diagram



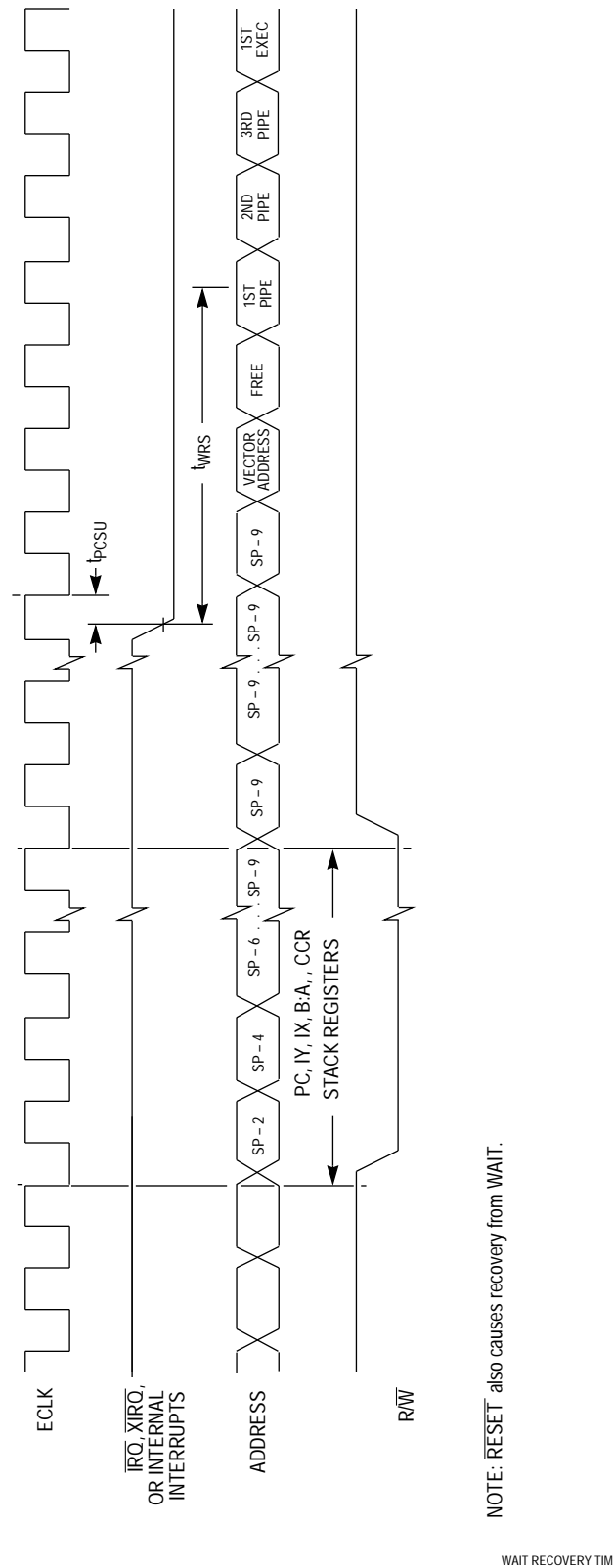


Figure 4 WAIT Recovery Timing Diagram

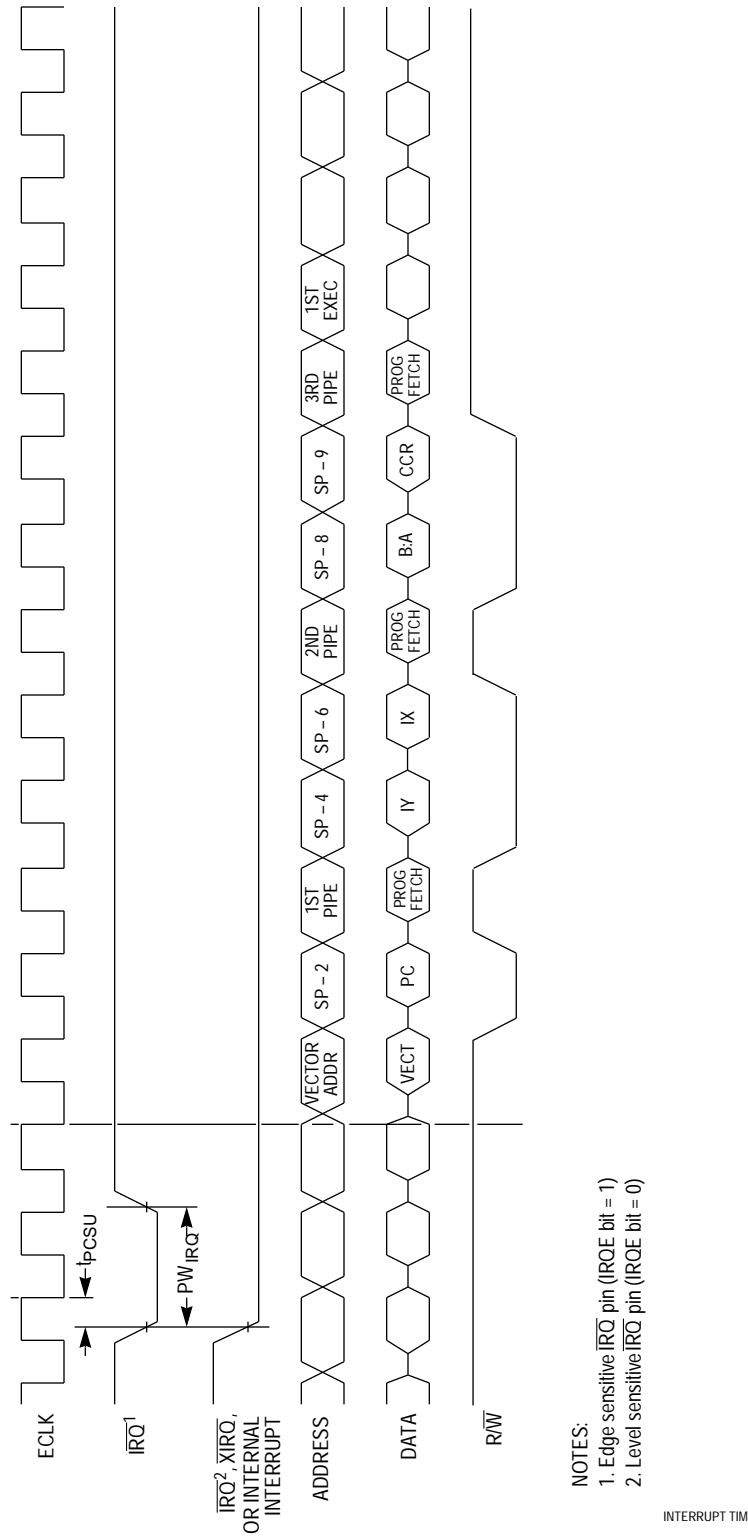


Figure 5 Interrupt Timing Diagram

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Table 11 Peripheral Port Timing

Characteristic	Symbol	8.0 MHz		Unit
		Min	Max	
Frequency of operation (E-clock frequency)	f_o	dc	8.0	MHz
E-clock period	t_{cyc}	125	—	ns
Peripheral data setup time MCU read of ports $t_{PDSU} = t_{cyc}/2 + 40$	t_{PDSU}	102	—	ns
Peripheral data hold time MCU read of ports	t_{PDH}	0	—	ns
Delay time, peripheral data write MCU write to ports	t_{PWD}	—	40	ns

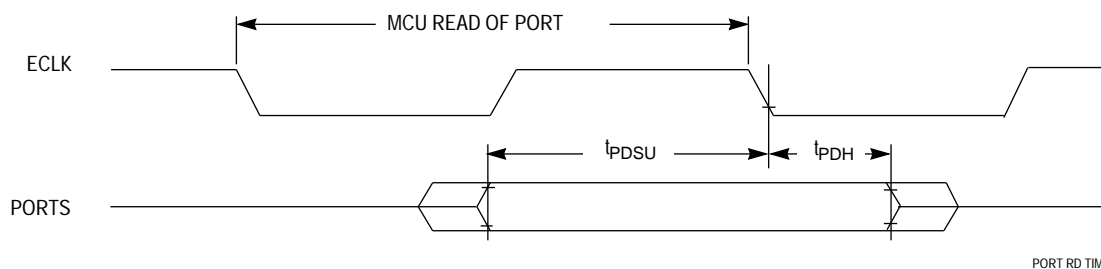


Figure 6 Port Read Timing Diagram

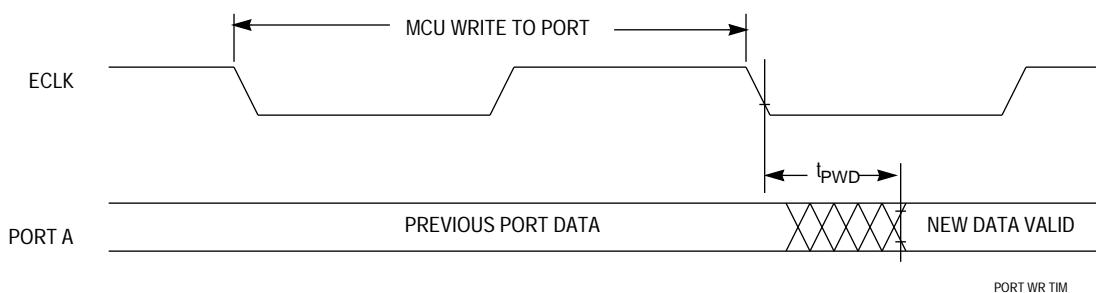


Figure 7 Port Write Timing Diagram

Table 12 Non-Multiplexed Expansion Bus Timing $V_{DD} = 5.0 \text{ Vdc} \pm 10\%$, $V_{SS} = 0 \text{ Vdc}$, $T_A = T_L$ to T_H , unless otherwise noted

Num	Characteristic ¹	Delay	Symbol	8 MHz		Unit
				Min	Max	
	Frequency of operation (E-clock frequency)		f_o	dc	8.0	MHz
1	Cycle time $t_{cyc} = 1/f_o$		t_{cyc}	125	—	ns
2	Pulse width, E low $PW_{EL} = t_{cyc}/2 + \text{delay}$	–2	PW_{EL}	60	—	ns
3	Pulse width, E high ² $PW_{EH} = t_{cyc}/2 + \text{delay}$	–2	PW_{EH}	60	—	ns
5	Address delay time $t_{AD} = t_{cyc}/4 + \text{delay}$	9	t_{AD}	—	40	ns
6	Address hold time $t_{AH} = t_{cyc}/4 + \text{delay}$	–6	t_{AH}	25	—	ns
7	Address valid time to E rise $t_{AV} = PW_{EL} - t_{AD}$	—	t_{AV}	20	—	ns
11	Read data setup time	—	t_{DSR}	20	—	ns
12	Read data hold time	—	t_{DHR}	0	—	ns
13	Write data delay time $t_{DDW} = t_{cyc}/4 + \text{delay}$	9	t_{DDW}	—	40	ns
14	Write data hold time $t_{DHW} = t_{cyc}/4 + \text{delay}$	–6	t_{DHW}	25	—	ns
15	Write data setup time ² $t_{DSW} = PW_{EH} - t_{DSR}$	—	t_{DSW}	40	—	ns
16	Read/write delay time $t_{RWD} = t_{cyc}/4 + \text{delay}$	9	t_{RWD}	—	40	ns
17	Read/write valid time to E rise $t_{RWV} = PW_{EL} - t_{RWD}$	—	t_{RWV}	20	—	ns
18	Read/write hold time $t_{RWH} = t_{cyc}/4 + \text{delay}$	–6	t_{RWH}	25	—	ns
19	Low strobe delay time $t_{LSD} = t_{cyc}/4 + \text{delay}$	9	t_{LSD}	—	40	ns
20	Low strobe valid time to E rise $t_{LSV} = PW_{EL} - t_{LSD}$	—	t_{LSV}	20	—	ns
21	Low strobe hold time $t_{LSH} = t_{cyc}/4 + \text{delay}$	–6	t_{LSH}	25	—	ns
22	Address access time ² $t_{ACCA} = t_{cyc} - t_{AD} - t_{DSR}$	—	t_{ACCA}	—	65	ns
23	Access time from E rise ² $t_{ACCE} = PW_{EH} - t_{DSR}$	—	t_{ACCE}	—	40	ns
26	Chip select delay time $t_{CSD} = t_{cyc}/4 + \text{delay}$	9	t_{CSD}	—	40	ns
27	Chip select access time ² $t_{ACCS} = t_{cyc} - t_{CSD} - t_{DSR}$	—	t_{ACCS}	—	65	ns
28	Chip select hold time	—	t_{CSH}	0	10	ns
29	Chip select negated time $t_{CSN} = t_{cyc}/4 + \text{delay}$	–1	t_{CSN}	30	—	ns

NOTES:

1. All timings are calculated for normal port drives.
2. This characteristic is affected by clock stretch.
Add $N \times t_{cyc}$ where $N = 0, 1, 2$, or 3 , depending on the number of clock stretches.

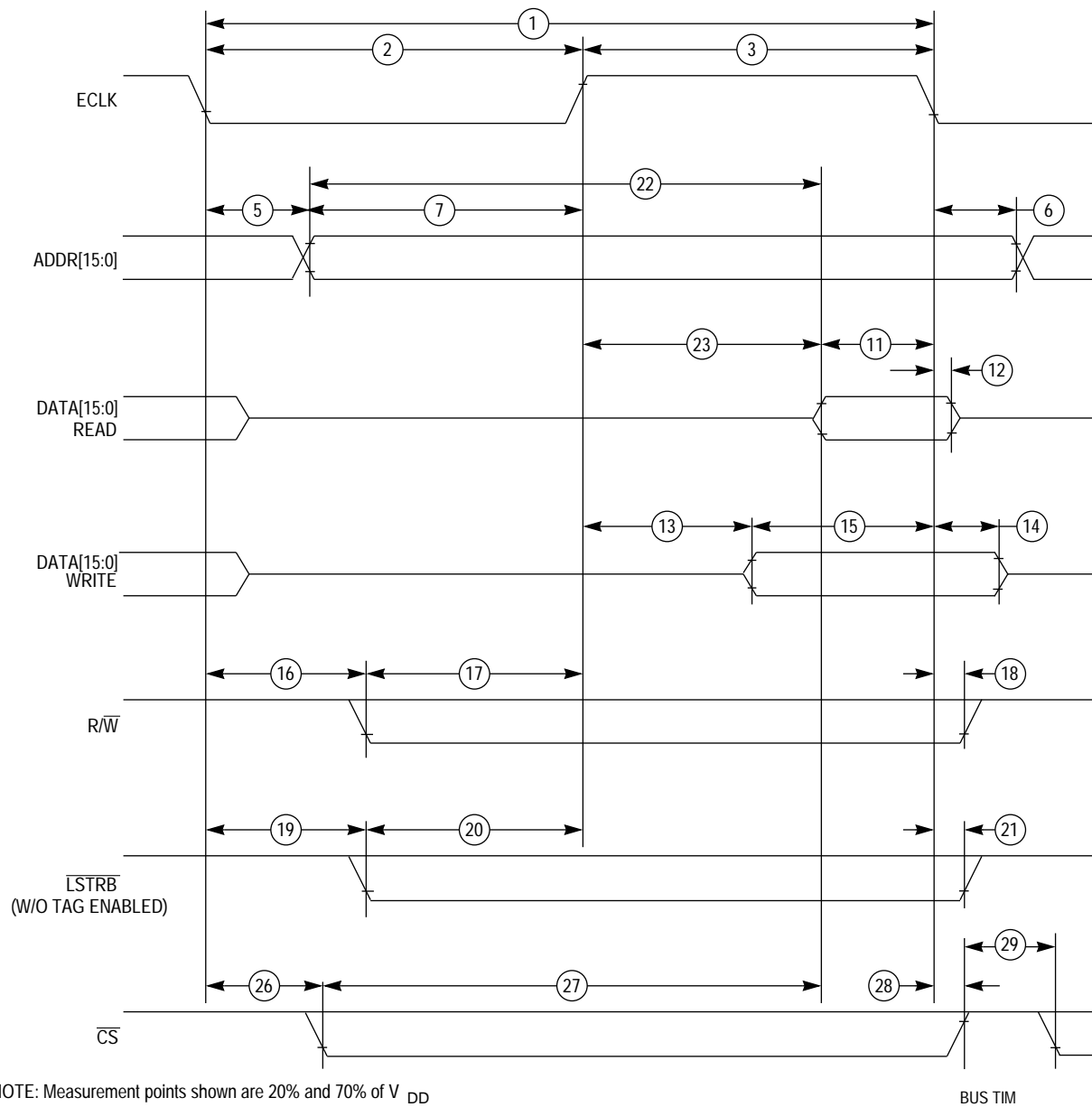


Figure 8 Non-Multiplexed Expansion Bus Timing Diagram

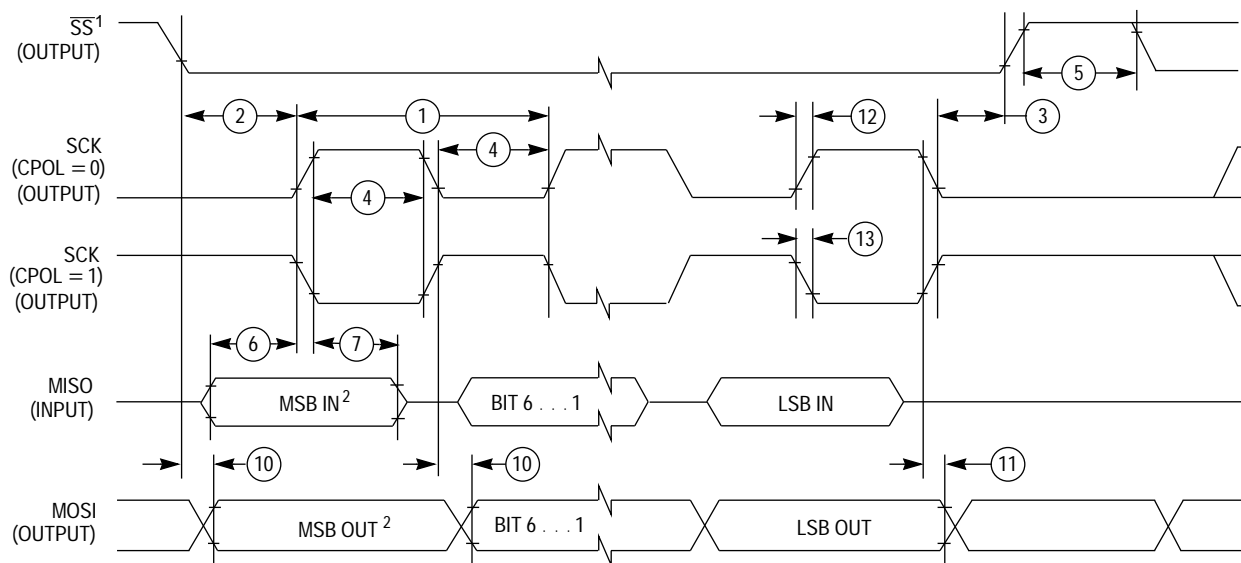
Table 13 SPI Timing(V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, T_A = T_L to T_H, 200 pF load on all SPI pins)¹

Num	Function	Symbol	Min	Max	Unit
	Operating Frequency Master Slave	f _{op}	DC DC	1/2 1/2	E-clock frequency
1	SCK Period Master Slave	t _{sck}	2 2	256 —	t _{cyc} t _{cyc}
2	Enable Lead Time Master Slave	t _{lead}	1/2 1	— —	t _{sck} t _{cyc}
3	Enable Lag Time Master Slave	t _{lag}	1/2 1	— —	t _{sck} t _{cyc}
4	Clock (SCK) High or Low Time Master Slave	t _{wsck}	t _{cyc} – 60 t _{cyc} – 30	128 t _{cyc} —	ns ns
5	Sequential Transfer Delay Master Slave	t _{td}	1/2 1	— —	t _{sck} t _{cyc}
6	Data Setup Time (Inputs) Master Slave	t _{su}	30 30	— —	ns ns
7	Data Hold Time (Inputs) Master Slave	t _{hi}	0 30	— —	ns ns
8	Slave Access Time	t _a	—	1	t _{cyc}
9	Slave MISO Disable Time	t _{dis}	—	1	t _{cyc}
10	Data Valid (after SCK Edge) Master Slave	t _v	— —	50 50	ns ns
11	Data Hold Time (Outputs) Master Slave	t _{ho}	0 0	— —	ns ns
12	Rise Time Input Output	t _{ri} t _{ro}	— —	t _{cyc} – 30 30	ns ns
13	Fall Time Input Output	t _{fi} t _{fo}	— —	t _{cyc} – 30 30	ns ns

NOTES:1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.**NOTES:**1. All timing is shown with respect to 20% V_{DD} and 70% V_{DD}, unless otherwise noted.

2. Signal production depends on software.

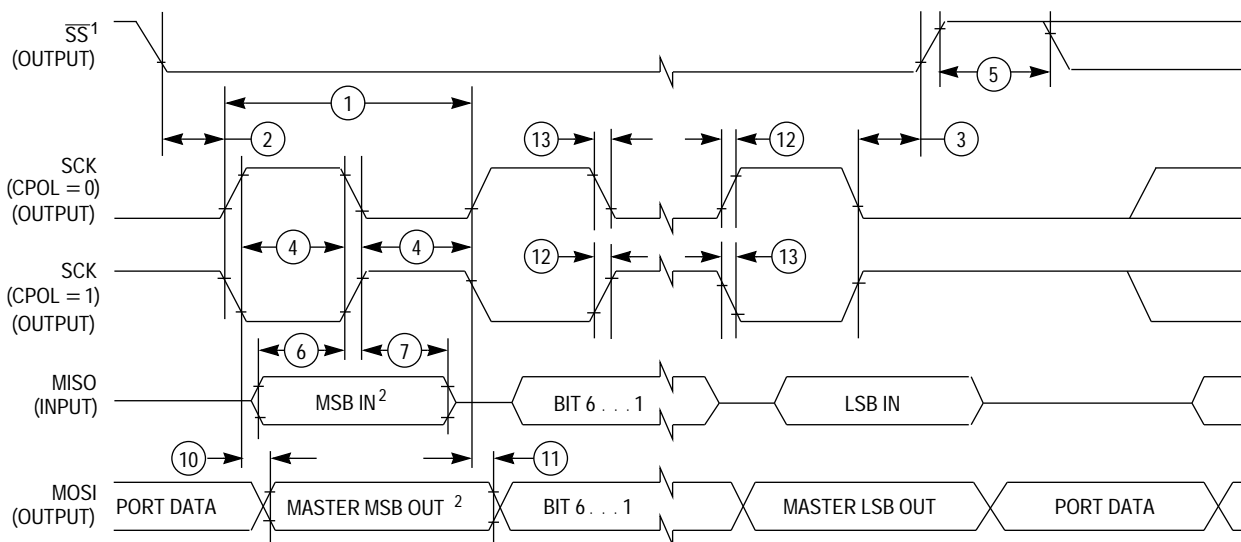
3. Assumes 100 pF load on all SPI pins.



1. \overline{SS} output mode (DDS7 = 1, SS0E = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

SPI MASTER CPHA0

A) SPI Master Timing (CPHA = 0)

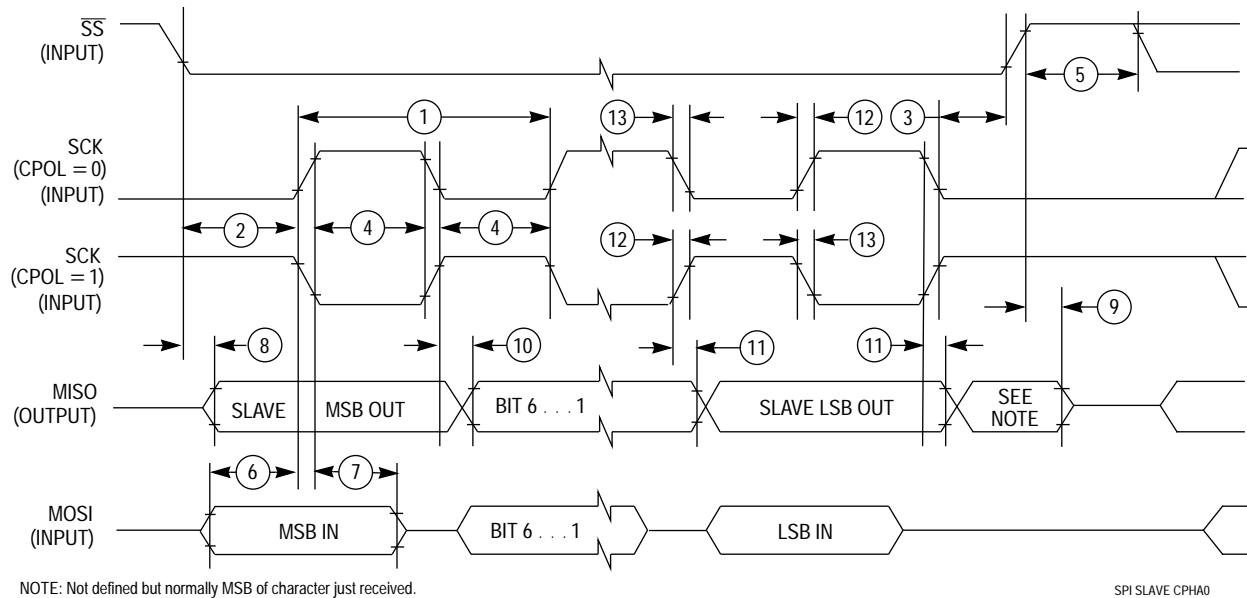


1. \overline{SS} output mode (DDS7 = 1, SS0E = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

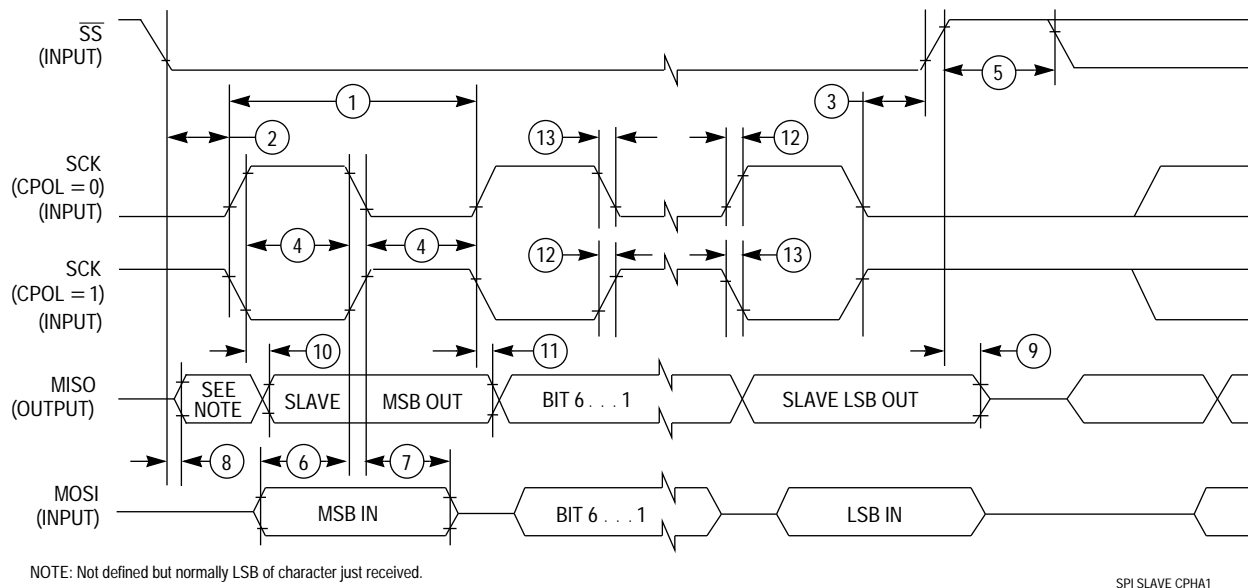
SPI MASTER CPHA1

B) SPI Master Timing (CPHA = 1)

Figure 9 SPI Timing Diagram (1 of 2)



A) SPI Slave Timing (CPHA = 0)



B) SPI Slave Timing (CPHA = 1)

Figure 10 SPI Timing Diagram (2 of 2)

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