Motorola Semiconductor Technical Data

Addendum to MC68HC705J1A HCMOS Microcontroller Unit Technical Data

This addendum provides changes to the *MC68HC705J1A*, *MC68HRC705J1A*, *MC68HSC705J1A*, and *MC68HSR705J1A Technical Data* (Motorola document order number MC68HC705J1A/D Rev. 3.0).

On page 35, change the last entry of Figure 2-2. I/O Register Summary

From:

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$07F1	Mask Option Register (MOR) See page 39.	Read: Write:	SOSCD	EPMSEC	OSCRES	SWAIT	SWPDI	PIRQ	LEVEL	COPEN
		Reset:	0	0	0	0	0	0	0	0

To:

Addr.	Register Name	Bit 7	6	5	4	3	2	1	Bit 0
\$07F1	Mask Option Register (MOR) Wri	SOSCD	EPMSEC	OSCRES	SWAIT	SWPDI	PIRQ	LEVEL	COPEN
	See page 39. Res	et:	Unaffected by reset						

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On page 39, change Figure 2-4. Mask Option Register (MOR)

From:

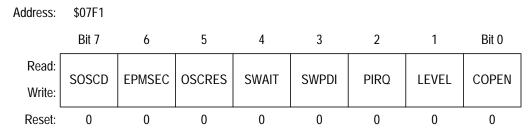


Figure 2-4. Mask Option Register (MOR)

To:



Figure 2-4. Mask Option Register (MOR)

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On page 89, change the note under 6.3.3 Pulldown Register A:

From:

NOTE: If the SWPDI bit in the mask option register is programmed to logic 1,

reset initializes all port A pins as inputs with enabled pulldown devices.

To:

NOTE: If the SWPDI bit in the mask option register is programmed to logic 1,

reset initializes all port A pins as inputs with disabled pulldown devices.

On page 92, change the note under 6.4.3 Pulldown Register B

From:

NOTE: If the SWPDI bit in the mask option register is programmed to logic 1,

reset initializes all port B pins as inputs with enabled pulldown devices.

To:

NOTE: If the SWPDI bit in the mask option register is programmed to logic 1,

reset initializes all port B pins as inputs with disabled pulldown devices.

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Addendum

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