Addendum to
MC68HC05P9
HCMOS Microcontroller Unit
Technical Data

This addendum provides additions and corrections to the *MC68HC05P9 Technical Data*, Rev. 0 (Motorola document number MC68HC05P9/D).

1. Page 1-1, section **1.1 Features** — Change the third bulleted item as follows:

   From:

   - 2112 Bytes of User ROM including 16 User Vector Locations

   To:

   - 2104 Bytes of User ROM including 8 User Vector Locations

2. Page 2-7, section **2.6.3 Port C and Analog-to-Digital Converter** — Replace the second paragraph with the following:

   From:

   When the A/D converter is enabled, PC7 becomes V_{RH}, and PC6–PC3 become AN3–AN0 (analog inputs 3–0). The values of CH1 and CH0 in the A/D status and control register (ADSCR) select one of the four pins as the input to the A/D converter. When the A/D converter is enabled, a digital read of port C gives a logical zero from the selected analog input pin. A digital read of port C's remaining pins gives their correct digital values. V_{RH} is the positive (high) reference voltage for the A/D converter. V_{SS} is the negative (low) reference voltage. A reset turns off the A/D converter and configures port C as a general-purpose I/O port. (Refer to **SECTION 8 ANALOG-TO-DIGITAL CONVERTER**.)

   To:

   When the A/D converter is enabled, PC7 becomes V_{RH}, and PC6–PC3 become AN3–AN0 (analog inputs 3–0). The values of CH1 and CH0 in the A/D status and control register (ADSCR) select one of the four pins as the input to the A/D converter.

   Unused analog inputs can be used as digital inputs, but no analog input can be used as a digital output while the ADC is on. Only pins PC0–PC2 can be used as digital outputs when the ADC is on.

   When the A/D converter is enabled, a digital read of port C gives a logical zero from the selected analog input pin. A digital read of the remaining port C pins gives their correct digital values.

   V_{RH} is the positive (high) reference voltage for the A/D converter. V_{SS} is the negative (low) reference voltage. A reset turns off the A/D converter and configures port C as a general-purpose I/O port. (Refer to **SECTION 8 ANALOG-TO-DIGITAL CONVERTER**.)

3. Page 3-23, **Table 3-13. Opcode Map** — Replace the opcode map with the opcode map on page 3. The new opcode map contains data corrections for the following opcodes:

Opcode	Mnemonic	Opcode	Mnemonic
13	BCLR1	68	ASL/LSL
25	BCS/BLO	69	ROL
38	ASL/LSL	6A	DEC
48	ASLA/LSLA	6C	INC
50	NEGX	6D	TST
58	ASLX/LSLX	6F	CLR
		78	ASL/LSL

Table 3-13. Opcode Map

	Bit Manipulation		Branch	Read-Modify-Write					Control		Register/Memory						
	DIR	DIR	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
MSB / LSB	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSB / LSB
0	5 BRSET0 3 DIR	5 BSET0 2 DIR	3 BRA 2 REL	5 NEG 2 DIR	3 NEGA 1 INH	3 NEGX 1 INH	6 NEG 2 IX1	5 NEG 1 IX	9 RTI 1 INH		2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	5 SUB 3 IX2	4 SUB 2 IX1	3 SUB 1 IX	**0**
1	5 BRCLR0 3 DIR	5 BCLR0 2 DIR	3 BRN 2 REL						6 RTS 1 INH		2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	5 CMP 3 IX2	4 CMP 2 IX1	3 CMP 1 IX	**1**
2	5 BRSET1 3 DIR	5 BSET1 2 DIR	3 BHI 2 REL		11 MUL 1 INH						2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	5 SBC 3 IX2	4 SBC 2 IX1	3 SBC 1 IX	**2**
3	5 BRCLR1 3 DIR	5 BCLR1 2 DIR	3 BLS 2 REL	5 COM 2 DIR	3 COMA 1 INH	3 COMX 1 INH	6 COM 2 IX1	5 COM 1 IX	10 SWI 1 INH		2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	5 CPX 3 IX2	4 CPX 2 IX1	3 CPX 1 IX	**3**
4	5 BRSET2 3 DIR	5 BSET2 2 DIR	3 BCC 2 REL	5 LSR 2 DIR	3 LSRA 1 INH	3 LSRX 1 INH	6 LSR 2 IX1	5 LSR 1 IX			2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	5 AND 3 IX2	4 AND 2 IX1	3 AND 1 IX	**4**
5	5 BRCLR2 3 DIR	5 BCLR2 2 DIR	3 BCS/BLO 2 REL								2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	5 BIT 3 IX2	4 BIT 2 IX1	3 BIT 1 IX	**5**
6	5 BRSET3 3 DIR	5 BSET3 2 DIR	3 BNE 2 REL	5 ROR 2 DIR	3 RORA 1 INH	3 RORX 1 INH	6 ROR 2 IX1	5 ROR 1 IX			2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	5 LDA 3 IX2	4 LDA 2 IX1	3 LDA 1 IX	**6**
7	5 BRCLR3 3 DIR	5 BCLR3 2 DIR	3 BEQ 2 REL	5 ASR 2 DIR	3 ASRA 1 INH	3 ASRX 1 INH	6 ASR 2 IX1	5 ASR 1 IX		2 TAX 1 INH		4 STA 2 DIR	5 STA 3 EXT	6 STA 3 IX2	5 STA 2 IX1	4 STA 1 IX	**7**
8	5 BRSET4 3 DIR	5 BSET4 2 DIR	3 BHCC 2 REL	5 ASL/LSL 2 DIR	3 ASLA/LSLA 1 INH	3 ASLX/LSLX 1 INH	6 ASL/LSL 2 IX1	5 ASL/LSL 1 IX		2 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	5 EOR 3 IX2	4 EOR 2 IX1	3 EOR 1 IX	**8**
9	5 BRCLR4 3 DIR	5 BCLR4 2 DIR	3 BHCS 2 REL	5 ROL 2 DIR	3 ROLA 1 INH	3 ROLX 1 INH	6 ROL 2 IX1	5 ROL 1 IX		2 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	5 ADC 3 IX2	4 ADC 2 IX1	3 ADC 1 IX	**9**
A	5 BRSET5 3 DIR	5 BSET5 2 DIR	3 BPL 2 REL	5 DEC 2 DIR	3 DECA 1 INH	3 DECX 1 INH	6 DEC 2 IX1	5 DEC 1 IX		2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	5 ORA 3 IX2	4 ORA 2 IX1	3 ORA 1 IX	**A**
B	5 BRCLR5 3 DIR	5 BCLR5 2 DIR	3 BMI 2 REL							2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	5 ADD 3 IX2	4 ADD 2 IX1	3 ADD 1 IX	**B**
C	5 BRSET6 3 DIR	5 BSET6 2 DIR	3 BMC 2 REL	5 INC 2 DIR	3 INCA 1 INH	3 INCX 1 INH	6 INC 2 IX1	5 INC 1 IX		2 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2	3 JMP 2 IX1	2 JMP 1 IX	**C**
D	5 BRCLR6 3 DIR	5 BCLR6 2 DIR	3 BMS 2 REL	4 TST 2 DIR	3 TSTA 1 INH	3 TSTX 1 INH	5 TST 2 IX1	4 TST 1 IX		2 NOP 1 INH	6 BSR 2 REL	5 JSR 2 DIR	6 JSR 3 EXT	7 JSR 3 IX2	6 JSR 2 IX1	5 JSR 1 IX	**D**
E	5 BRSET7 3 DIR	5 BSET7 2 DIR	3 BIL 2 REL						2 STOP 1 INH		2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	5 LDX 3 IX2	4 LDX 2 IX1	3 LDX 1 IX	**E**
F	5 BRCLR7 3 DIR	5 BCLR7 2 DIR	3 BIH 2 REL	5 CLR 2 DIR	3 CLRA 1 INH	3 CLRX 1 INH	6 CLR 2 IX1	5 CLR 1 IX	2 WAIT 1 INH	2 TXA 1 INH		4 STX 2 DIR	5 STX 3 EXT	6 STX 3 IX2	5 STX 2 IX1	4 STX 1 IX	**F**

INH = Inherent
IMM = Immediate
DIR = Direct
EXT = Extended

REL = Relative
IX = Indexed, No Offset
IX1 = Indexed, 8-Bit Offset
IX2 = Indexed, 16-Bit Offset

LSB of Opcode in Hexadecimal

MSB / LSB	0
0	5 BRSET0 3 DIR

MSB of Opcode in Hexadecimal
Number of Cycles
Opcode Mnemonic
Number of Bytes/Addressing Mode

4. Page 4-1, section **4.1 Resets** — Change the first bulleted item in the second paragraph as follows:

   From:

   - All implemented data direction register bits are cleared to logical zero, so the corresponding I/O pins become high-impedance inputs.

   To:

   - All implemented data direction register bits are cleared to logical zero, so the corresponding I/O pins become high-impedance inputs. (When an external reset or power-on reset occurs, I/O port pins become high-impedance inputs even if the system clock is absent.)

5. Page 4-2, section **4.1.3 Computer Operating Properly (COP) Watchdog Reset** — In the fourth sentence in the first paragraph, change the 64 ms to 65.5 ms as follows:

   From:

   The COP system is implemented with an 18-stage ripple counter that provides a timeout period of 64 ms at an internal clock rate of 2 MHz.

   To:

   The COP system is implemented with an 18-stage ripple counter that provides a timeout period of 65.5 ms at an internal clock rate of 2 MHz.

6. Page 4-2, section **4.1.3 Computer Operating Properly (COP) Watchdog Reset** — Replace the second paragraph as follows:

From:

The write-only COP register is used to prevent a COP timer reset. This location contains user-defined ROM data. Figure 4-1 shows the COP register.

To:

The write-only COP register is used to prevent a COP timer reset. This location contains user-defined ROM data. Figure 4-1 shows the COP register.

Use the following formula to calculate the COP timeout period:

$$\text{COP Timeout Period} = \frac{131{,}072}{f_{BUS}}$$

where

$$f_{BUS} = \frac{\text{crystal frequency}}{2}$$

7. Page 5-2, **Figure 5-1. Memory Map** — Change the USER VECTORS portion at the bottom of the map as follows:

From:

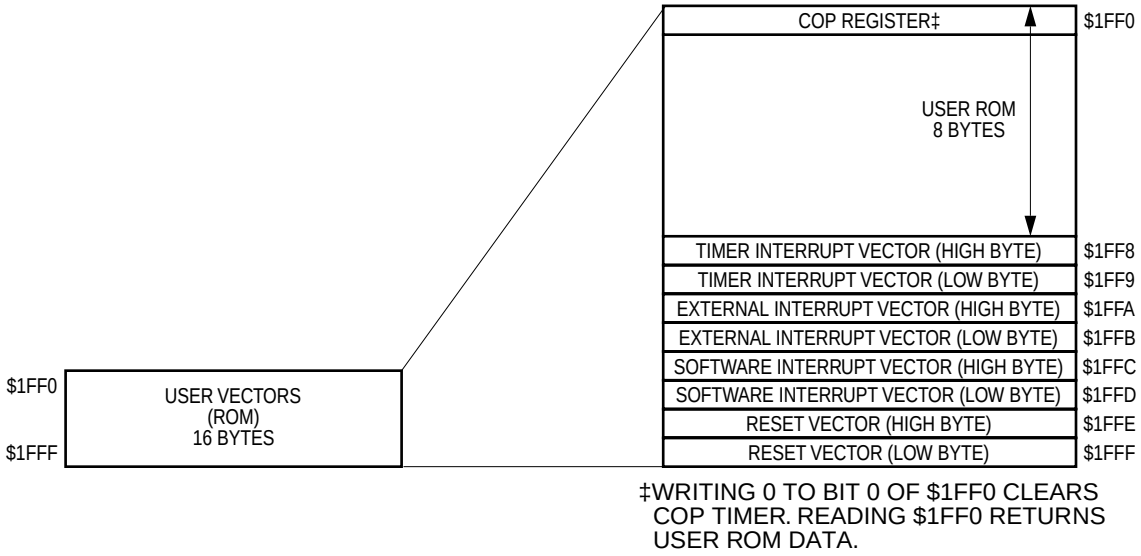
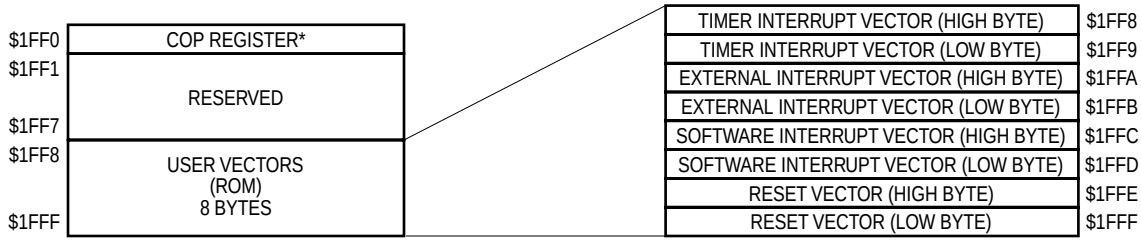


Figure 5-1. Memory Map

To:



*Writing zero to bit 0 of $1FF0 clears the COP timer.

Figure 5-1. Memory Map

8. Page 5-4, section **5.1.3 ROM** — Change the first paragraph as follows:

From:

On-chip user ROM includes 48 bytes at addresses $0020–$004F, 2048 bytes at $0100–$08FF, and 16 bytes at $1FF0–$1FFF that contain user-defined vectors for servicing interrupts and resets.

To:

On-chip user ROM includes 48 bytes at addresses $0020–$004F, 2048 bytes at $0100–$08FF, and 8 bytes at $1FF8–$1FFF that contain user-defined vectors for servicing interrupts and resets.

9. Page 7-3, section **7.2 SIOP Pin Descriptions** — Add the following note after the last paragraph:

NOTE

Enabling and then disabling the SIOP configures data direction register B for SIOP operation and can also change the port B data register. After disabling the SIOP, initialize data direction register B and the port B data register as your application requires.

10. Page 7-4, section **7.2.3 SIOP Data Output** — Change the paragraph as follows:

From:

The SDO pin becomes a serial output and goes to a logical one as soon as the SIOP is enabled. Between transfers, the state of the SDO pin reflects the value of the last bit received on the previous transmission. SDO cannot be used as a standard output while the SIOP is enabled, because it is coupled to the last stage of the serial shift register. On the first falling edge of SCK, the first data bit to be shifted out is presented to the SDO pin.

To:

Enabling the SIOP configures the SDO pin as an output. The state of the SDO pin:

- Is logic one if the SIOP has not been used since the last reset
- Reflects the last bit received if the SIOP has been used since the last reset
- Is unpredictable if SCK was low during reset or if SCK went low after reset

Between transfers, the state of the SDO pin reflects the value of the last bit received on the previous transmission. SDO cannot be used as a standard output while the SIOP is enabled, because it is coupled to the last stage of the serial shift register. On the first falling edge of SCK, the first data bit to be shifted out is presented to the SDO pin.

11. Page 8-1, section **8.1 ADC Operation** — Change the second paragraph as follows:

    From:

    A multiplexer selects one of four analog input channels (AN3, AN2, AN1, or AN0) for sampling. A comparator successively compares the output of an internal D/A converter to the sampled analog input. Control logic changes the D/A converter input one bit at a time, starting with the MSB, until the D/A converter output matches the sampled analog input. The conversion is monotonic and has no missing codes.

    To:

    A multiplexer selects one of four analog input channels (AN0, AN1, AN2, or AN3) for sampling. The conversion takes 32 cycles. The first 12 cycles sample the voltage on the selected input pin by charging an internal capacitor. In the last 20 cycles, a comparator successively compares the output of an internal D/A converter to the sampled analog input. Control logic changes the D/A converter input one bit at a time, starting with the MSB, until the D/A converter output matches the sampled analog input. The conversion is monotonic and has no missing codes. At the end of the conversion, the conversion complete flag (CC) becomes set, and the CPU takes 2 cycles to move the result to the ADC data register (ADDR).

12. Page 8-2, section **8.2 A/D Status and Control Register (ADSCR)** — Change the CCF bit description as follows:

    From:

    CCF — Conversion Complete Flag

    This read-only bit is automatically set when an analog-to-digital conversion is complete, and a new result can be read from the A/D data register. CCF is automatically cleared when a new conversion begins or when either the A/D status and control register or the A/D data register is accessed. Writing to or reading the A/D status and control register or the A/D data register starts a new conversion sequence. Data from the previous conversion is overwritten regardless of the state of the CCF bit. While CCF is a logical zero, the requested A/D result is not yet available in the A/D data register.

    To:

    CCF — Conversion Complete Flag

    This read-only bit is automatically set when an analog-to-digital conversion is complete, and a new result can be read from the A/D data register. Clear the CCF bit by writing to the A/D data register or by reading the A/D data register. Reset clears the CCF bit.

13. Page 10-7, **Table 10-5. A/D Converter Characteristics** — Change the **Max** column in the second row of Table 10-5 as follows:

From:

Table 10-5. A/D Converter Characteristics

Characteristic	Min	Max	Unit
Absolute Accuracy ($4.0 > V_{RH} > V_{DD}$) (refer to NOTE 1)	—	± 1-1/2	LSB

To:

Table 10-5. A/D Converter Characteristics

Characteristic	Min	Max	Unit
Absolute Accuracy ($4.0 > V_{RH} > V_{DD}$) (refer to NOTE 1)	—	± 1.5	LSB

14. Page 10-8, **Figure 10-6. TCAP Timing** — Change the t_{TLTL} parameter to t_{ILIL} as follows:

From:

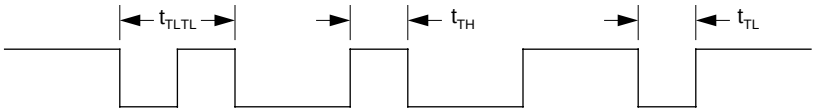


Figure 10-6. TCAP Timing

To:

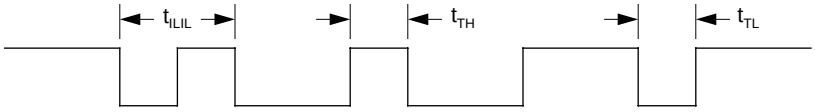


Figure 10-6. TCAP Timing

15. Page 10-12, **Table 10-8. SIOP Timing (V_{DD} = 5.0 Vdc)** — Change the first row as follows:

From:

Table 10-8. SIOP Timing (V_{DD} = 5.0 Vdc)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation Master Slave	$f_{SIOP(M)}$ $f_{SIOP(S)}$	0.25 dc	0.25 525	f_{OP} kHz

To:

Table 10-8. SIOP Timing (V_{DD} = 5.0 Vdc)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation Master Slave	$f_{SIOP(M)}$ $f_{SIOP(S)}$	f_{OSC}/64 dc	f_{OSC}/8 525	MHz kHz

Change NOTE 1 at the bottom of the table as follows:

From:

1. $f_{OP} = f_{OSC} \div 2$ = 2.1 MHz maximum; $t_{CYC} = 1 \div f_{OP}$

To:

1. f_{OSC} = crystal frequency; $f_{OP} = f_{OSC} \div 2$; $t_{CYC} = 1 \div f_{OP}$ (See Table 10-6. Control Timing (V_{DD} = 5.0 Vdc).)

Delete NOTE 2 at the bottom of the table.

16. Page 10-13, **Table 10-9. SIOP Timing (V_{DD} = 3.3 Vdc)** — Change the first row as follows:

From:

Table 10-9. SIOP Timing (V_{DD} = 3.3 Vdc)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation Master Slave	$f_{SIOP(M)}$ $f_{SIOP(S)}$	0.25 dc	0.25 250	f_{OP} kHz

To:

Table 10-9. SIOP Timing (V_{DD} = 3.3 Vdc)

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation Master Slave	$f_{SIOP(M)}$ $f_{SIOP(S)}$	f_{OSC}/64 dc	f_{OSC}/8 250	MHz kHz

Change the note at the bottom of the table as follows:

From:

NOTE: f_{OP} = 1.0 MHz maximum

To:

NOTE: f_{OSC} = crystal frequency; $f_{OP} = f_{OSC} \div 2$; $t_{CYC} = 1 \div f_{OP}$ (See Table 10-7. Control Timing (V_{DD} = 3.3 Vdc).)

Literature Distribution Centers:
USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong

MOTOROLA