

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

MC68HC05P4

Addendum to
MC68HC05P4
HCMOS Microcontroller Unit
Technical Data

This addendum supplements *MC68HC05P4 Technical Data* (Motorola document number MC68HC05P4/D) with the following additional information:

- DC Electrical Characteristics
- MC68HCL05P4 data — APPENDIX A contains data for the MC68HCL05P4, a low-power version of the MC68HC05P4
- MC68HSC05P4 data — APPENDIX B contains data for the MC68HSC05P4, a high-speed version of the MC68HC05P4

Specifications and information herein are subject to change without notice.



9.4 DC ELECTRICAL CHARACTERISTICS

The following table replaces Table 9-3 in *MC68HC05P4 Technical Data*.

Table 9-3. DC Electrical Characteristics ($V_{DD} = 5.0 \text{ Vdc} \pm 10\%$)

| Characteristic | Symbol | Min | Typ ⁽¹⁾ | Max | Unit |
|--|-----------------------|---------------------|-------------------------|-------------------------|--|
| Output Voltage $I_{LOAD} = 10.0 \mu\text{A}$ $I_{LOAD} = -10.0 \mu\text{A}$ | V_{OL} V_{OH} | — $V_{DD} - 0.1$ | — — | 0.1 — | V V |
| Output High Voltage ($I_{LOAD} = -0.8 \text{ mA}$) PA7–PA0, PB7–PB5, PC7–PC0, PD5, TCMP | V_{OH} | $V_{DD} - 0.8$ | — | — | V |
| Output Low Voltage ($I_{LOAD} = 1.6 \text{ mA}$) PA7–PA0, PB7–PB5, PC7–PC0, PD5, TCMP | V_{OL} | — | — | 0.4 | V |
| Input High Voltage PA7–PA0, PB7–PB5, PC7–PC0, PD5, PD7/TCAP, <u>IRQ</u> , <u>RESET</u> , OSC1 | V_{IH} | $0.7 \times V_{DD}$ | — | V_{DD} | V |
| Input Low Voltage PA7–PA0, PB7–PB5, PC7–PC0, PD5, PD7/TCAP, <u>IRQ</u> , <u>RESET</u> , OSC1 | V_{IL} | V_{SS} | — | $0.2 \times V_{DD}$ | V |
| Data-Retention Mode Supply Voltage | V_{RM} | 2 | — | — | V |
| Supply Current Run ⁽²⁾ WAIT ⁽³⁾ STOP ⁽⁴⁾ 25 °C 0 to 70 °C (Standard) | I_{DD} | — — — — | 3.1 1.1 2.25 — | 7.0 4.0 50 140 | mA mA μA μA |
| I/O Ports High-Z Leakage Current PA7–PA0, PB7–PB5, PC7–PC0, PD5 | I_{IL} | — | — | ± 10 | μA |
| Input Current <u>RESET</u> , <u>IRQ</u> , OSC1, PD7/TCAP | I_{IN} | — | — | ± 1 | μA |
| Capacitance Ports (Input or Output) <u>RESET</u> , <u>IRQ</u> , PD5, PD7/TCAP | C_{OUT} C_{IN} | — — | — — | 12 8 | pF pF |

1. Typical values at midpoint of voltage range, 25 °C only.

2. Run (operating) I_{DD} measured using external square wave clock source ($f_{OSC} = 4.2 \text{ MHz}$). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. $C_L = 20 \text{ pF}$ on OSC2.

3. WAIT I_{DD} measured using external square wave clock source ($f_{OSC} = 4.2 \text{ MHz}$). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. $C_L = 20 \text{ pF}$ on OSC2. All ports configured as inputs. $V_{IL} = 0.2 \text{ V}$. $V_{IH} = V_{DD} - 0.2 \text{ V}$. OSC2 capacitance linearly affects WAIT I_{DD} .

4. STOP I_{DD} measured with OSC1 = V_{SS} . All ports configured as inputs. $V_{IL} = 0.2 \text{ V}$. $V_{IH} = V_{DD} - 0.2 \text{ V}$.

The following table replaces Table 9-4 in *MC68HC05P4 Technical Data*.

Table 9-4. DC Electrical Characteristics ($V_{DD} = 3.3 \text{ Vdc} \pm 10\%$)

| Characteristic | Symbol | Min | Typ ⁽¹⁾ | Max | Unit |
|--|-----------------------|---------------------|-------------------------|------------------------|--|
| Output Voltage $I_{LOAD} = 10.0 \mu\text{A}$ $I_{LOAD} = -10.0 \mu\text{A}$ | V_{OL} V_{OH} | — $V_{DD} - 0.1$ | — — | 0.1 — | V V |
| Output High Voltage ($I_{LOAD} = -0.2 \text{ mA}$) PA7–PA0, PB7–PB5, PC7–PC0, PD5, TCMP | V_{OH} | $V_{DD} - 0.3$ | — | — | V |
| Output Low Voltage ($I_{LOAD} = 0.4 \text{ mA}$) PA7–PA0, PB7–PB5, PC7–PC0, PD5, TCMP | V_{OL} | — | — | 0.3 | V |
| Input High Voltage PA7–PA0, PB7–PB5, PC7–PC0, PD5, PD7/TCAP, $\overline{\text{IRQ}}$, RESET, OSC1 | V_{IH} | $0.7 \times V_{DD}$ | — | V_{DD} | V |
| Input Low Voltage PA7–PA0, PB7–PB5, PC7–PC0, PD5, PD7/TCAP, $\overline{\text{IRQ}}$, RESET, OSC1 | V_{IL} | V_{SS} | — | $0.2 \times V_{DD}$ | V |
| Supply Current Run ⁽²⁾ WAIT ⁽³⁾ STOP ⁽⁴⁾ 25 °C 0 to 70 °C (Standard) | I_{DD} | — — — — | 0.8 0.35 0.6 — | 2.5 1.4 30 80 | mA mA μA μA |
| I/O Ports High-Z Leakage Current PA7–PA0, PB7–PB5, PC7–PC0, PD5 | I_{IL} | — | — | ± 10 | μA |
| Input Current RESET, $\overline{\text{IRQ}}$, OSC1, PD7/TCAP | I_{IN} | — | — | ± 1 | μA |
| Capacitance Ports (Input or Output) RESET, $\overline{\text{IRQ}}$, PD5, PD7/TCAP | C_{OUT} C_{IN} | — — | — — | 12 8 | pF pF |

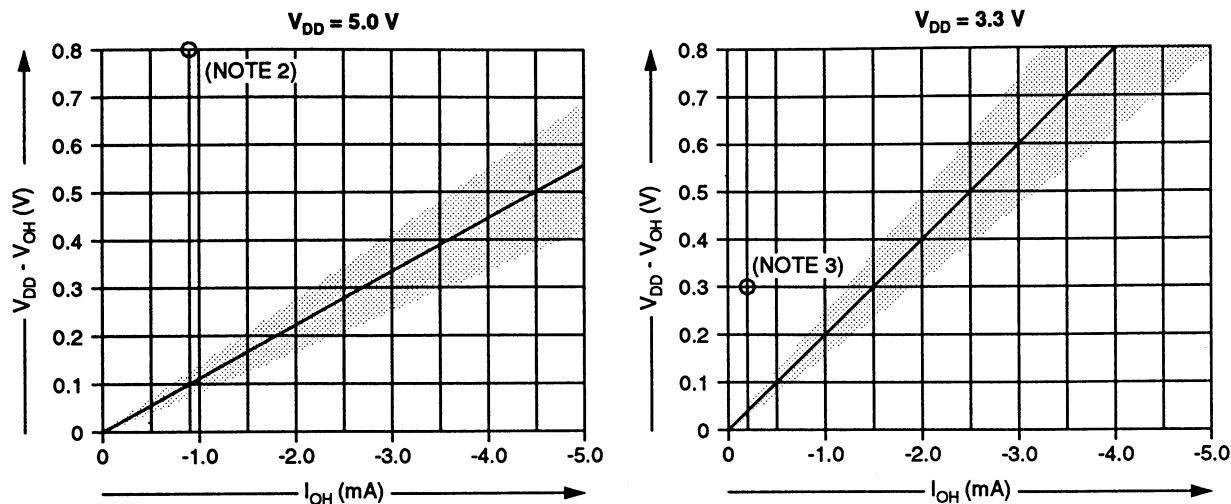
1. Typical values at midpoint of voltage range, 25 °C only.

2. Run (operating) I_{DD} measured using external square wave clock source ($f_{OSC} = 2.1 \text{ MHz}$). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. $C_L = 20 \text{ pF}$ on OSC2.

3. WAIT I_{DD} measured using external square wave clock source ($f_{OSC} = 2.1 \text{ MHz}$). All inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. $C_L = 20 \text{ pF}$ on OSC2. All ports configured as inputs. $V_{IL} = 0.2 \text{ V}$. $V_{IH} = V_{DD} - 0.2 \text{ V}$. OSC2 capacitance linearly affects WAIT I_{DD} .

4. STOP I_{DD} measured with OSC1 = V_{SS} . All ports configured as inputs. $V_{IL} = 0.2 \text{ V}$. $V_{IH} = V_{DD} - 0.2 \text{ V}$.

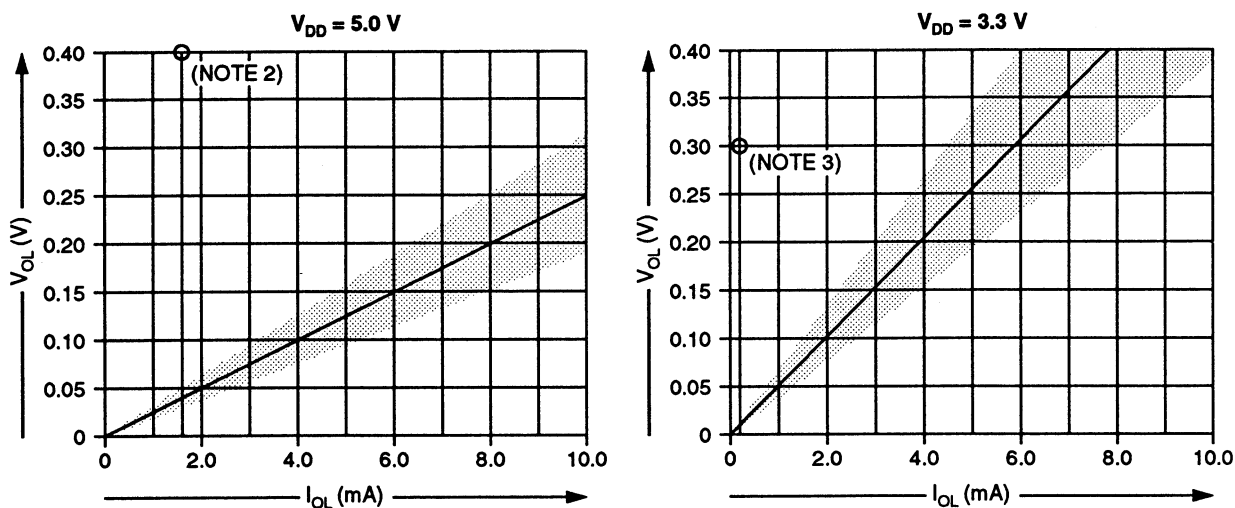
The following figures replace Figure 9-2 and Figure 9-3 of *MC68HC05P4 Technical Data*.



NOTES:

1. Shaded area indicates variation in driver characteristics due to changes in temperature and for normal processing tolerances. Within the limited range of values shown, V vs I curves are approximately straight lines.
2. At $V_{DD} = 5.0\text{ V}$, devices are specified and tested for $V_{OH} \geq V_{DD} - 800\text{ mV}$ @ $I_{OH} = -0.8\text{ mA}$.
3. At $V_{DD} = 3.3\text{ V}$, devices are specified and tested for $V_{OH} \geq V_{DD} - 300\text{ mV}$ @ $I_{OH} = -0.2\text{ mA}$.

Figure 9-2. Typical High-Side Driver Characteristics



NOTES:

1. Shaded area indicates variation in driver characteristics due to changes in temperature and for normal processing tolerances. Within the limited range of values shown, V vs I curves are approximately straight lines.
2. At $V_{DD} = 5.0\text{ V}$, devices are specified and tested for $V_{OL} \leq 400\text{ mV}$ @ $I_{OL} = 1.6\text{ mA}$.
3. At $V_{DD} = 3.3\text{ V}$, devices are specified and tested for $V_{OL} \leq 300\text{ mV}$ @ $I_{OL} = 0.4\text{ mA}$.

Figure 9-3. Typical Low-Side Driver Characteristics

The following figures replace Figure 9-4 and Figure 9-5 in *MC68HC04P4 Technical Data*.

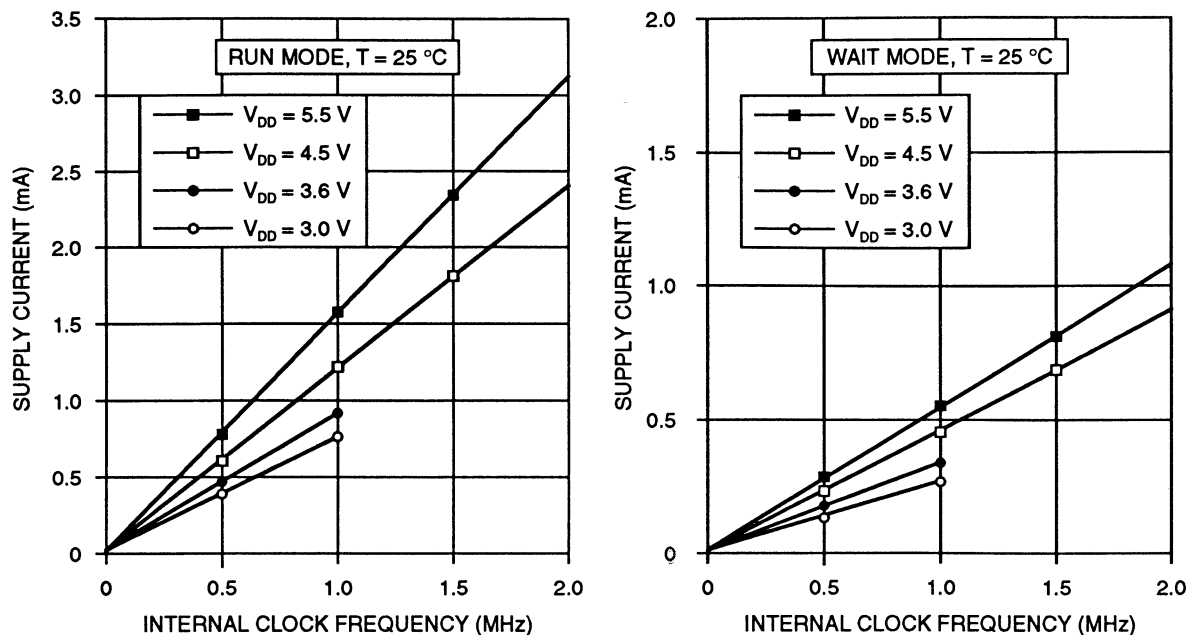
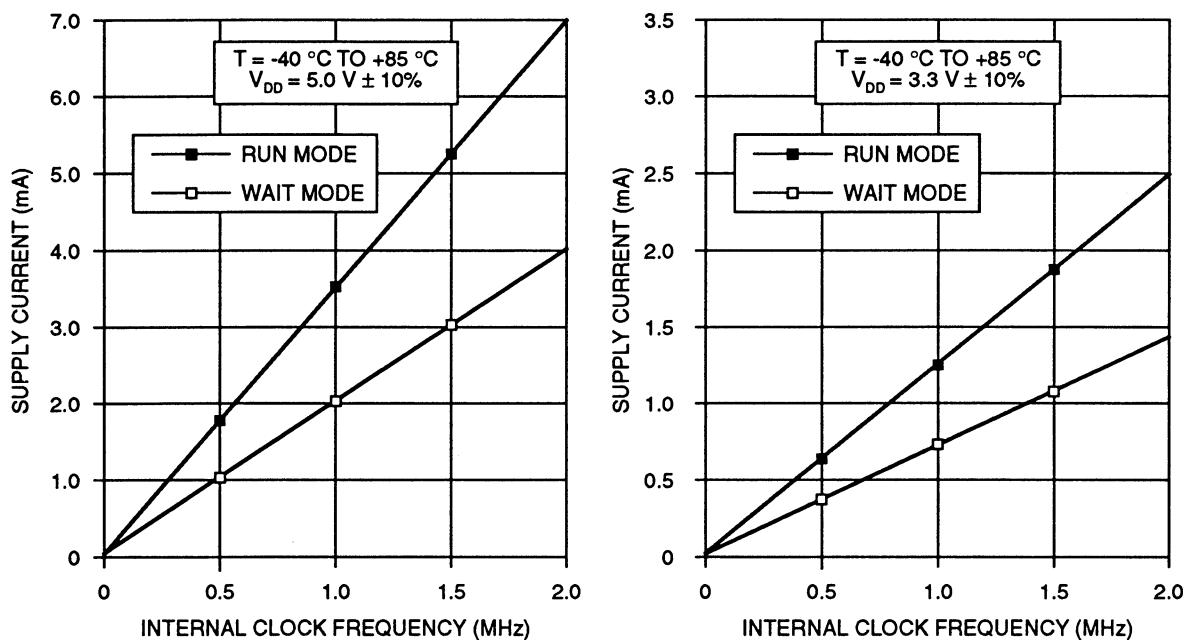


Figure 9-4. Typical Supply Current vs Internal Clock Frequency



NOTE: Maximum STOP I_{DD} = 50 μA when V_{DD} = 5 V.

NOTE: Maximum STOP I_{DD} = 50 μA when V_{DD} = 3.3 V.

Figure 9-5. Maximum Supply Current vs Internal Clock Frequency

APPENDIX A MC68HCL05P4

This appendix introduces the MC68HCL05P4, a low-power version of the MC68HC05P4. All of the information in *MC68HC05P4 Technical Data* applies to the MC68HCL05P4 with the exceptions given in this appendix.

A.1 DC ELECTRICAL CHARACTERISTICS

The data given in Table 9-3 and Table 9-4 of *MC68HC05P4 Technical Data* applies to the MC68HCL05P4 with the exceptions given in Table A-1, Table A-2, and Table A-3.

Table A-1. Low-Power Output Voltage ($V_{DD} = 1.8\text{--}2.4\text{ Vdc}$)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|----------|----------------|-----|-----|------|
| Output High Voltage ($I_{LOAD} = -0.1\text{ mA}$) PA7-PA0, PB7-PB5, PC7-PC0, PD5, TCMP | V_{OH} | $V_{DD} - 0.3$ | — | — | V |
| Output Low Voltage ($I_{LOAD} = 0.2\text{ mA}$) PA7-PA0, PB7-PB5, PC7-PC0, PD5, TCMP | V_{OL} | — | — | 0.3 | V |

Table A-2. Low-Power Output Voltage ($V_{DD} = 2.5\text{--}3.6\text{ Vdc}$)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|----------|----------------|-----|-----|------|
| Output High Voltage ($I_{LOAD} = -0.2\text{ mA}$) PA7-PA0, PB7-PB5, PC5-PC0, PD5, TCMP | V_{OH} | $V_{DD} - 0.3$ | — | — | V |
| Output Low Voltage ($I_{LOAD} = 0.4\text{ mA}$) PA7-PA0, PB7-PB5, PC5-PC0, PD5, TCMP | V_{OL} | — | — | 0.3 | V |

Table A-3. Low-Power Supply Current

| Characteristic | Symbol | Min | Typ ⁽¹⁾ | Max | Unit |
|--|----------|-----|--------------------|------|------|
| Supply Current ($V_{DD} = 4.5\text{--}5.5\text{ Vdc}$, $f_{OP} = 2.1\text{ MHz}$) | I_{DD} | | | | |
| Run ⁽²⁾ | | — | 3.1 | 4.25 | mA |
| WAIT ⁽³⁾ | | — | 1.1 | 2.25 | mA |
| STOP ⁽⁴⁾ | | | | | |
| 25 °C | | — | 2.0 | 15 | μA |
| 0 °C to 70 °C (Standard) | | — | — | 25 | μA |
| Supply Current ($V_{DD} = 2.5\text{--}3.6\text{ Vdc}$, $f_{OP} = 1.0\text{ MHz}$) | I_{DD} | | | | |
| Run ⁽²⁾ | | — | 0.8 | 1.6 | mA |
| WAIT ⁽³⁾ | | — | 0.35 | 1.0 | mA |
| STOP ⁽⁴⁾ | | | | | |
| 25 °C | | — | 0.6 | 5.0 | μA |
| 0 °C to 70 °C (Standard) | | — | — | 10.0 | μA |
| Supply Current ($V_{DD} = 2.5\text{--}3.6\text{ Vdc}$, $f_{OP} = 500\text{ kHz}$) | I_{DD} | | | | |
| Run ⁽²⁾ | | — | 400 | 800 | μA |
| WAIT ⁽³⁾ | | — | 200 | 500 | μA |
| STOP ⁽⁴⁾ | | | | | |
| 25 °C | | — | 0.6 | 5.0 | μA |
| 0 °C to 70 °C (Standard) | | — | — | 10.0 | μA |
| Supply Current ($V_{DD} = 1.8\text{--}2.4\text{ Vdc}$, $f_{OP} = 500\text{ kHz}$) | I_{DD} | | | | |
| Run ⁽²⁾ | | — | 300 | 600 | μA |
| WAIT ⁽³⁾ | | — | 200 | 400 | μA |
| STOP ⁽⁴⁾ | | | | | |
| 25 °C | | — | 0.3 | 2.0 | μA |
| 0 °C to 70 °C (Standard) | | — | — | 5.0 | μA |

1. Typical values reflect average measurements at midpoint of voltage range at 25 °C.
2. Run (operating) I_{DD} measured using external square wave clock source with all inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. $C_L = 20\text{ pF}$ on OSC2.
3. WAIT I_{DD} measured using external square wave clock source with all inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. $C_L = 20\text{ pF}$ on OSC2. All ports configured as inputs. $V_{IL} = 0.2\text{ V}$, $V_{IH} = V_{DD} - 0.2\text{ V}$. OSC2 capacitance linearly affects WAIT I_{DD} .
4. STOP I_{DD} measured with OSC1 = V_{DD} . All ports configured as inputs. $V_{IL} = 0.2\text{ V}$, $V_{IH} = V_{DD} - 0.2\text{ V}$.

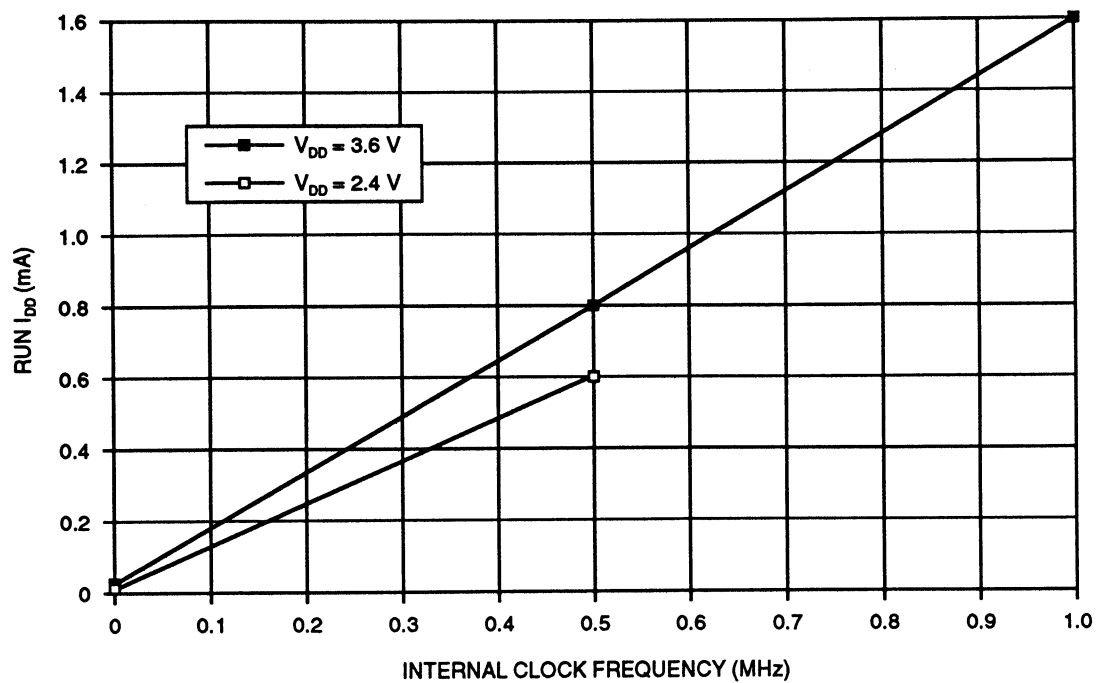


Figure A-1. Maximum Run Mode I_{DD} vs Frequency

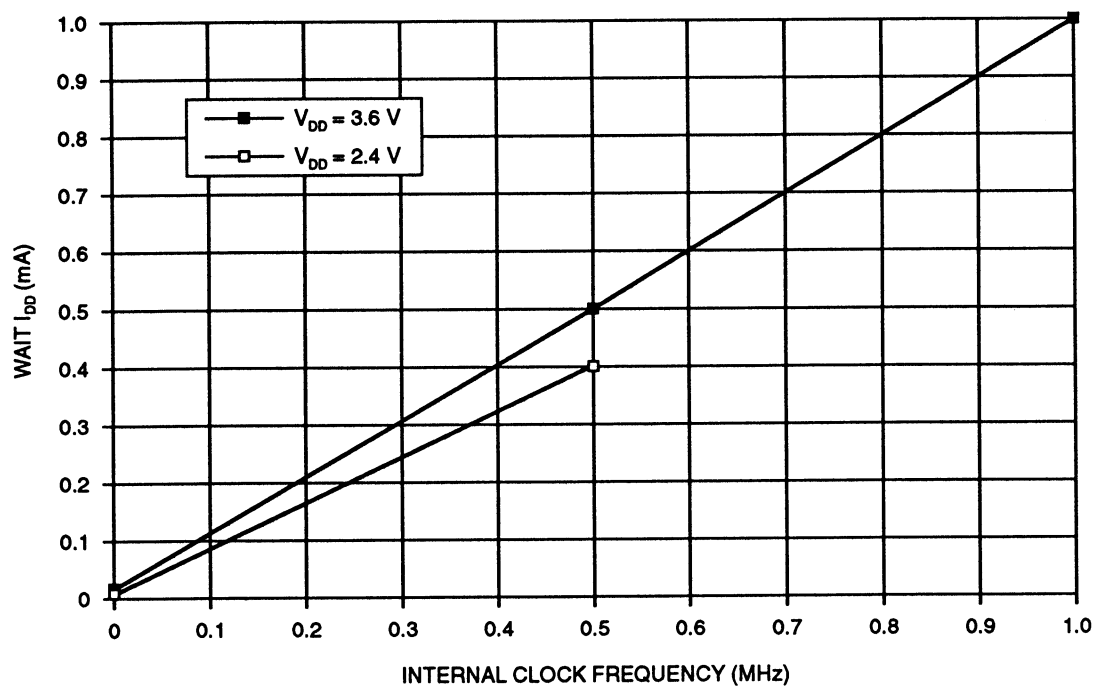


Figure A-2. Maximum WAIT Mode I_{DD} vs Frequency

A.2 MC Ordering Information

Table A-4 provides information for available package types.

Table A-4. MC Order Numbers

| Package Type | Temperature | MC Order Number |
|--|----------------|-----------------|
| 28-Pin Plastic Dual In-Line Package (DIP) | 0° C to +70° C | MC68HCL05P4P |
| 28-Pin Small Outline Integrated Circuit (SOIC) | 0° C to +70° C | MC68HCL05P4DW |

APPENDIX B

MC68HSC05P4

This appendix introduces the MC68HSC05P4, a high-speed version of the MC68HC05P4. All of the information in *MC68HC05P4 Technical Data* applies to the MC68HSC05P4 with the exceptions given in this appendix.

B.1 DC ELECTRICAL CHARACTERISTICS

The data in Table 9-3 and Table 9-4 of *MC68HC05P4 Technical Data* applies to the MC68HSC05P4 with the exceptions given in Table B-1.

Table B-1. High-Speed Supply Current

| Characteristic | Symbol | Min | Typ ⁽¹⁾ | Max | Unit |
|--|----------|-----|--------------------|-----|---------------|
| Supply Current ($V_{DD} = 4.5\text{--}5.5\text{ Vdc}$, $f_{OP} = 4.0\text{ MHz}$) | I_{DD} | | | | |
| Run ⁽²⁾ | | — | 7.0 | 9.0 | mA |
| WAIT ⁽³⁾ | | — | 2.0 | 5.0 | mA |
| STOP ⁽⁴⁾ | | — | 2.0 | 15 | μA |
| 25 °C | | — | — | 28 | μA |
| -40 to +85 °C | | | | | |
| Supply Current ($V_{DD} = 3.0\text{--}3.6\text{ Vdc}$, $f_{OP} = 2.1\text{ MHz}$) | I_{DD} | | | | |
| Run ⁽²⁾ | | — | 1.8 | 5.0 | mA |
| WAIT ⁽³⁾ | | — | 0.8 | 2.5 | mA |
| STOP ⁽⁴⁾ | | — | 0.6 | 5.0 | μA |
| 25 °C | | — | — | 12 | μA |
| -40 to +85 °C | | | | | |

1. Typical values at midpoint of voltage range, 25 °C only.

2. Run (operating) I_{DD} measured using external square wave clock source with all inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. $C_L = 20\text{ pF}$ on OSC2.

3. WAIT I_{DD} measured using external square wave clock source with all inputs 0.2 V from rail. No dc loads. Less than 50 pF on all outputs. $C_L = 20\text{ pF}$ on OSC2. All ports configured as inputs; $V_{IL} = 0.2\text{ V}$, $V_{IH} = V_{DD} - 0.2\text{ V}$. OSC2 capacitance linearly affects WAIT I_{DD} .

4. STOP I_{DD} measured with OSC1 = V_{DD} . All ports configured as inputs. $V_{IL} = 0.2\text{ V}$, $V_{IH} = V_{DD} - 0.2\text{ V}$.

B.2 CONTROL TIMING

The data given in Table 9-5 and Table 9-6 of *MC68HC05P4 Technical Data* applies to the MC68HSC05P4 with the exceptions given in Table B-2 and Table B-3.

Table B-2. High-Speed Control Timing ($V_{DD} = 5.0\text{ V} \pm 10\%$)

| Characteristic | Symbol | Min | Max | Unit |
|---|---------------------|-----|------------|------------|
| Oscillator Frequency Crystal Oscillator External Clock | f_{OSC} | dc | 8.0 8.0 | MHz MHz |
| Internal Operating Frequency ($f_{OSC} + 2$) Crystal Oscillator External Clock Option | f_{OP} | dc | 4.0 4.0 | MHz MHz |
| Internal Clock Cycle Time | t_{CYC} | 250 | | ns |
| Capture/Compare Timer Input Capture Pulse Width | t_{TH} , t_{TL} | 63 | | ns |
| Interrupt Pulse Width Low (Edge-Triggered) | t_{LUL} | 63 | | ns |
| OSC1 Pulse Width | t_{OH} , t_{OL} | 45 | | ns |

Table B-3. High-Speed Control Timing ($V_{DD} = 3.3\text{ V} \pm 10\%$)

| Characteristic | Symbol | Min | Max | Unit |
|---|---------------------|-----|------------|------------|
| Oscillator Frequency Crystal Oscillator External Clock | f_{OSC} | dc | 4.2 4.2 | MHz MHz |
| Internal Operating Frequency ($f_{OSC} + 2$) Crystal Oscillator External Clock Option | f_{OP} | dc | 2.1 2.1 | MHz MHz |
| Internal Clock Cycle Time | t_{CYC} | 480 | | ns |
| Capture/Compare Timer Input Capture Pulse Width | t_{TH} , t_{TL} | 125 | | ns |
| Interrupt Pulse Width Low (Edge-Triggered) | t_{LUL} | 125 | | ns |
| OSC1 Pulse Width | t_{OH} , t_{OL} | 90 | | ns |

B.3 SIOP TIMING

The data given in Table 9-7 and Table 9-8 of *MC68HC05P4 Technical Data* applies to the MC68HSC05P4 with the exceptions given in Table B-4 and Table B-5.

Table B-4. SIOP Timing ($V_{DD} = 5.0 \text{ V} \pm 10\%$)

| Characteristic | Symbol | Min | Max | Unit |
|---|------------|-----|-----|------|
| Clock (SCK) Low Time ($f_{OP} = 4.2 \text{ MHz}$) | t_{SCKL} | 466 | — | ns |
| SDO Data Valid Time | t_V | — | 100 | ns |
| SDO Hold Time | t_{HO} | 0 | — | ns |
| SDI Setup Time | t_S | 50 | — | ns |
| SDI Hold Time | t_H | 50 | — | ns |

Table B-5. SIOP Timing ($V_{DD} = 3.3 \text{ V} \pm 10\%$)


| Characteristic | Symbol | Min | Max | Unit |
|---|------------|-----|-----|------|
| Clock (SCK) Low Time ($f_{OP} = 2.1 \text{ MHz}$) | t_{SCKL} | 990 | — | ns |
| SDO Data Valid Time | t_V | — | 200 | ns |
| SDO Hold Time | t_{HO} | 0 | — | ns |
| SDI Setup Time | t_S | 100 | — | ns |
| SDI Hold Time | t_H | 100 | — | ns |

B.4 MC ORDERING INFORMATION

Table B-6 provides information for available package types.

Table B-6. MC Order Numbers

| Package Type | Temperature | MC Order Number |
|--|------------------------------------|---------------------------------|
| 28-Pin Plastic Dual In-Line Package (DIP) | 0° C to +70° C -40° C to +85° C | MC68HSC05P4P MC68HSC05P4CP |
| 28-Pin Small Outline Integrated Circuit (SOIC) | 0° C to +70° C -40° C to +85° C | MC68HSC05P4DW MC68HSC05P4CDW |

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