H
TEST AND DEBUG

H.1 HIGH-IMPEDANCE DIGITAL OUTPUT MODE

The MC145572 U–interface transceiver has the capability of forcing all outputs (both analog and digital) to the high–impedance state. This feature, known as the Serial Control Port High Impedance Digital Output Mode, is provided to allow in–circuit testing of other circuits or devices resident on the same PCB without requiring the removal of the MC145572.

The SCP HIDOM mode is entered by holding $\overline{\text{SCPEN}}$ low for a minimum of 33 consecutive rising edges of SCPCLK while SCP Rx is high. If SCPEN goes high or if SCP Rx goes low, the device will exit the SCP HIDOM mode and return to normal operation.

H.2 CONTROL OF TRANSMIT SIGNALS

The MC145572 permits an external microcontroller to take control of the transmit superframe framer by writing to control bits in Byte Register 8. This is very useful for debugging prototypes since the MC145572 can be forced to transmit a variety of signals regardless of the presence or lack of presence of a signal on the receive pins. **Table 4–8** summarizes these signals and the control bits.

The MC145572 can be forced to transmit SL0, SL1, SL2, SL3, SN0, TN + SN1, SN2, SN3, 10 kHz, and 40 kHz tones and alternating quats. See the description of BR8 in Section 4.4.9 for more details.

H.3 CHARACTERIZATION OF THE PULLABLE CRYSTAL

The MC145572 makes it very easy to measure the free running frequency of oscillation of the 20.48 MHz crystal oscillator and to measure its frequency pullablility. This is done by using the 20.48 MHz square wave signal on BUF XTAL OUT pin to drive a frequency counter. Make sure that this output has not been turned off. Never probe the crystal pins since the capacitance of the probe introduces severe errors in the measurement.

Also the measured frequency must be verified against the make tolerance of the crystal at 25°C. Do not include the aging and temperature tolerances of the crystal when performing free running frequency checks at room temperature. If it is desired to verify operation of the crystal oscillator over temperature then the crystal temperature tolerance should be included. The MC145572 has a typical crystal load capacitance including board traces of about 24 pF. Note that individual board implementations may change this figure slightly.

The free running frequency of oscillation of the 20.48 MHz oscillator can be characterized when the MC145572 is set to NT mode operation. In NT mode the on chip variable capacitance array is set for the nominal center frequency point when the transceiver is deactivated. A frequency of 20.48 MHz plus or minus the tolerance is measured at BUFXTAL OUT. It may be necessary to change the crystal calibration load capacitance specification slightly in order to have the free running frequency of oscillation meet the 20.48 MHz specification. The nominal crystal load capacitance is 24 pF.

The pullability of a crystal can be measured by putting the MC145572 into LT mode and changing the frequency applied to the FREQREF input pin. Any external square wave clock source can be used for this but DO NOT use a clock that is generated by, or derived from, the MC145572 on which the test is being performed since this may cause the on chip PLL to force the on chip capacitance array to its mid frequency point at all times.

To measure the pullability towards the low frequency direction pull FREQ REF to V_{DD} or V_{SS}. This causes the on chip PLL to attempt to pull the 20.48 MHz crystal towards DC. Since this is not possible the MC145572 pulls the crystal as low in frequency as possible by driving the on chip capacitance

to its maximum value. Once the frequency of oscillation has stabilized the negative direction pullability can be measured with a frequency counter at BUF XTAL OUT. If a board is designed to have a pull up resistor on FREQREF then automatic test equipment can be programmed for the low frequency measurement and to inject a high frequency clock for the high frequency measurement.

To measure the pullability towards the high frequency direction FREQ REF is driven with a square wave signal that can be between 8001 Hz and 20 MHz. Note that 8001 Hz is + 1000 ppm, which exceeds the pull range of the on chip PLL. This causes the on chip capacitance array to go to its minimum value and thereby increases the frequency of the 20.48 MHz oscillator. Once the oscillator has stabilized the frequency of oscillation is measured at BUF XTAL OUT.

It is also possible to use the 4.096 CLK OUT pin to do these measurement but it is necessary to relate the pullability in ppm to 4096 kHz instead of 20.48 MHz.

Example 1: Free running frequency of oscillation measurement at room temperature.

Configuration:

MC145572 in NT mode.

Crystal specification is 20.48 MHz ± 15 ppm. See Section B.3.2

Results:

BUF XTAL OUT measures as 20,480,307.2 Hz.

((|20,480,307.2 Hz – 20,480,000 Hz|)*1,000,000 ppm) / 20,248,000 Hz = + 15 ppm

Example 2: Oscillator pullability measurement at room temperature.

Crystal specification is ± 20.48 MHz with 360 ppm or ± 180 ppm pull between 15 and 45 pF. See Section B.3. In this example 20,480,000 MHz is used as the nominal frequency. In a real life situation it may be desirable to use the actual measured free run frequency when measuring pullability.

Configuration 1:

MC145572 in LT mode.

FREQ REF connected to V_{SS}.

Results:

BUF XTAL OUT measures as 20,475,801.6 Hz.

((|20,475,801.6 Hz – 20,480,000 Hz|)* 1,000,000 ppm) / 20,248,000 Hz = – 205 ppm.

Configuration 2:

MC145572 in LT mode.

FREQ REF connected to 4 MHz.

Results:

BUF XTAL OUT measures as 20,483,952.6 Hz.

((20,483,952.6 Hz| – 20,248,000 Hz|)* 1,000,000 ppm) / 20,248,000 Hz = + 193 ppm.

Conclusion:

Since 20.48 MHz + 193 ppm, – 205 ppm exceeds the ± 180 ppm minimum crystal pull range specification the oscillator is working correctly.