4

MCU MODE REGISTER DESCRIPTION REFERENCE

4.1 INTRODUCTION

This section describes all of the MC145572 U–interface transceiver control and status registers available via the Serial and Parallel Control Ports. Tables 4–1 through 4–3 contain Register Maps, and Section 4.2.1 contains a Register Index. **Section 4.3** follows with detailed descriptions of each register.

The internal registers of the MC145572 are used when the device is in MCU mode. When in GCI mode, MCU/GCI = 0, the MC145572 is controlled via the C/I and monitor channels and it is not necessary to access the registers in normal applications.

The MC145572 provides a Parallel Control Port interface mode that provides access to all control registers. See **Section 5.3.2** for more information on the use of the Parallel Control Port interface.

The register map for the MC145572 is nearly identical to that for the MC145472 after a hardware or software reset. Reserved bits in the MC145472 register map have been redefined to permit access to new registers in the MC145572. Most software developed for the MC145472 will work for the MC145572 without modifications.

The MC145572 Serial Control Port (SCP) Interface is pin–for–pin identical to that of the MC145474/75 and MC145574 S/T–interface transceivers. Using the same interface as the MC145474/75 provides a common interface for applications utilizing both the MC145572 and the MC145474/75 and for applications that can use either device, such as line cards or terminal equipment.

In addition to being pin–for–pin compatible, the architecture of the register map and the SCP Interface is nearly identical to that of the MC145474/75. This simplifies the code development effort and minimizes device driver code size for the microcontroller.

For complete information on the operation of the Control Interfaces see **Section 5.3**.

Table 4–1. Nibble Registers and R6 Map (NR0 – NR5; R6) — See Section 4.3

	b3	b2	b1	b0
NR0	Software Reset	Power–Down Enable	Absolute Power–Down	Return to Normal
NR1	Linkup	Error Indication	Superframe Sync	Transparent Activation in Progress
NR2	Activation Request	Deactivation Request	Superframe Update Disable	Customer Enable
NR3	IRQ3	IRQ2	IRQ1	IRQ0
NR4	Enable IRQ3	Enable IRQ2	Enable IRQ1	Enable IRQ0
NR5	Reserved	Block B1	Block B2	Swap B1/B2

	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
R6	eoc a1	eoc a2	eoc a3	eoc dm	eoc i1	eoc i2	eoc i3	eoc i4	eoc i5	eoc i6	eoc i7	eoc i8

Table 4–2. Byte Register Map (BR0 – BR15A)

	b7	b6	b5	b4	b3	b2	b1	b0
BR0	M40	M41	M42	M43	M44	M45	M46	M47
BR1	M40	M41	M42	M43	M44	M45	M46	M47
BR2	M50	M60	M51	febe Input	Reserved	Reserved	Reserved	Reserved
BR3	M50	M60	M51	Received febe	Computed nebe	Verified act	Verified dea	Superframe Detect
BR4	febe Counter 7	febe Counter 6	febe Counter 5	febe Counter 4	febe Counter 3	febe Counter 2	febe Counter 1	febe Counter 0
BR5	nebe Counter 7	nebe Counter 6	nebe Counter 5	nebe Counter 4	nebe Counter 3	nebe Counter 2	nebe Counter 1	nebe Counter 0
BR6	U–Loop B1	U–Loop B2	U–Loop 2B + D	U–Loop Transparent	IDL2–Loop B1	IDL2–Loop B2	IDL2–Loop 2B + D	IDL2–Loop Transparent
BR7	BR15A Select	**OUT2**	**OUT1**	IDL2 Invert	IDL2 Free Run	IDL2 Speed	IDL2 M/S Invert	IDL2 8/10
		GCI IN2	**GCI IN1**					
BR8	Frame Steering	Frame Control 2	Frame Control 1	Frame Control 0	crc Corrupt	Match Scrambler	Receive Window Disable	NT/LT Invert
	Frame State 3	Frame State 2	Frame State 1	Frame State 0	Reserved	Reserved	Reserved	NT/LT Mode
BR9	eoc Control 1	eoc Control 0	M4 Control 1	M4 Control 0	M5/M6 Control 1	M5/M6 Control 0	febe/nebe Control	Reserved
BR10	Reserved	Reserved	Reserved	Reserved	Reserved	Select Dump Access	Select DCH Access	Select Overlay
BR11	Activation Control 6	Activation Control 5	Activation Control 4	Activation Control 3	Activation Control 2	Activation Control 1	Activation Control 0	Activation Timer Disable
	Activation State 6	Activation State 5	Activation State 4	Activation State 3	Activation State 2	Activation State 1	Activation State 0	Activation Timer Expire
BR12	Activation Control Register	Interpolate Enable	Load Activation State	Step Activation State	Hold Activation State	Jump Select	Reserved	Force Linkup
	EPI 18	EPI 17	EPI 16	EPI 15	EPI 14	EPI 13	EPI 12	EPI 11
BR13	Enable MEC Updates	Accumulate EC Output	Enable EC Updates	Fast EC Beta	Accumulate DFE Output	Enable DFE Updates	Fast DFE/ ARC Beta	Clear All Coefficients
	EPI 10	EPI 9	EPI 8	EPI 7	EPI 6	EPI 5	EPI 4	EPI 3
BR14	Reserved	ro/wo to r/w	Reserved	Framer to Deframer Loop	± 1 Tones	Reserved	Reserved	Enable CLKs
BR15	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
	Mask 7	**Mask 6**	**Mask 5**	Mask 4	Mask 3	Mask 2	Mask 1	Mask 0
BR15A	FREQ ADAPT	Jump Disable	Reserved	Reserved	Enable Tx SFS	Reserved	Reserved	Enable Eye Data and Baud Clock
				Reserved	Reserved	Reserved	Reserved	Reserved

NOTE: Bits in bold type were reserved bits in the MC145472/MC14LC5472 register map.

Table 4–3. Overlay Register Map (OR0 – OR13)

INIT GROUP REGISTER OVERLAY REGISTERS OR0 – OR9, OR11, AND OR12								
	b7	**b6**	**b5**	**b4**	**b3**	**b2**	**b1**	**b0**
OR0	D_{out} B1 Channel Timeslot Bits (7:0)							
OR1	D_{out} B2 Channel Timeslot Bits (7:0)							
OR2	D_{out} D Channel Timeslot Bits (7:0)							
OR3	D_{in} B1 Channel Timeslot Bits (7:0)							
OR4	D_{in} B2 Channel Timeslot Bits (7:0)							
OR5	D_{in} D Channel Timeslot Bits (7:0)							
						GCI Slot (2:0)		
OR6	TSA B1 Enable	TSA B2 Enable	TSA D Enable	GCI Select M4 – OR0	GCI Mode Enable	Reserved	Reserved	Reserved
OR7	Internal Analog Loopback	Line Connect	$\overline{\text{TSEN}}$ D Channel Enable	IDL2 Rate 2	IDL2 Long Frame Mode	crc Corrupt Mode	febe/nebe Rollover	M4 Trinal Mode
OR8	D/R Mode 1	D/R Mode 0	SFAX Output Enable	FREQREF Output Enable	$\overline{\text{TSEN}}$ Enable B1, B2	Reserved	SFAX SFAR Enable	D Channel Port Enable
OR9	Reserved	Open Feedback Switches	Analog Loopback	CLKOUT 2048	4096 Hirate	2048 Disable	1536 Disable	4096 Disable
BR10	Reserved	Reserved	Reserved	Reserved	Reserved	**Select Dump Access**	**Select DCH Access**	**Select INIT Group**
D Channel Access Select Overlay								
OR12	D Channel Transmit Bits (7:0)							
	D Channel Receive Bits (7:0)							
Dump/Restore Access Select Overlay								
OR13	Dump Register Write Access (7:0)							
	Dump Register Read Access (7:0)							

4.2 REGISTER MAP

The Register Map consists of six 4–bit Nibble Registers (NR0 – NR5), one 12–bit Nibble Register (R6), seventeen Byte Registers (BR0 – BR15A), and twelve Overlay Registers (OR0 – OR9, OR11, and OR12).

4.2.1 Register Index

The following guide lists the registers alphabetically by functional groups and indicates which register number, NR0 – NR5, R6, or BR0 – BR15A, and bit or bits, (b7:b0), to refer to for detailed information.

Activation

Control — BR11(b7:b1)
Control Steer — BR12(b7)
Customer Enable — NR2(b0)
Deactivation Request — NR2(b2)
Error Indication — NR1(b2)
Error Power Indicator — BR12, BR13
Force Linkup — BR12(b0)
Hold Activation State — BR12(b3)
In Progress — NR1(b0)
Jump Select — BR12(b2)
Linkup — NR1(b3)
Load Activation State — BR12(b5)
Request — NR2(b3)
State — BR11(b7:b1)

Diagnostics

± 1 Tones — BR14(b3)
Accumulate DFE Output — BR13(b3)
Accumulate EC Output — BR13(b6)
Clear All Coefficients — BR13(b0)
Enable Clocks — BR14(b0)
Enable DFE Updates — BR13(b2)
Enable EC Updates — BR13(b5)
Enable Eye Data and Baud Clock — BR15A(b0)
Enable MEC Updates — BR13(b7)
Enable Tx SFS — BR15A(b3)
Enable 15.36 MHz — BR15A(b2)
Enable 20.48 MHz — BR15A(b1)
Error Power Indicator — BR12, BR13
Fast DFE/ARC Beta — BR13(b1)

Activation (continued)
Step Activation State — BR12(b4)
Superframe Sync — NR1(b1)
Superframe Update Disable — NR2(b1)
Timer Disable — BR11(b0)
Timer Expire — BR11(b0)
Transparent — NR1(b0)
Verified act — BR3(b2), BR9(b5:b4)
Verified dea — BR3(b1), BR9(b5:b4)
Deactivation
Request — NR2(b2)
GCI
IN/OUT — BR7(b6:b5)
GCI Mode Enable — OR6 (b3)
IDL2
Timeslot Assigner
D_{out} B1 Timeslot — OR0
D_{out} B2 Timeslot — OR1
D_{out} D Timeslot — OR2
D_{in} B1 Timeslot — OR3
D_{in} B2 Timeslot — OR4
D_{in} D Timeslot — OR5
TSA Enable — OR6 (b7:b5)
8–Bit/10–Bit Mode — BR7(b0)
Block B1 — NR5(b2)
Block B2 — NR5(b1)
Customer Enable — NR2(b0)
Free Run — BR7(b3)
Invert — BR7(b4)
Loopbacks — See loopbacks
Master/Slave Invert — BR7(b1)
Speed — BR7(b2)
Swap B1/B2 — NR5(b0)
B1 IDL2 Timeslot Enable — OR6(b7)
B2 IDL2 Timeslot Enable — OR6(b6)
D IDL2 Timeslot Enable — OR6(b5)
IDL2 Long Frame Mode — OR7(b3)
IDL2 Rate OR7(b4)
Interrupt
Enable — NR5
Status — NR3
Loopbacks
Framer to Deframer Loop — BR14(b4)
IDL2–Loop 2B + D — BR6(b1)
IDL2–Loop B1 — BR6(b3)
IDL2–Loop B2 — BR6(b2)
IDL2–Loop Transparent — BR6(b1)
Match Scrambler — BR8(b2)
Receive Window Disable — BR8(b1)
U–Loop 2B + D — BR6(b5)
U–Loop B1 — BR6(b7)
U–Loop B2 — BR6(b6)
U–Loop Transparent — BR6(b4)
Open Feedback Switch — OR9(b6)
Analog Loopback — OR9(b5)
nebe
Computed — BR3(b3)
Control — BR9(b1)
Counter — BR5
febe/nebe Rollover — OR7(b2)
Diagnostics (continued)
Fast EC Beta — BR 13(b4)
Force Linkup — BR12(b0)
Freq Adapt — BR15A(b7)
Jump Disable — BR15A(b6)
Mask — BR15(b4:b0)
ro/wo to r/w — BR14(b6)
Superframe Detect — BR3(b0)
Select Dump Access — BR10(b2)
Select DCH Access — BR10(b1)
D Channel Access Overlay — OR12
Dump/Restore Access Overlay — OR13
eoc
Control — BR9(b7:b6)
act — BR3(b2)
Message — R6
febe
Control — BR9(b1)
Counter — BR4
Input — BR2(b4), BR9(b1)
Received — BR3(b4)
febe/nebe Rollover OR7(b2)
Maintenance
act — BR3(b2)
crc Corrupt — BR8(b3)
dea — BR3(b1)
eoc — See eoc
febe — See febe
M4 Trinal Mode — OR7(b0)
M4 Control — BR9(b5:b4)
M4 Send — BR0
M4 Received — BR1
M5/M6 Control — BR9(b3:b2)
M50 Received — BR3(b7)
M50 Send — BR2(b7)
M51 Received — BR3(b5)
M51 Send — BR2(b5)
M60 Received — BR3(b6)
M60 Send — BR2(b6)
nebe — See nebe
Return to Normal — NR0(b0)
Superframe Update Disable — NR2(b1)
Verified act — BR3(b2)
Verified dea — BR3(b1)
Mode
Absolute Power–Down — NR0(b1)
NT/LT Invert Mode — BR8(b0)
NT/LT Mode — BR8(b0)
Power–Down Enable — NR0(b2)
Software Reset — NR0(b3)
GCI 2B+D Mode — OR6(b3)
Superframe Framer
Frame Control — BR8(b6:b4)
Frame State — BR8(b7:b4)
Frame Steering — BR8(b7)

4.2.2 Bit Description Legend

Each bit described in the following sections has a read/write indicator associated with it. This indicator, shown in the lower right corner of each bit, shows what type of bit resides there. The options are described in Table 4–4.

Table 4–4. Bit Read/Write Indicator

Indicator	Type	Description
rw	Read/Write	A Read/Write bit may be written to by the external microcontroller. The information that is read back will be the data that was written.
ro	Read Only	A Read Only bit may be read by the external microcontroller. Writing to it has no effect unless otherwise specified in the text. When the text says that an “ro” bit is set or cleared, this operation is performed internally.
ro/wo	Read Only/Write Only	A Read Only/Write Only bit may be written to by the external microcontroller. However, the value that is read back by the external microcontroller is not necessarily the value that was written. An “ro” bit is set and cleared by some internal operation in the U–interface transceiver.

NOTE

Byte Register 14 includes a bit (BR14(b6)) that converts all of the write only (wo) registers to read/write registers for diagnostic purposes. If not specified, a register is not affected by BR14(b6) and operates as discussed for all modes.

4.3 NIBBLE REGISTERS

4.3.1 NR0: Reset and Power-Down Register

This register contains read/write control bits. All bits are cleared on Hardware Reset ($\overline{\text{RESET}}$), but are unaffected by Software Reset (NR0(b3)). This register is write–only when the U–interface transceiver is in Absolute Power–Down mode (NR0(b1)).

CAUTION

NR0 should not be modified while device is in GCI Mode.

	b3	b2	b1	b0
NR0	SOFTWARE RESET rw	POWER–DOWN ENABLE rw	ABSOLUTE POWER–DOWN rw	RETURN TO NORMAL rw

Software Reset

This bit forces the U–interface transceiver into a reset state. Setting this bit to 1 causes a software reset. To allow the Transceiver to resume operation, this bit must be cleared by either writing a 0 to it or asserting hardware reset. Reset must be asserted for at least six 20.48 MHz clock periods. There must be a 20.48 MHz clock at $XTAL_{in}$ for the MC145572 to reset correctly. This bit has no effect on the contents of NR0 and BR10.

Power–Down Enable

When this bit is set to 1 and the U–interface transceiver is searching for a wake–up tone from the far end tranceiver, the MC145572 enters the Power–Down mode. In Power–Down mode the MC145572 transmit drivers and the time division multiplex interface circuitry for both IDL2 and GCI operation are turned off. This bit must be cleared to 0 before enabling the MC145572 to perform any non–activation related functions other than waiting for a wake up tone. The MC145572 automatically exits from Power–Down mode on one of three conditions:

1. A wake–up tone is detected on the U–interface.

2. The external microcontroller sets the Activation Request bit (NR2(b3)).
3. This bit is reset to 0.

When this bit is 0, the U–interface transceiver is not permitted to enter power–down mode. The U–interface transceiver has warm start capability regardless of the state of this bit.

Absolute Power–Down

When this bit is 1, the U–interface transceiver enters its Absolute Power–Down mode, the equivalent of a software reset. All clocks except the Phase Locked Loop (PLL) subsystem used in the LT mode are shut off when this bit is set to 1. In NT mode the oscillator is turned off. All internal bias currents are turned off and the transmit drivers are high impedance. After setting this bit back to 0, the internal circuits resume full power. After this bit is cleared, the Software Reset bit must be set to 1 for approximately 1 ms while the internal clocks stabilize. Absolute Power–Down may also be aborted by a Hardware Reset (RESET). During Absolute Power–Down, NR0 is the only register that may be written to. Setting this bit clears all coefficients and forces the Transceiver to activate in cold start mode during the next activation procedure.

Return to Normal

This bit is used to return maintenance functions to their normal operating state. When set to 1, the `crc` Corrupt bit (BR8(b3)) and all of the loopback control bits in BR6 are cleared.

4.3.2 NR1: Activation Status Register

This register contains device activation status. All bits are cleared on Software Reset (NR0(b3)) or Hardware Reset (RESET). If any bit in this register changes from 0 to 1, or if Linkup, Superframe Sync, or Transparent/Activation in Progress change from 1 to 0, an IRQ3 (NR3(b3)) is generated. The IRQ3 interrupt is cleared by reading NR1.

	b3	b2	b1	b0
NR1	LINKUP r0	ERROR INDICATION ro	SUPERFRAME SYNC ro	TRANSPARENT ACTIVATION IN PROGRESS ro

NOTE

When access to the D channel via register OR12 is enabled, NR1 indicates a D channel interrupt by setting all four status bits to 1s. Reading OR12 clears the special code (1111) from NR1 but does not affect any updates in activation status. So, if there has been a change in activation status, an interrupt is still queued up even though the D channel interrupt has been cleared.

Linkup

This bit is set when the U–interface transceiver has completed an activation up to the point where full–duplex operation of the U–interface has been established. For the ANSI T1.601–1992 defined activation to be completed, the `act` bit in the M4 maintenance bits must still be exchanged. However, from purely a transmit/receive point of view, the U–interface is operational when Linkup is 1. Linkup will remain set until one of four things happens:

1. Receive framing is lost or severely in error, and remains so, for 480 ms.
2. While operating in the NT mode, receive framing is lost after Deactivate Request is set in NR2(b2), or Verified `dea` (BR3(b1)) becomes a 1 during M4 Control Mode 0,0 (BR9(b5:b4)).
3. While operating in the LT mode, the Deactivate Request bit (NR2(b2)) is set.
4. A hardware or software reset occurs.

See ***D Channel Interrupt*** below for operation of this bit when D channel access has been enabled by setting BR10(b1).

Error Indication

This bit is set to 1 when a timer expires. Time–out sources are:

1. 15 second Activation Timer (BR11(b0)).
2. 480 ms loss of frame/signal.
3. Failure to get NT1 response to the TL signal (10 ms following the cessation of TL. TL is 3 ms in duration).

Error Indication is always automatically reset prior to the next IRQ3. This is the result of either setting the Activate Request bit in NR2(b3) or receiving a wakeup tone. Error Indication is not cleared by reading NR1.

See ***D Channel Interrupt*** below for operation of this bit when D channel access has been enabled by setting BR10(b1).

Superframe Sync

This bit is 1 when the received superframe is being reliably detected. It transitions from 0 to 1 coincident with Linkup being set. Subsequently, if the superframe is lost, Superframe Sync returns to 0, and if Superframe Sync remains 0 for 480 ms, the U–interface transceiver will deactivate. While Superframe Sync is 0, the received maintenance bits are unknown. IRQ2, IRQ1, and IRQ0 are not generated while Superframe Sync is 0. The 2B+D data is blocked (forced to all 1s) when Superframe Sync is 0.

See ***D Channel Interrupt*** below for operation of this bit when D channel access has been enabled by setting BR10(b1).

Transparent/Activation in Progress

This bit has a dual purpose. When the Transceiver is deactivated, this bit is 0. Whenever an activation begins, this bit is internally set to 1, and an IRQ3 is generated. When the activation process is completed, Linkup is set to 1 indicating success, and this bit remains set to 1, indicating that the receiver and Superframe Deframer are ready to pass data transparently from the U–interface to the IDL2 interface. If the activation process fails, this bit is cleared and Error Indication is set to 1. Whenever Linkup is 1, this bit may be cleared, indicating that the receiver has detected a high error on the U–interface. Under this condition, the receiver blocks received data (forcing the 2B+D data to all 1s) until the error returns to normal.

See ***D Channel Interrupt*** below for operation of this bit when D channel access has been enabled by setting BR10(b1).

NOTE

The received data is not transmitted on the IDL2 interface until Linkup is 1, Superframe Sync is 1, Transparent/Activation in Progress is 1, and either Customer Enable (see NR2(b0)) or Verified `act` (see BR3(b2)) is 1.

D Channel Interrupt

When access to the D channel Register OR12 has been enabled by setting BR10(b1), the operation of the NR1 status bits is modified. A D channel available status is indicated by NR1(b3:b0) all being set to 1s. Software must first do a check for NR1 = $F then perform a check for status of the individual bits. The D channel interrupt is cleared by reading OR12.

4.3.3 NR2: Activation Control Register

Register NR2 contains activation/deactivation control bits. All bits are cleared on Software Reset (NR0(b3)) or Hardware Reset (RESET).

CAUTION

NR2 normally is not written to in GCI mode; if necessary, NR2 can be written to, but bits b3 and b2 should always be written as 0 while the device is in GCI Mode.

	b3	b2	b1	b0
NR2	Activation Request rw	Deactivation Request rw	Superframe Update Disable rw	Customer Enable rw

Activation Request

When this bit is set to 1, and the U–interface transceiver is in ANSI T1.601–1992 defined “Full Reset”, the Transceiver will begin an activation. The external microcontroller never needs to set this bit to 0. The bit is internally set to 0 whenever Transparent/Activation in Progress (NR1(b0)) is set to 1, whenever TL is transmitted in the LT mode, or on hardware or software reset. If the activation fails for any reason, the Activation Request bit must be set to 1 once again to initiate another activation attempt. The Transceiver self–activates if an incoming tone is detected when in LT or NT mode. Once activation starts, the MC145572 automatically clears this bit. Do not continuously reassert this bit. It only needs to be set once per activation attempt.

Deactivation Request

When this bit is set to 1 in the LT mode, upon reaching Linkup = 1 the U–interface transceiver will halt transmission and proceed to ANSI T1.601 defined “Tear Down”, state H10 or J10, following three complete superframes. The deactivation sequence can be aborted if the Deactivate Request bit is set back to 0 prior to completion of three transmitted superframes. In the NT mode, the Deactivate Request bit is set to 1 by the external microcontroller in response to a received `dea` bit on the M4 channel, which indicates to the U–interface transceiver that this is a normal deactivation attempt. In this case, the MC145572 will reactivate in the warm start mode. In NT mode the MC145572 automatically clears this bit upon deactivation. In LT mode this bit is not cleared prior to starting the next activation and must be cleared when the MC145572 is deactivated.

Superframe Update Disable

This bit tells the Superframe Framer whether or not to update the maintenance bits M40–M47, M50, M51, and M60, which are being transmitted with the new bits that have been loaded in the control registers. In normal operation, this bit is always set to 0, allowing the transmitted bits to be updated at the transmit superframe boundary with the maintenance channel data in registers BR0 and BR2(b7:b4). The exception to this is during a deactivation in the LT mode. The Transceiver can be forced to send exactly three superframes of updated M4 channel data before it deactivates. In that sequence of operations, the Superframe Update Disable bit is first set to 1. The M4 maintenance bits are then written by the external microcontroller to the proper setting for deactivation. The Superframe Update Disable bit is set to 0, and the Deactivate Request bit in NR2(b2) is set to 1 by the external microcontroller. This guarantees that the U–interface transceiver will send exactly three superframes of updated M4 data before the activation state controller shuts everything down. Note that Superframe Update Disable does not affect the transmitted eoc, `febe`, or `crc` maintenance bits.

Customer Enable

When this bit is set to 1, it permits the U–interface transceiver to pass 2B+D data transparently. During the activation procedure, the Customer Enable bit normally is set to 0. Only after the U–interface transceiver has reached full–duplex operation and the `act` bits of the M4 maintenance channel have been properly exchanged should the Customer Enable bit be set to 1. See BR9(b5:b4), M4 Control Bits, for another way to achieve 2B+D data transparency.

4.3.4 NR3: Interrupt Status Register

This is the interrupt status register, and it is read only. All bits are cleared on Software Reset (NR0(b3)) or Hardware Reset (RESET). Each interrupt status bit in the register operates the same. If it is 1 and its corresponding interrupt enable is 1 in Register NR4, the IRQ pin on the chip will become active. IRQ3 has the highest priority and IRQ0 has the lowest.

	b3	b2	b1	b0
NR3	IRQ3 ro	IRQ2 ro	IRQ1 ro	IRQ0 ro

IRQ3

This interrupt is set whenever there is a state change in NR1 and is cleared by reading NR1. If this bit is set by the D channel register interrupt, it is cleared once OR12 has been read, unless there has been a change in activation status.

IRQ2

This interrupt is dedicated to the Embedded Operations Channel (eoc). Whenever the eoc buffer, Register R6, is updated by the Superframe Deframer, this bit is set. The loading of the eoc buffer is dependent on its mode of operation. See Register BR9(b7:b6) for details of when the buffer is loaded. To clear the interrupt, it is necessary to read Register R6, the eoc buffer register. IRQ2 is asserted at the end of the fourth and eighth basic frame of a superframe.

IRQ1

This interrupt is dedicated to the received M4 maintenance bits. This bit is set whenever the M4 buffer, Register BR1, is updated. The updating of the M4 buffer is dependent on its mode of operation. See Register BR9(b5:b4) for details of when the buffer is updated. To clear the interrupt it is necessary to read Register BR1, which is the M4 receive buffer. IRQ1 is asserted at the end of every superframe.

IRQ0

This interrupt is dedicated to the received M50, M51, and M60 bits from basic frames 1 and 2 that are buffered in Register BR3. Whenever these bits in Register BR3 are updated, this interrupt bit is set. The updating of BR3 is dependent on its mode of operation. See Register BR9(b3:b2) for details of when the buffer is updated. To clear the interrupt, it is necessary to read Register BR3. IRQ0 is asserted at the end of the fourth received basic frame of a superframe.

4.3.5 NR4: Interrupt Mask Register

This is the interrupt mask register. All bits are cleared on Software Reset (NR0(b3)) or Hardware Reset (RESET). Each bit operates in the the same manner. For example, if Enable IRQ1 is set to 1 by the external microcontroller and the IRQ1 interrupt bit is set to 1 in NR3, the IRQ pin becomes active when there is a change in activation status or there is a D channel interrupt when D channel register OR12 is updated.

	b3	b2	b1	b0
NR4	Enable IRQ3 rw	Enable IRQ2 rw	Enable IRQ1 rw	Enable IRQ0 rw

4.3.6 NR5: IDL2 Data Control Register

This register contains controls for the IDL2 interface. More IDL2 controls are in Registers BR6, BR7 and OR0–OR9. All bits are cleared on Software Reset (NR0(b3)) or Hardware Reset (RESET). See Figures 4–4 and 4–5 in the Register BR6 description for clarification regarding the precedence of the swap and blocking functions listed in this register.

CAUTION

Reserved bit b3 should be set to 0 at all times to maintain future compatibility.

	b3	b2	b1	b0
NR5	Reserved rw	Block B1 rw	Block B2 rw	Swap B1/B2 rw

Block B1

When this bit is 1 and the IDL2 Invert (BR7(b4)) is 0, the B1 channel is forced to transmit 1s on the IDL2 interface. 0s are transmitted in the B1 timeslot when IDL2 Invert (BR7(b4)) is 1. Data received on the B1 channel from the IDL2 interface is still transmitted normally through the U–interface. The B1 designator on this bit always refers to the IDL2 interface. Therefore, even if bit Swap B1/B2 (NR5(b0)) is 1, data in the first B channel timeslot on the IDL2 interface is the data that is blocked.

Block B2

When this bit is 1 and the IDL2 Invert (BR7(b4)) is 0, the B1 channel is forced to transmit 1s on the IDL2 interface. 0s are transmitted in the B2 timeslot when IDL2 Invert (BR7(b4)) is 1. Data received on the B2 channel from the IDL2 interface is still transmitted normally out of the U–interface. The B2 designator on this bit always refers to the IDL2 interface. Therefore, even if bit Swap B1/B2 (NR5(b0)) is 1, data in the second B channel timeslot on the IDL2 interface is the data that is blocked.

Swap B1/B2

When this bit is 1, the IDL2 interface performs a swap of the B channels from the U–interface to the IDL2 interface and from the IDL2 interface to the U–interface.

4.3.7 R6: eoc Data Register

This register is 12 bits long to match the length of the eoc message. Refer to Tables 4–5 and 4–6. to see how the eoc bits in this register map to the superframe. Operation of Register R6 depends on the setting of the eoc control bits in BR9(b7:b6) and BR14(b6). This register is double buffered for read and write operations.

In the default mode (BR14(b6) is 0), R6 performs as a read only/write only register. Data that is read from R6 by the external microcontroller is the eoc message that the Superframe Deframer stores according to the eoc Control Register (BR9(b7:b6)). Data that is written to R6 is stored in a latch contained in the Superframe Framer and is subsequently transmitted beginning on the next transmit eoc frame boundary. The Superframe Framer latches are set to 1s on hardware or software resets. The Superframe Update Disable Register, NR2(b1), has no effect on this register.

	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
R6	eoc a1 ro/wo	eoc a2 ro/wo	eoc a3 ro/wo	eoc dm ro/wo	eoc i1 ro/wo	eoc i2 ro/wo	eoc i3 ro/wo	eoc i4 ro/wo	eoc i5 ro/wo	eoc i6 ro/wo	eoc i7 ro/wo	eoc i8 ro/wo

When BR14(b6) is set to 1, the Superframe Framer register that contains the transmit eoc message bits becomes a read/write register. Therefore, the data that is written to the Superframe Framer may be read back through R6. In this mode, the received eoc message is not available.

Table 4–5. Register Bit Locations within the Superframe LT → NT

	Framing	2B+D	Overhead Bits (M1–M6)					
QUAT Positions	**1 – 9**	**10 – 117**	**118s**	**118m**	**119s**	**119m**	**120s**	**120m**
Bit Positions	**1 – 18**	**19 – 234**	**235**	**236**	**237**	**238**	**239**	**240**
Basic Frame #	**Sync Word**	**2B+D**	**M1**	**M2**	**M3**	**M4**	**M5**	**M6**
1	ISW	12 x 2B+D	eoc a1	eoc a2	eoc a3	act	1	1
2	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	dea	1	febe
3	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	sco	crc1	crc2
4	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	1	crc3	crc4
5	SW	12 x 2B+D	eoc a1	eoc a2	eoc a3	1	crc5	crc6
6	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	1	crc7	crc8
7	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	uoa	crc9	crc10
8	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	aib	crc11	crc12

act = start up bit, set = 0 during start up.
aib = alarm indication bit (set = 0 to indicate interruption)
crc = cyclic redundancy check: covers 2B + D + M4
dea = turn off bit (set = 0 to indicate turn off)
1 = reserved bit for future standard (set = 1)
sco = 0 start on command only
eoc = embedded operations channel
a = address bit
dm = data/message indicator (0 = data, 1 = message)
febe = far end block error
uoa = U–only–activation

Table 4–6. Register Bit Locations within the Superframe NT → LT

	Framing	2B+D	Overhead Bits (M1–M6)					
QUAT Positions	**1 – 9**	**10 – 117**	**118s**	**118m**	**119s**	**119m**	**120s**	**120m**
Bit Positions	**1 – 18**	**19 – 234**	**235**	**236**	**237**	**238**	**239**	**240**
Basic Frame #	**Sync Word**	**2B+D**	**M1**	**M2**	**M3**	**M4**	**M5**	**M6**
1	ISW	12 x 2B+D	eoc a1	eoc a2	eoc a3	act	1	1
2	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	ps1	1	febe
3	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	ps2	crc1	crc2
4	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	ntm	crc3	crc4
5	SW	12 x 2B+D	eoc a1	eoc a2	eoc a3	cso	crc5	crc6
6	SW	12 x 2B+D	eoc dm	eoc i1	eoc i2	1	crc7	crc8
7	SW	12 x 2B+D	eoc i3	eoc i4	eoc i5	sai	crc9	crc10
8	SW	12 x 2B+D	eoc i6	eoc i7	eoc i8	nib	crc11	crc12

act = start up bit, set = 1 during start up.
crc = cyclic redundancy check: covers 2B + D + M4
cso = cold start only (set = 1 for cold start only)
eoc = embedded operations channel
a = address bit
dm = data/message indicator (0 = data, 1 = message)
febe = far end block error
ntm = NT in test mode bit (set = 0 to indicate test mode)
ps1, ps2 = power status bits, (set = 0 to indicate power problems)
sai = S–activation indicator bit (optional, set = 1 for S/T activity)
nib = network indicator bit

4.4 BYTE REGISTERS

4.4.1 BR0: M4 Transmit Data Register

This register contains the M4 bits that are framed and sent by the Superframe Framer. The bits written to this register are sent out on the next transmit Superframe boundary if Superframe Update Disable (NR2(b1)) is set to 0. This register is double buffered. All bits are set to 1s following a Hardware Reset (RESET) or Software Reset (NR0(b3)). This register is replaced by Register OR0 when BR10(b0) = 1.

CAUTION

BR0 should not be modified while device is in GCI Mode. See OR6(b4).

	b7	b6	b5	b4	b3	b2	b1	b0
BR0	M40 rw	M41 rw	M42 rw	M43 rw	M44 rw	M45 rw	M46 rw	M47 rw

Table 4–7 shows the definitions of the M4 bits as defined by ANSI T1.601–1992 for the Network to NT channel and the NT to Network channel.

Table 4–7. M4 Bit Definitions

M4 Bits	Network to NT	NT to Network
M40	act	act
M41	dea	ps1
M42	sco**	ps2
M43	1*	ntm
M44	1*	cso
M45	1*	1*
M46	[uoa]	[sai]
M47	[aib]	nib**

* These bits are presently reserved by ANSI T1.601–1988 and should be set to 1s.
** These bits are defined in Bellcore document TR–NWT000397 Issue 3. When set to "0", the LT indicates to the NT that the network will deactivate the loop between calls.
[ ] These are bit definitions for the revised ANSI T1.601–1992. In ANSI T1.601–1988 they were set to 1s.

4.4.2 BR1: M4 Receive Data Register

By reading this register, the external microcontroller obtains a buffered copy of the M4 bits that are parsed from the received superframe by the Superframe Deframer. The values in the register are valid when Superframe Sync (NR1(b1)) is 1. See Register BR9(b5:b4) for a description of when the "read" information is updated, and when to write to this register. This register is double buffered. The receive M4 channel byte can be read at any time during the superframe prior to the next update. It is recommended that the MPU read this register as soon as possible after an interrupt. Note that BR14(b6) has no effect on the operation of this register. Bit 0 in overlay register OR7 selects trinal checking on M4 act, dea, uoa, sai bits when set to 1. If trinal checking is desired for all bits, then it must be done in software. This register is replaced by Register OR1 when BR10(b0) = 1. When OR7(b0) is set, the M4 act, dea, uoa, sai bits must be the same for three superframes before they are updated in this register.

	b7	b6	b5	b4	b3	b2	b1	b0
BR1	M40 ro/wo	M41 ro/wo	M42 ro/wo	M43 ro/wo	M44 ro/wo	M45 ro/wo	M46 ro/wo	M47 ro/wo

4.4.3 BR2: M5/M6 Transmit Data Register

This register contains the reserved M5 and M6 bits that are sent by the Superframe Framer. The bits written to the register are sent out on the next transmit Superframe boundary if Superframe Update Disable, (NR2(b1)) is set to 0. All bits are set to 1s following a hardware (RESET) or Software Reset (NR0(b3)). See BR9(b1) for details concerning use of the `febe` Input, b4. Bits b7, b6, and b5 are double buffered. When BR10(b0) = 1 this register is replaced by Register OR2.

CAUTION

Reserved bits b0, b1, b2, and b3 should be set to 0 at all times to maintain future compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
BR2	M50 rw	M60 rw	M51 rw	`febe` Input rw	Reserved rw	Reserved rw	Reserved rw	Reserved rw

ANSI T1.601–1992 presently reserves bits M50, M60, and M51. Therefore, these bits should be set to 1s for ISDN applications.

`febe` Input

The value in this bit is enabled to be transmitted as the `febe` when BR9(b1) is set to 1.

4.4.4 BR3: M5/M6 Receive Data Register

This register contains the ANSI T1.601–1992 reserved M5 and M6 bits that are received by the Superframe Deframer, occurring in basic frames 1 and 2 of the superframe, and four other Superframe Deframer status bits. The M5 and M6 values in the register are valid when the Superframe Sync bit, NR1(b1), is 1. M50, M51, and M60 are updated based on the mode set in Register BR9(b3:b2). Bits b7, b6, b5 are double buffered. They can be read at any time during the superframe prior to the next update. It is recommended that this register be read as soon as possible after an M5/M6 channel interrupt. Refer to the description of BR9(b3:b2) for details concerning the operation of these three bits. When BR10(b0) = 1 this register is replaced by Register OR3.

	b7	b6	b5	b4	b3	b2	b1	b0
BR3	M50 ro/wo	M60 ro/wo	M51 ro/wo	Received `febe` ro	Computed `febe` ro	Verified `act` ro	Verified `dea` ro	Super-frame Detect ro

Received `febe`

This is the state of the received `febe` bit in the last complete received superframe. It is updated at the end of each received superframe when Superframe Sync (NR1(b1)) and Linkup (NR1(b3)) are both 1s.

Computed nebe

This is the state of the `crc` check from the last complete received superframe. It is updated at the end of each received superframe. This bit is 0 when a `crc` error is detected. Also, when either Superframe Sync (NR1(b1)) or Linkup (NR1(b3)) is 0 this Computed `nebe` bit is forced to 0.

Verified `act`

This is the dual–consecutively checked setting of the `act` bit in the received superframe. Dual–consecutive checking requires that the received bit be in the same state for two consecutive superframes. Whenever the U–interface transceiver detects a transition from 0 to 1 on Superframe Sync, NR1(b1), Verified `act` is set to 0. It remains in its current state until both Superframe Sync (NR1(b1)) and Linkup (NR1(b3)) are 1s. Then, if the received `act` bit is 1 for two consecutive superframes, Verified `act` becomes a 1. After Verified `act` becomes a 1, it changes to 0 if the received `act` bit is received as a 0 for two consecutive superframes. This bit is updated at the end of the first frame of each superframe and is provided in this register for status only. See BR9(b5:b4) for more information regarding this bit. When OR7(b0) is set, the M4 `act` and `dea` bits must be valid for three superframes before verified `act` or verified `dea` are updated.

Verified dea

This is the dual–consecutively checked, inverted setting of the dea bit, in the received superframe. Since the dea bit can only be received by an NT, this bit can only be 1 in the LT mode. Dual–consecutive checking requires that the received bit is in the same state for two consecutive superframes. Whenever the U–interface transceiver detects a transition from '0' to '1' on Superframe Sync in NR1(b1), Verified dea is set to 0. It remains in its current state until both Superframe Sync (NR1(b1)) and Linkup (NR1(b3)) are 1s. Then, if the received dea bit is 0 for two consecutive superframes, Verified dea will become 1. After Verified dea becomes 1, if the received dea bit is ever 1 for two consecutive superframes, then Verified dea will become a 0. This bit is updated at the end of the second basic frame of each superframe and is provided in this register for status only. See BR9(b5:b4) for more information regarding this bit. When OR7(b0) is set, the M4 dea bit must be valid for three superframes before verified dea is updated.

Superframe Detect

This is the unmodified output of the Superframe Deframer's superframe detection circuit. It is primarily intended for diagnostic purposes.

4.4.5 BR4: febe Counter

This register contains the current febe count. The counter is not cleared by a software or hardware reset. The register can be preset to any value by writing to it. If the febe bit is active in a superframe, the counter will increment at the end of the received superframe. The counter will not increment unless Superframe Sync (NR1(b1)) and Linkup (NR1(b3)) are both 1s. If OR7(b1) is set, then the febe counter will roll over from $FF to $00. The user software must take into account that if OR7(b1) is set, the counter value read from BR4 might be less than the previous value, which means that the counter has rolled over. The default setting for OR7(b1) after any hardware or software reset produces the same operation as the MC145472/MC14LC5472. This register is replaced by Register OR4 when BR10(b0) = 1. When OR7(b1) is cleared BR4 counts to $FF and does not roll over. This is the default configuration after any reset to maintain MC145472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
BR4	febe Counter 7 rw	febe Counter 6 rw	febe Counter 5 rw	febe Counter 4 rw	febe Counter 3 rw	febe Counter 2 rw	febe Counter 1 rw	febe Counter 0 rw

4.4.6 BR5: nebe Counter

This register contains the current nebe count. A nebe occurs whenever the received crc message does not match the computed crc or when Linkup (NR1(b3)) is 1 and Superframe Sync (NR1(b1)) is 0. The Superframe Framer maintains the Superframe timing to increment the nebe counter when Superframe Sync is 0. The counter is not cleared by a software or hardware reset. The register can be preset to any value by writing to it.

When the Superframe Deframer detects a crc error in the received superframe, the counter is incremented at the end of that superframe. When OR7(b1) is set, then the febe counter rolls over from $FF to $00. The user software must take into account that if OR7(b1) is set, the counter value read from BR5 might be less than the previous value, which means that the counter has rolled over. The default setting for OR7(b1) after any hardware or software reset produces the same operation as the MC145472/MC14LC5472. When BR10(b0) = 1 this register is replaced by Register OR5. When OR7(b1) is cleared BR5 counts to $FF and does not roll over. This is the default configuration after any reset to maintain MC145472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
BR5	nebe Counter 7 rw	nebe Counter 6 rw	nebe Counter 5 rw	nebe Counter 4 rw	nebe Counter 3 rw	nebe Counter 2 rw	nebe Counter 1 rw	nebe Counter 0 rw

4.4.7 BR6: Loopback Control Register

This register contains the loopback controls. For normal (no loopback) operation, bits b7:b5 and b3:b1 of BR6 should be 0. BR6 is cleared by a Software Reset (NR0(b3)), Hardware Reset (RESET), or when the Return to Normal bit (NR0(b0)) is set. When a bit is set to 1, the appropriate loopback is enabled. This register is replaced by Register OR6 when BR10(b0) = 1.
Bits b7 through b4, inclusive, are not set when the MC145572 is operating in the automatic eoc mode.

	b7	b6	b5	b4	b3	b2	b1	b0
BR6	U–Loop B1 rw	U–Loop B2 rw	U–Loop 2B + D rw	U–Loop Trans–parent rw	IDL–Loop B1 rw	IDL–Loop B2 rw	IDL–Loop 2B + D rw	IDL–Loop Trans–parent rw

U–Loop B1

This bit selects a loopback on the B1 channel toward the U–interface.

U–Loop B2

This bit selects a loopback on the B2 channel toward the U–interface.

U–Loop 2B + D

This bit selects a loopback on the B1, B2, and D channels toward the U–interface.

U–Loop Transparent

This bit selects whether the loopback toward the U–interface should be handled transparently or not. This transparency selection applies to all channels that are selected for loopback to the U–interface.

IDL2–Loop B1

This bit selects a loopback on the B1 channel toward the IDL2 interface. This bit operates in all IDL2 and GCI modes.

IDL2–Loop B2

This bit selects a loopback on the B2 channel toward the IDL2 interface. This bit operates in all IDL2 and GCI modes.

IDL2–Loop 2B+D

This bit selects a loopback on the B1, B2, and D channels toward the IDL2 interface. When this bit is set to 1, the IDL2–loop B1 and IDL2–loop B2 bits are ignored. This bit operates in all IDL2 and GCI modes.

IDL2–Loop Transparent

This bit selects whether the loopback toward the IDL2 interface should be handled transparently or not. This transparency selection applies to all channels that are selected for loopback to the IDL2 interface.

Figures 4–1 and 4–2 may be used to determine the combined effect of setting more than one loopback control in BR6, as well as the bits in NR5 and BR7. Only details for the B1 channel are shown, but a similar set of logic applies to both the B2 and D channels. D_{out} and D_{in} refer to the two external pins on the device. There are two control signals shown in Figure 4–2 that do not come from MC145572 registers. LINK ACTIVE is an internal signal that is asserted when the ANSI T1.601–1992 defined activation sequence reaches SN3/SL3 and Customer Enable (NR2(b0)) is set, or Verified `act` (BR3(b2)) is set. LINK GOOD is asserted whenever the ANSI T1.601–1992 defined activation sequence is completed successfully and the internally monitored receive error rate is adequate for passing data.

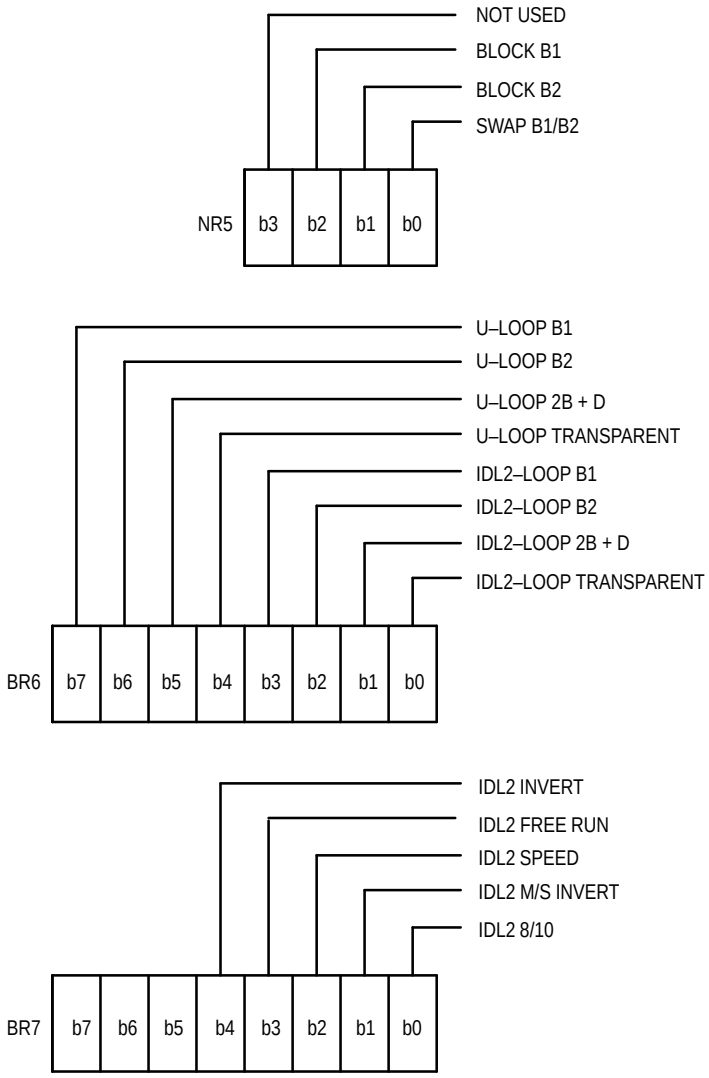

Figure 4–1. IDL2 Interface Loopback Control Bits

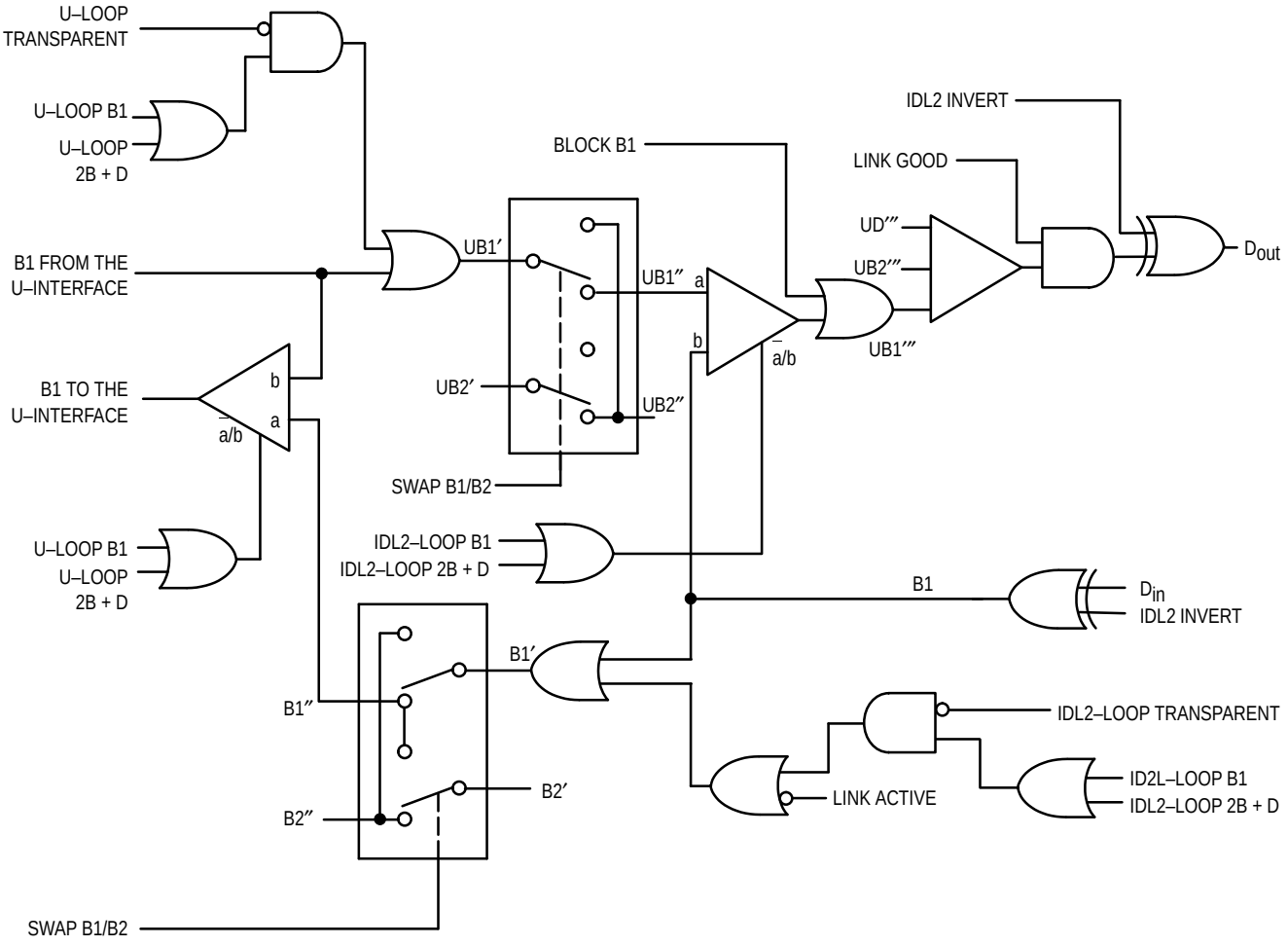

Figure 4–2. IDL2 Interface Loopback Logic Diagram

4.4.8 BR7: IDL2 Configuration Register

This register contains IDL2 interface mode information. BR7 is cleared on Hardware Reset ($\overline{\text{RESET}}$) or Software Reset (NR0(b3)). All bits in this register are read/write. This register is replaced by Register OR7 when BR10(b0) = 1.

	b7	b6	b5	b4	b3	b2	b1	b0
BR7	BR15A Select	OUT2	OUT1	IDL2 Invert	IDL2 Free Run	IDL2 Speed	IDL2 M/S Invert	IDL2 8/10
		wo	wo					
		GCI IN2	GCI IN1					
	rw	ro	ro	rw	rw	rw	rw	rw

BR15A Select

When set to 1, this bit causes register BR15A to be substituted for register BR15 in the SCP register map. After any reset, this bit is cleared to 0.

GCI IN2/OUT2

This is a read–only/write–only bit. The write–only portion, OUT2, is cleared by hardware and software resets. In full GCI mode, entered by holding the pin MCU/GCI low, the state of OUT2 is driven onto a GCI mode dedicated output pin. However, if the GCI C/I channel decodes the input command DISS to the MC145572, this same pin is forced high. When read, (again, provided the MC145572 is in full GCI mode), the bit IN2 reflects the state of a GCI mode dedicated input pin. These pins may be used for any purpose in a GCI application. See Section 3, ***Device Description***, for more information. GCI command LTD2 when active in LT mode or NTD2 when active in NT mode sets OUT2 high.

GCI IN1/OUT1

This is a read–only/write–only bit. The write–only portion, OUT1, is cleared by hardware and software resets. In full GCI mode, entered by holding the pin MCU/GCI low, the state of OUT1 is driven onto a GCI mode, dedicated output pin. When read (again, provided the MC145572 is in full GCI mode), the bit IN1 reflects the state of a GCI mode, dedicated input pin. These pins may be used for any purpose in a GCI application. See Section 3, ***Device Description***, for more information. GCI command LTD1 when active in LT mode or NTD1 when active in NT mode sets OUT1 high.

IDL2 Invert

When set to 1, this bit forces the IDL2 interface to invert every bit just before it is transmitted on the D_{out} pin and invert every bit that is received on D_{in}.

IDL2 Free Run

When set to 0, this bit forces the DCL and FSR and FSX outputs to run continuously when in the IDL2 Master mode. When this bit is 1, the DCL and FSR and FSX stop when the U–interface transceiver is deactivated. DCL and FSR/FSX will start operating when Superframe Sync in NR1(b1) becomes 1 and halts when the U–interface transceiver enters the ANSI T1.601 defined “Tear Down” state.

IDL2 Speed

This bit selects the DCL clock speed in the IDL2 Master mode. When this bit is 0, the clock rate is 2.56 MHz. A 1 selects a rate of 2.048 MHz. This bit also sets the output clock rate for FREQREF or $FREF_{out}$ when in NT slave mode. Also, see the description for OR7(b4).

IDL2 M/S Invert

When this bit is 1, it inverts the polarity of the IDL2 Master/Slave pin. When this bit is 0 and IDL2 Master is set high, the U–interface transceiver operates in the IDL2 Master mode.

IDL2 8/10

This bit reorders the sequence of 2B+D data presented in the IDL2 data transfer. The two possible transfer sequences are shown in Figures 4–3 and 4–4. A ‘1’ selects the 8–bit mode and a ‘0’ selects the 10–bit mode. In the 8–bit mode, the two B channels are provided sequentially, followed by the two D channel bits. In the 10–bit mode one D channel bit follows each B channel byte. The ability to swap the B channels (NR5(b0)) applies to both of these modes. For further information about the IDL2 interface see **Section 5.4**.

NOTE

If timeslot assignment mode is enabled via OR6 b(7), b(6), or b(5), then the IDL2 8/10 control bit is ignored and B channel and D channel data is placed according to OR0–OR5.

If GCI electrical mode is selected by setting OR6(b3) to a 1 the IDL2 interface transfers only 2B+D data in the GCI timeslot locations as programmed in OR5(b2:b0).

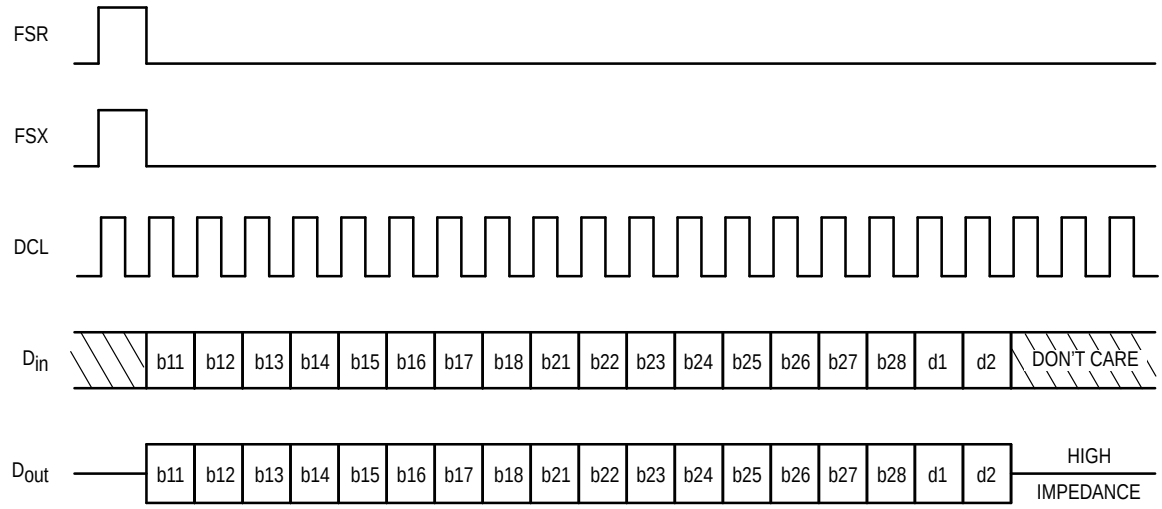

Figure 4–3. IDL2 Interface Timing in 8–Bit Master Mode

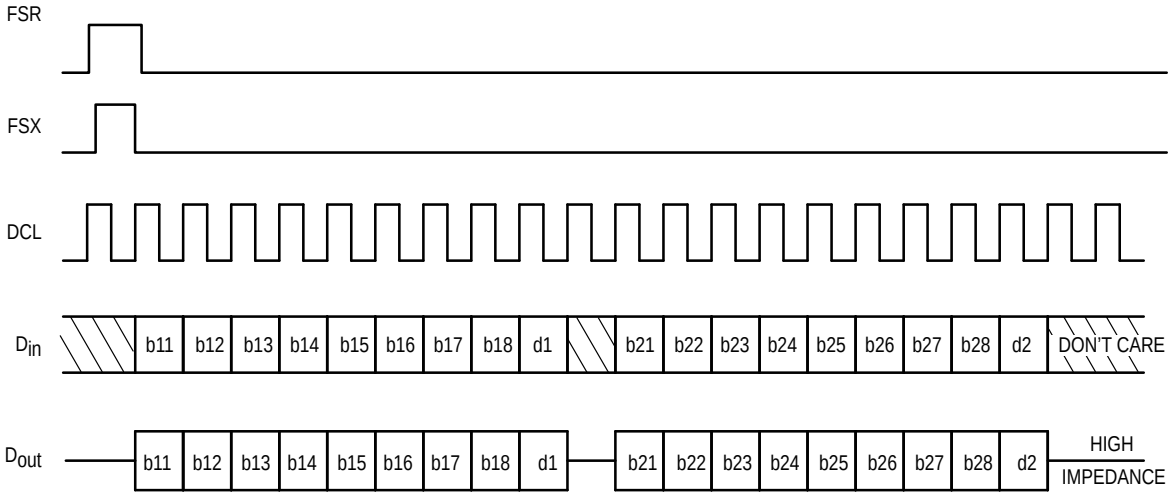

Figure 4–4. IDL2 Interface Timing in 10–Bit Master Mode

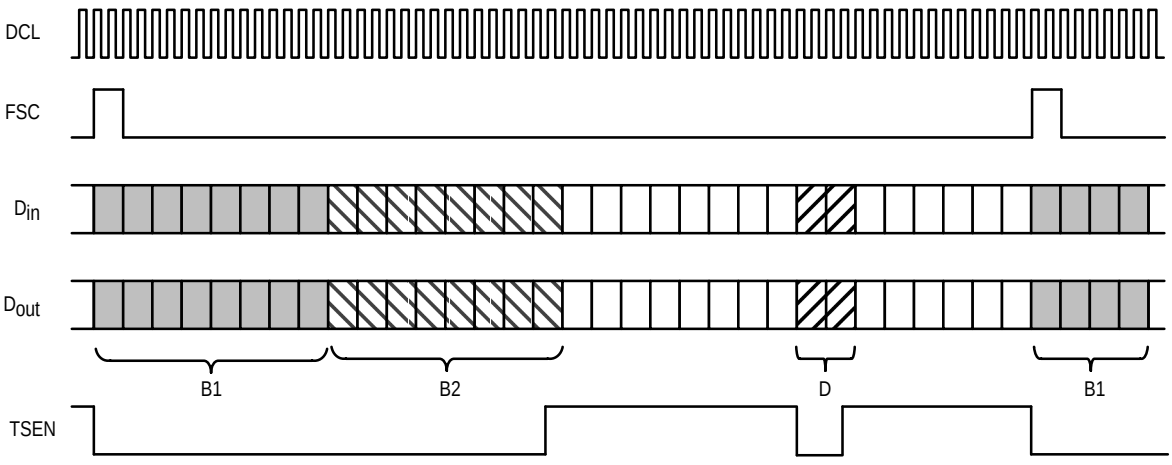

Figure 4–5. IDL2 Interface Timing in GCI 2B+D Mode

4.4.9 BR8: Transmit Framer and Mode Control Register

This register contains controls used for test operations such as external loopbacks, Superframe Framer Control, and State information, and NT/LT mode control. All write capable bits are cleared on a Software Reset (NR0(b3)) or Hardware Reset (RESET). Bits b7–b4 and b0, are read only/write only. To read the write only bits, it is necessary to set BR14(b6) to 1. When BR10(b0) = 1 this register is replaced by Register OR8.

	b7	b6	b5	b4	b3	b2	b1	b0
BR8	Frame Steering wo	Frame Control 2 wo	Frame Control 1 wo	Frame Control 0 wo	crc Corrupt rw	Match Scrambler rw	Receive Window Disable rw	NT/LT Invert wo
	Frame State 3 ro	Frame State 2 ro	Frame State 1 ro	Frame State 0 ro	Reserved	Reserved	Reserved	NT/LT Mode ro

Frame Steering

When this bit is a 1, the Frame Control 2:0 bits take over control of the Superframe Framer's mode of operation.

Frame Control 2:0

These bits set the mode of operation for the Superframe Framer when the Frame Steering bit is 1. Table 4–8 shows the mode the Superframe Framer will go into based on the three Frame Control bits and the Frame Steering bit.

Table 4–8. Frame Control Modes

Frame Steering	Frame Control 2:0			Superframe Framer Mode of Operation	
b7	**b6**	**b5**	**b4**	**NT**	**LT**
1	0	0	0	SN0	SL0
1	0	0	1	Six frames of 10 kHz tone followed by SN1	SL1
1	0	1	0	SN2	SL2
1	0	1	1	SN3	SL3
1	1	0	0	10 kHz tone	
1	1	0	1	40 kHz tone	
1	1	1	0	Generates a single quat every basic frame which alternates over all four of the 2B1Q symbols.	
1	1	1	1	Superframe Framer free runs the scrambler with no synchronization words.	
0	Don't Care			The Superframe Framer output is determined by the state of the Automatic Activation Controller.	

Frame State 3:0

These bits provide the external microcontroller with the current state of the U–interface transceiver's Superframe Framer, regardless of whether the Superframe Framer is being controlled by the external microcontroller or internally by the Automatic Activation Controller. The meaning of Frame State 2:0 maps directly onto the meaning of Frame Control 2:0. Frame State 3 is 0 at all times, except during TN of an NT activation sequence. State transitions are always made on frame or superframe boundaries.

crc Corrupt

When set to 1, this bit forces the transmitted crc to be inverted. It is used for eoc maintenance procedures and to force an outgoing corrupt crc in digital loop carrier systems. As the transmit framer

transmits the crc and this bit is set, the transmitted crc is inverted. This bit can be cleared or set at any time during transmission of a superframe. This bit functions the same as in the MC145472/ MC14LC5472 after a Hardware Reset (RESET). When OR7(b2) is set to 1 the operation of this bit is modified so that the outgoing crc is only corrupted on the current superframe.

Match Scrambler
When set to 1, this bit forces the descrambler and scrambler polynomials to match. This is used for external analog loopback and framer to deframer loopback.

Receive Window Disable
When set to 1, this bit disables the search window placed around the received synchronization word in the LT mode. When the receive window is disabled, the LT will synchronize to an incoming synchronization word that is located at any arbitrary point with respect to its transmitted synchronization word. This allows the U–interface transceiver to use its own transmitted synchronization word for frame detection when operated in external analog loopback mode, and framer to deframer loopback.

NT/$\overline{\text{LT}}$ Invert
This bit allows override control of the setting of the NT or LT operation of the U–interface transceiver's external NT/LT mode pin. If this bit is 0 and the NT/LT pin is high, the device is in NT mode. When this bit is then set to 1, the device will then be in the LT mode.

NT/$\overline{\text{LT}}$ Mode
This read only bit reflects the current mode of the device. If 1, the U–interface transceiver is operating in the NT mode.

4.4.10 BR9: Maintenance Channel Configuration Register

This register contains mode control over the deframer's updating of the received maintenance bits. The register is cleared on Software Reset (NR0(b3)) or Hardware Reset (RESET). When BR10(b0) = 1 this register is replaced by Register OR9.

CAUTION

Reserved bit b0 should be set to 0 at all times to maintain future compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
BR9	eoc Control 1 rw	eoc Control 0 rw	M4 Control 1 rw	M4 Control 0 rw	M5/M6 Control 1 rw	M5/M6 Control 0 rw	febe/ nebe Control rw	Reserved

eoc Control 1:0
These bits control the eoc handling capability of the U–interface transceiver. Table 4–9 gives a brief description of each mode selected by the eoc Control bits. The eoc Trinal–Check mode (b7,b6 = 1,0) and the Automatic eoc Processor mode (b7,b6 = 0, "Don't Care") are described in the paragraphs following Table 4–9. The default mode setting is 0,0, thereby selecting the Automatic eoc Processor. Regardless of the operating mode, every time R6 is loaded by the deframer, IRQ2 (NR3(b2)) is set to 1. Use the update on every frame mode (b7,b6 = 1,1) for digital loop carrier or proprietary applications.

Table 4–9. eoc Control Modes

eoc Control 1:0		eoc Function Description
b7	b6	
1	1	Update eoc register (R6) on every eoc frame (twice during each superframe). Recommended for Digital Loop Carrier applications.
1	0	Update eoc register (R6) after passing a trinal–check.
0	Don't Care	Update eoc register (R6) after passing a trinal–check and also invoke Automatic eoc Processor to operate when in NT mode.

eoc Trinal–Check Mode (b7, b6 = 1,0)

The eoc trinal–check operation checks for three identical consecutive eoc messages being received before loading the eoc message into R6. Register R6 is always updated with the received message when the third identical consecutive message is received.

In trinal–check mode when operating as an LT, the trinal check is automatically restarted whenever a new message is written to the Superframe Framer's R6 register for transmission. The eoc trinal–check is reset whenever the Linkup (NR1(b3)) or Superframe Sync (NR1(b1)) bits are 0.

When operating as an NT in trinal–check mode, received eoc messages are automatically transmitted back by the Superframe Framer if the address is either the NT1 or broadcast address. This continues until three valid consecutive identical messages have been received. If the eoc address in the received eoc message is not 0 or 7, the HOLD message is substituted and automatically transmitted back to the LT. Once three valid consecutive identical messages have been received, the deframer updates Register R6. Once R6 has been updated with the received message, the Superframe Framer's Register R6 (written to by an SCP Interface operation) is transmitted. It is up to the microcontroller firmware to handle the eoc message and place a response into R6 before the U–chip sends the next eoc frame out to the LT (see Figure 4–2). Register R6 will be repeated throughout all subsequent eoc frames until it is altered by another CPI Interface write to it or the received eoc message changes.

Automatic eoc Processor Mode (b7 = 0, b6 = Don't care)

An Automatic eoc Processor is provided in the NT mode. This processor operates the eoc in accordance with ANSI T1.601–1992. The processor recognizes eoc messages addressed to either the NT1 or the broadcast address. The processor decodes the messages in Table 4–10 and then takes the action indicated. If a properly addressed message is received that is not listed in the table, the "Unable to Comply" message is transmitted in response. If an improperly addressed message is received, the "Hold State" message is transmitted with the NT1 address. Whenever operating in this mode, the eoc trinal–check operation continues to function and R6 will be loaded with the eoc message that the Automatic eoc Processor decodes. Note that because the Automatic eoc Processor is an NT mode only function, selecting Mode 0,0 in the LT mode is equivalent to mode 1,0.

Regardless of eoc mode, Register R6 will not be altered while Superframe Detect (BR3(b0)) is a 0. When the automatic eoc mode is enabled, bits in BR6 are not set when loopback messages are received.

Table 4–10. Automatic eoc Processor Functions

eoc Message	Automatic eoc Processor Response
Operate 2B + D Loopback	Invokes a loopback to the U–interface at the IDL Interface of the B1, B2, and D channels. Transparency will be determined by the setting of BR6(b4), U–loop transparent.
Operate B1 Channel Loopback	Invokes a loopback to the U–interface at the IDL Interface of the B1 channel. The loopback is transparent.
Operate B2 Channel Loopback	Invokes a loopback to the U–interface at the IDL Interface of the B2 channel. The loopback is transparent.
Request Corrupted `crc`	Equivalent to setting BR8(b3) to a 1.
Notify of Corrupted `crc`	None.
Return to Normal	Resets all of the previously invoked eoc functions.
Hold State	Maintains previously invoked eoc functions.

M4 Control 1:0

These bits control the M4 handling capability of the U–interface transceiver. The default mode setting is b5, b4 = 0,0. In all of the modes, BR1 will not be loaded and an IRQ1 (NR3(b1)) will not be issued unless both Linkup (NR1(b3)) and Superframe Sync (NR1(b1)) are 1s. When OR7(b0) is set to 1 `uoa`, `act`, `sai`, `dea` bits in the M4 channel are trinal checked.

Table 4–11. M4 Control Modes

OR7	BR9 M4 Control 1:0		M4 Function Description
	b5	b4	
0	0	0	M4 Dual Consecutive mode. In addition, the Verified act (BR3(b2)) and Verified dea (BR3(b1)) operations are enabled in this mode only.
0	0	1	M4 Dual Consecutive mode.
0	1	0	Delta mode.
0	1	1	Every mode.
1	X	X	M4 Channel bits M40 (act), M41 (dea), M46 (uoa, sai) are trinal checked. Remaining bits operate per BR9(b5,b4) settings. Verified act and Verified dea available on trinal checked act, dea bits when b5:b4 = 0,0.

M4 Dual Consecutive Modes (b5, b4 = 0,0 or 0,1)

The M4 Dual Consecutive modes perform a simple algorithm on the received M4 bits, and only interrupt the external microcontroller when an M4 bit has changed state and has remained in the new state for two consecutive superframes. The M4 bit values read from BR1 in this mode are only the most recent values that have been the same for two consecutive superframes. Referring to Table 4–12, suppose, for example, that for several superframes the M4 bits have been all 0s, as shown in the column labeled Received M4 Byte. If the external microcontroller read BR1, it would read all 0s as shown in the column labeled BR1 Contents. Now, notice in the subsequent superframes 2 and 3 that the received M4 bits that do not hold their state for at least two consecutive superframes do not cause an interrupt and do not show up in BR1.

Table 4–12. M4 Dual Consecutive Modes Example

Superframe	Received M4 Byte	BR1 Contents	Action
1	0000 0000	0000 0000	
2	1000 0001	0000 0000	
3	0001 0001	0000 0001	IRQ1 is set

At start–up, there is no history of what has been received in the M4 bits. Therefore, the technique for the initial setting for BR1 is as follows: a hardware or software reset sets BR1 to all 0s. However, at the user's discretion, while either Linkup (NR1(b3)) or Superframe Sync (NR1(b1)) is 0, the user may write to BR1 and set the initial value. In this way, the external microcontroller may assume a current state for the M4 bits, and then wait for an IRQ1 to inform it of a change in state. Also, any time that Superframe Sync is lost and then regained, the initial programmed value is reloaded into BR1.

The default M4 Dual Consecutive Mode (b5, b4 = 0,0) has the additional feature of performing automatic detection of the act and dea bits. Verified act (BR3(b2)) and Verified dea ((BR3(b1)) are dual consecutive checked values of M40 and M41. Verified act is valid for both NT and LT modes. Verified dea operates in the NT mode only. Whenever there is a 0 to 1 transition on Superframe Sync (NR1(b1)), Verified act and Verified dea are reset. If M40 is received as 1 for two consecutive superframes, Verified act is set to 1. Similarly, if M40 is received as 0 for two consecutive superframes, Verified act is set to 0. When this mode is selected, the logical OR of Verified act and the Customer Enable bit in NR2(b0) permits customer data transparency without any action taken by the external microcontroller. In the NT mode, if M41 is received for two consecutive superframes as 0, Verified dea is set to 1. Similarly, if M41 is received as 1 for two consecutive superframes, Verified dea will return to 0. When this mode is selected, the logical OR of Verified dea and the Deactivate Request bit in NR2(b2) allows the U–interface transceiver to respond to the far end transceiver's intention to deactivate without requiring any interaction by the external microcontroller. Note that the state of Verified act and Verified dea may be monitored by the external microcontroller through BR3(b2:b1).

M4 Delta Mode (b5, b4 = 1,0)

The Delta Mode compares the M4 data from the previous superframe against the current received superframe M4 data. If there is a difference in at least one bit, BR1 is updated and an IRQ1 interrupt is issued. Note that in this mode BR1 always contains a copy of the latest received M4 byte from the previous superframe.

M4 Every Mode (b5, b4 = 1,1)

The Every Mode stores each received superframe of M4 data in BR1 and issues an interrupt at the end of every received superframe.

Note that regardless of mode of operation, BR1 will not be altered while Superframe Sync (NR1(b1)) is 0.

M4 Trinal Check Mode

The M4 act, dea, sai, and uoa bits can be configured for trinal check operation by setting OR7(b0) to a 1. **See Section 4.5.8** for more detail.

M5/M6 Control 1:0

These bits control the M5/M6 handling capability of the U–interface transceiver. The default mode setting is b3, b2 = 0,0, which selects the Dual Consecutive mode. These controls are identical in operation to the M4 Mode Control functions, except that they apply to M50, M51, and M60. Refer to the M4 Control Mode paragraphs above for a description of the M5/M6 Control Modes. The M5/M6 interrupt, IRQ0 (NR3(b0)), occurs in the middle of the superframe when basic frame 4 has been completely received.

Table 4–13. M5/M6 Control Modes

M5/M6 Control 1:0		M5/M6 Function Description
b3	b2	
0	Don't Care	M5/M6 Dual Consecutive Mode
1	0	Delta Mode
1	1	Every Mode

febe/nebe Control

This bit controls how the transmitted febe is computed. If this bit is 0, the transmitted febe is set active if either the Computed nebe (BR3(b3)) is active or the febe Input (BR2(b4)) is set active. If this control bit is set to 1, the transmitted febe is set to whatever is set in the febe Input (BR2(b4)).

NOTE

Regarding febe and nebe, "active" means they are set to 0.

4.4.11 BR10: Overlay Select Register

This register is used to enable access to the overlay register set of the MC145572. To maintain future compatibility the reserved bits must be written as 0's.

	b7	b6	b5	b4	b3	b2	b1	b0
BR10	Reserved	Reserved	Reserved	Reserved	Reserved	Select Dump Access rw	Select DCH Access rw	Select Overlay rw

Select Dump Access

This bit hides the normal byte register BR13, and the register becomes a byte–wide access port, OR13, to the Dump/Restore mechanism of the U–chip. Two more bits in the overlay registers control the operating mode of the Dump/Restore mechanism. See Overlay Registers overlay register OR8. This bit is reset by both hardware and software resets.

Select DCH Access

This bit hides the normal byte register BR12, and the register becomes an 8 bit read–only/write–only register, OR12, and provides access to the D channel. When this bit is asserted, D channel input data present on the pin interfaces of the MC145572 is ignored and D_{out} is high–impedance. Instead, the D channel is sourced strictly from this register. D channel data received from the U–interface maintains correct byte alignment relative to the U–interface basic frame boundary on the pin interfaces, and is readable through the overlay register OR12 eight bits at a time. IRQ3 is used to indicate when every new 8 bits of data are received in addition to indicating a change in receive status.

A special code (1111) is loaded in nibble register NR1, to indicate that the source of the interrupt is the D channel access register. Both transmit and receive of the D channel data is aligned respective to the transmit and receive superframes. When selected, the D channel access register has the highest priority over other possible routes, (e.g., the IDL2 interface and the D channel port), for the D channel data. This bit is reset by both hardware and software resets. Software should read and write this register at the time the D channel interrupt occurs.

Enabling OR12 access enables the D channel interrupt onto IRQ3. The interrupt must still be enabled via IRQ3 Enable in NR4 for the IRQ pin to become active. Upon receipt of the interrupt, the external controller must read the interrupt status in NR3 to determine that it is an IRQ3. The controller must then read NR1, where it would find the code 1111, indicating the actual source is a D channel interrupt.

NOTE

If DCH Access mode is used in conjunction with timeslot assignment, the D channel timeslot must not be timeslot 0 in order to maintain synchronization with the transmit superframe. This is especially true in LT mode when SFAX is used as an input.

Select Overlay

This bit hides the normal byte registers BR0–BR9, and the registers become the overlay registers OR0–OR9. In general, the overlay registers contain device information that needs to be set only once following reset such as the timeslot information, or during some test mode. This bit is reset by both hardware and software resets.

4.4.12 BR11: Activation State Register

This register contains activation state and control data. All the bits are cleared on Hardware Reset (RESET) and Software Reset (NR0(b3)). The register is a read only/write only register. Setting BR14(b6) to 1 permits the external microcontroller to read back the write portion of the register.

	b7	b6	b5	b4	b3	b2	b1	b0
BR11	Activation Control 6 wo	Activation Control 5 wo	Activation Control 4 wo	Activation Control 3 wo	Activation Control 2 wo	Activation Control 1 wo	Activation Control 0 wo	Activation Timer Disable wo
	Activation State 6 ro	Activation State 5 ro	Activation State 4 ro	Activation State 3 ro	Activation State 2 ro	Activation State 1 ro	Activation State 0 ro	Activation Timer Expire ro

Activation Control 6:0

These write only bits allow the external microcontroller to set a new activation state for the U–interface transceiver to execute. The transition to this state is controlled by BR12. Use of this register is not required for normal operation.

Activation Timer Disable

When this write only bit is ‘0’, the activation timer operates normally. During activation the timer will time for approximately 15 seconds, and then the Activation Timer Expire bit will become 1, and the activation state machine will react to the time–out. When this bit is set to 1, the activation timer is disabled and the Activation Timer Expire will always read back as 0.

Activation State 6:0

These read only bits contain the current state of the internal activation controller. Activation State 6, BR11(b7) indicates cold start mode when it is 0 and indicates warm start mode when it is 1.

Activation Timer Expire

This bit shows the status of the activation timer. A 1 indicates that the activation timer has expired.

4.4.13 BR12: Activation State Test Register

This register is read only/write only. The write only portion controls the U–interface transceiver’s internal central processing unit (CPU) and activation controller. The read portion contains the eight most significant bits of the Error Power Indicator (EPI) register in the CPU. By setting BR14(b6) to 1, the external microcontroller can read back the setting of the control bits. These bits are cleared on a Hardware Reset (RESET) or Software Reset (NR0(b3)). This register is replaced by OR12 when BR10(b1) = 1.

CAUTION

Reserved bit b1 should be set to 0 at all times to maintain future compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
BR12	Activation Control Register wo	Interpolate Enable wo	Load Activation State wo	Step Activation State wo	Hold Activation State wo	Big Jump Select wo	Reserved wo	Force Linkup wo
	EPI 18 ro	EPI 17 ro	EPI 16 ro	EPI 15 ro	EPI 14 ro	EPI 13 ro	EPI 12 ro	EPI 11 ro

Activation Control Steer

When this bit is 0, the internal CPU of the MC145572 has total control of its peripherals, and has them perform a normal activation procedure. However, when this bit is set to 1, the internal CPU and its peripherals are directed to use the control information provided in the Interpolate Enable bit in this register (b6), BR13, BR15A(b7), and BR15A(b6).

Interpolate Enable

This bit is active only when the Activation Control Steer bit (b7) is set to 1. The timing interpolator is enabled when this bit is 1 and the transceiver is operating in LT mode. The timing interpolator is disabled when this bit is 0 and the transceiver is operating in LT mode.

Load Activation State

When this bit is set to 1, Activation Control 6:0 is loaded into the activation controller as the new state. The load is performed at a time that does not adversely affect the operation of the CPU, and will take place within one baud of setting this bit to 1. To load an activation state, this bit must initially be 0. The desired state should then be loaded into BR11 and this bit should be set to 1. Loading overrides the setting of the Hold Activation State bit (b3).

Step Activation State

When this bit is set to 1, the activation controller advances to its next state based on its current inputs. The step is performed at a time that does not adversely affect the operation of the CPU. This bit must be returned to 0 following the step to prepare for subsequent steps. Stepping overrides the Hold Activation State bit (b3). Note that the step will not occur unless the CPU has determined that a condition for continuing to the next activation state has been satisfied.

Hold Activation State

When this bit is set to 1, the activation controller is held in the current state until either a Load Activation State (b5) or a Step Activation State (b4) is performed.

Big Jump Select

When this bit is 1, timing phase jumps will be made in four unit increments. When this bit is 0, timing phase jumps will be made in one unit increments.

Force Linkup

When this bit is set to 1, the internal status is forced to be that of full–duplex operation. Note that the CPU is still operating according to the activation state as read in BR11. However, loopbacks and maintenance operations may be performed at the Superframe Framer/Deframer level with full data transparency.

EPI 18:11

These are the most significant bits of the Error Power Indicator register within the CPU. The EPI register in the CPU takes on different meanings depending on the current activation state. This EPI register is updated once per frame. The EPI 10:3 bits are in register BR13. EPI 2:0 are not available to the external microcontroller.

4.4.14 BR13: Echo Canceller Test Register

This register contains several items that control the internal operation of the U–interface transceiver echo canceller. These bits are cleared on a Hardware Reset (RESET) or Software Reset (NR0(b3)). Note that none of the control bits in this register affect the operation of the chip unless the Activation Control Steer bit in BR12(b7) is set to 1. This register is replaced by OR13 when BR10(b2) = 1.

	b7	b6	b5	b4	b3	b2	b1	b0
BR13	Enable MEC Updates wo	Accumu-late EC Output wo	Enable EC Updates wo	Fast EC Beta wo	Accumu-late DFE Output wo	Enable DFE Updates wo	Fast DFE/ARC Beta wo	Clear All Coeffi-cients wo
	EPI 10 ro	EPI 9 ro	EPI 8 ro	EPI 7 ro	EPI 6 ro	EPI 5 ro	EPI 4 ro	EPI 3 ro

Enable MEC Updates

When set to 0, this bit freezes the current coefficients of the Memory Echo Canceller (MEC).

Accumulate EC Output

When this bit is set to 1, the results of all three echo cancellers (MEC, Transversal Echo Canceller (TEC), and Infinite Impulse Response Echo Canceller (IIREC)) are included in the process of recovering the received symbol.

Enable EC Updates

When set to 0, this bit freezes the current coefficients of the TEC and IIREC echo cancellers.

Fast EC Beta

This bit controls the echo canceller beta constant. A 1 instructs the echo canceller to adapt at its fastest rate.

Accumulate DFE Output

When 0, this bit forces the output from the Decision Feedback Equalizer (DFE) convolution to 0 and the symbol storage elements of the DFE will set to alternating ±1. When this bit is 1, the DFE convolution is included in the process of recovering the received symbol.

Enable DFE Updates

When set to 0, this bit freezes the DFE coefficients and the Adaptive Reference Control (ARC) tap.

Fast DFE/ARC Beta

This bit controls the betas for the DFE and ARC. When set to 1, the DFE and ARC adapt at their highest rate.

Clear All Coefficients

When set to 1, the coefficients in the DFE, ARC, TEC, and MEC are cleared and the elastic buffer is reset. The timing offset between the receive and transmit clocks is not altered by setting this bit.

EPI 10:3

These are the least significant bits of the Error Power Indicator (EPI) register within the CPU. The EPI register in the CPU takes on different meanings depending on the current activation state. This EPI register is updated once per frame. The EPI 18:11 bits are in register BR12. EPI 2:0 are not available to the external microcontroller.

4.4.15 BR14: Test Register

This register is used for setting various diagnostic modes. This register is cleared on a Hardware Reset (RESET) or Software Reset (NR0(b3)). When all of these bits are 0, the register map is in the default mode.

CAUTION

Reserved bits b7, b5, b2, and b1 must be set to 0 at all times.

	b7	b6	b5	b4	b3	b2	b1	b0
BR14	Reserved rw	ro/wo to r/w rw	Reserved rw	Framer to Deframer Loop rw	± 1 Tones rw	Reserved rw	Reserved rw	Enable CLKs rw

ro/wo to r/w

When this bit is set to 1, all of the write only registers, except BR15A, become read/write registers for diagnostic purposes. A bit that is normally read only will not be available when this bit is set to 1. Setting this bit to 1 has no effect on BR15A(b4:b0); they remain write only bits at all times.

Framer to Deframer Loopback

This bit enables the Superframe Framer to Superframe Deframer Loopback mode when it is 1. The transmit drivers are off in this mode.

±1 Tones

When this bit is set to 1, the Superframe Framer generates its tones (10 kHz and 40 kHz) using ±1 quats instead of the default of ±3 quats.

Enable CLKs

When set to 1 this bit enables the SYSCLK, EYE DATA, Rx BCLK, Tx BCLK, and Tx SFS pins. Note that BR15A(b3) must also be set to 1 for the Tx SFS output to be enabled.

NOTE

SYSCLK, EYE DATA, Rx BCLK, Tx BCLK, and Tx SFS pin functionality can be modified by the setting of bits in OR8 and OR9.

4.4.16 BR15: Revision Number Register

This read only register contains the revision number of the particular U–interface transceiver device. BR15 is accessed by a serial control port or parallel control port transfer when BR7(b7) is 0 and the byte address is 15.

	b7	b6	b5	b4	b3	b2	b1	b0
BR15	Mask 7 ro	Mask 6 ro	Mask 5 ro	Mask 4 ro	Mask 3 ro	Mask 2 ro	Mask 1 ro	Mask 0 ro

Mask 7:0

These bits allow for an electronic determination of the revision number of the MC145572 U–interface transceiver manufacturing mask set.

4.4.17 BR15A: Baud Clock and Timing Test Register

This register is used to enable clock and test data outputs. All writable bits in this register are cleared to 0 after a reset. BR15A is accessed by a CPI transfer when BR7(b7) is 1 and the byte address in the SCP transfer is 15. The write only bits in this register remain write only bits when BR14(b6) is set to a 1.

CAUTION

Reserved bits b5 and b4 must be set to 0 at all times.

	b7	b6	b5	b4	b3	b2	b1	b0
BR15A	FREQ ADAPT rw	Jump Disable rw	Reserved rw	Reserved wo Reserved ro	Enable Tx SFS wo Reserved ro	Reserved wo Reserved ro	Reserved wo Reserved ro	Enable Eye Data and Baud Clock wo Reserved ro

FREQ ADAPT

This bit is a r/w bit. There is no effect on the operation of the U–interface transceiver unless Control Steer (BR12 (b7)) is set to 1. When Control Steer is 1 and FREQ ADAPT is set to 1, the NT frequency adaptation circuits are enabled to adjust the external crystal frequency. Setting this bit to 0 freezes the frequency adaptation circuits in their current state.

Jump Disable

This bit is a r/w bit. Setting this bit to 1 disables the digital PLL when Activation Control Steer (BR12(b7)) is set to 1 (this bit is used for Motorola test purposes only).

Enable Tx SFS

When set to 1 with BR14(b0) set to 1, this bit enables the transmit superframe sync to be output.

Enable Eye Data and Baud Clock

When set to 1, this bit enables the EYE DATA, SYSCLK, Rx BAUD CLK, and Tx BAUD CLK output pins.

NOTE

When the MC145572 is configured for IDL2 and Serial Control Port operation the 15.36 CLKOUT, 4.096 CLKOUT, and BUF XTAL pins default to “on.” Software written for the MC145472/MC14LC5472 that set BR15A (b1 or b2) is not affected when an existing MC145472 or MC14LC5472 product is upgraded to the MC145572.

4.5 OVERLAY REGISTERS

Table 4–3 shows the registers on the MC145572 that overlay the standard byte registers. The SCP address for the overlay registers is the same as the address for the standard byte register set. The overlay registers are substituted for the standard registers when at least one of BR7(b7), or BR10(b2, b1, b0) is set to 1. BR15A was implemented in the MC145472, but the other registers are new to the MC145572.

BR15A was modified on the MC145572 from the MC145472, to change the 15.36 MHz and 20.48 MHz clock outputs to default to enabled. In order to maintain code–compatibility with the MC145472, the bits were moved from BR15A to the overlay registers. To disable these clocks OR9(b2, b1, b0) can be set to 1s.

Overlay registers OR0 – OR5 are used for defining the timeslot assignment when the IDL2 interface is put into timeslot assigner mode by setting one or more of the bits TSA B1 Enable, TSA B2 Enable, or TSA D Enable, found in overlay register OR6. Timeslots are two DCL clocks in width and are numbered starting from 0.

Overlay register OR5 also is used to define the GCI timeslot when the bit GCI Mode Enable is asserted in overlay register OR6. The remainder of the bits in overlay registers OR6 – OR9 are explained following Table 4–3.

All bits in the overlay registers are reset to 0 on hardware and software resets. The overlay overlay registers are hidden after a hardware or software reset. They can be accessed when BR10(b0) is set to 1.

4.5.1 OR0: D_{out} B1 Timeslot Register

This register controls when the B1 timeslot appears on the D_{out} pin. After a hardware or software reset, all bits default to 0 to maintain MC145472/MC14LC5472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
OR0	D_{out} B1 Channel Timeslot Bits (7:0) rw							

4.5.2 OR1: D_{out} B2 Timeslot Register

Programmed the same way as OR0. This register controls when the B2 timeslot appears on the D_{out} pin. After a hardware or software reset, all bits default to 0 to maintain MC145472/ MC14LC5472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
OR1	D_{out} B2 Channel Timeslot Bits (7:0) rw							

4.5.3 OR2: D_{out} D Timeslot Register

Programmed the same way as OR0. This register controls when the D timeslot appears on the D_{out} pin. After a hardware or software reset, all bits default to 0 to maintain MC145472/ MC14LC5472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
OR2	D_{out} D Channel Timeslot Bits (7:0) rw							

4.5.4 OR3: D_{in} B1 Timeslot Register

Programmed the same way as OR0. This register controls when the B1 timeslot is input from the D_{in} pin. After a hardware or software reset all bits default to 0 to maintain MC145472/ MC14LC5472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
OR3	D_{in} B1 Channel Timeslot Bits (7:0)							
	rw							

4.5.5 OR4: D_{in} B2 Timeslot Register

Programmed the same way as OR0. This register controls when the B2 timeslot is input from the D_{in} pin. After a hardware or software reset all bits default to 0 to maintain MC145472/ MC14LC5472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
OR4	D_{in} B2 Channel Timeslot Bits (7:0)							
	rw							

4.5.6 OR5: D_{in} D and GCI Timeslot Register

Programmed similar to OR2. This register controls when the D timeslot is input from the D_{in} pin. After a hardware or software reset, all bits default to 0 to maintain MC145472/MC14LC5472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
OR5	D_{in} B2 Channel Timeslot Bits (7:0)							
	rw					GCI Slot		
						rw		

GCI Slot (2:0)

In IDL2 mode, if OR6 b(3) is set to indicate GCI 2B+D operation, b(2:0) are used to program the GCI timeslot.

4.5.7 OR6: Timeslot and GCI Control Register

This register is used to enable the timeslot assigner and select GCI 2B+D data format when in IDL2 mode. After a hardware or software reset, all bits default to 0 to maintain MC145472/MC14LC5472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
OR6	TSA B1 Enable	TSA B2 Enable	TSA D Enable	GCI Select M4 – BR0	GCI Mode Enable	Reserved	Reserved	Reserved
	rw	rw	rw	rw	rw	rw	rw	rw

NOTE

Setting b7, or b6, or b5 will put the MC145572 in Timeslot Assigner Mode. In Timeslot Assigner Mode, the IDL2 8/10 mode bit in BR7(b0) is ignored and data is placed according to values programmed in OR0–OR5.

TSA B1 Enable

This bit is used to enable the B1 channel in IDL2 timeslot mode. The B1 timeslot is defined through overlay registers OR0 and OR3. Whenever any channel (B1, B2, or D) is enabled for timeslot mode, all channels enter timeslot mode. If in timeslot mode and TSA B1 Enable is 0, then the B1 channel is not present on the pin D_{out}, and the B1 channel transmit on the U–interface is actively driven to V_{OH}.

TSA B2 Enable

This bit is used to enable the B2 channel in IDL2 timeslot mode. The B2 timeslot is defined through overlay registers OR1 and OR4. Whenever any channel (B1, B2, or D) is enabled for timeslot mode, all channels enter timeslot mode. If in timeslot mode and TSA B2 Enable is 0, then the B2 channel is not present on the pin D_{out}, and the B1 channel transmit on the U–interface is actively driven to V_{OH}.

TSA D Enable

This bit is used to enable the D channel in IDL2 timeslot mode. The D timeslot is defined through overlay registers OR2 and OR5. Whenever any channel (B1, B2, or D) is enabled for timeslot mode, all channels enter timeslot mode. If in timeslot mode and TSA D Enable is a 0, then the D channel is not present on the pin D_{out}, and the D channel transmit on the U–interface is actively driven to V_{OH}.

If both TSA D Enable, and D channel port Enable are set to 1, then the D channel data is presented on both D_{out} and DCH_{out}, and the data transmit onto the U–interface is taken from DCH_{in}. If the D channel port is enabled and TSA D Enable is set to 0, (see overlay register OR8(b0)), then the D channel continues to operate on the D channel port and D_{out} is high impedance during the D channel bit time.

The clock on DCHCLK (assuming the D channel port is enabled), operates relative to FSR based on the timeslot programmed in the timeslot registers for the D channel.

GCI Select M4–BR0

This bit is useful only in conjunction with full GCI mode when the pin MCU/$\overline{\text{GCI}}$ = 0. In that mode, when this bit is set to 0, the GCI C/I channel control automatically sets and resets M4 channel control bits pertaining to the activation state. The bits controlled by the C/I channel are: {`act`, `dea`, `uoa`} in the LT mode, and {`act`, `sai`} in the NT mode. Additionally the {ps1, ps2} bits in the NT mode are transmitted according to the state of IN1 and IN2 pin inputs. When this bit is set to 1, all M4 bits are transmitted according to the data present in register BR0. When operating in full GCI mode, the bit can be set/cleared by using the monitor channel byte register read/write commands. After a hardware or software reset this bit is 0. Normally GCI operation does not require this bit to be set to a 1.

GCI Mode Enable

This bit makes it possible to transfer 2B+D data over the IDL2 interface as if it were in GCI mode. This operation is established by setting the pin MCU/GCI and this bit to 1. The 2B+D data is transferred at the timeslot indicated in OR5(2:0). The Monitor and C/I channels of the GCI interface are ignored as inputs and are not driven as outputs. Additionally, the operation of FSC, regarding its control of the transmit superframe in slave mode, takes precedence over the input on SFAX. See OR5 b(2:0) for GCI slot assignment in this mode.

4.5.8 OR7: Configuration Register 1

This register is used to enable or control various modes of the MC145572. After a hardware or software reset, all bits default to 0 to maintain MC145472/MC14LC5472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
OR7	Internal Analog Loopback rw	Line Connect rw	TSEN DCH Enable rw	IDL2 Rate 2 rw	IDL2 Long Frame Mode rw	`crc` Corrupt Mode rw	`febe`/ `nebe` Rollover rw	M4 Trinal Mode rw

Internal Analog Loopback

When this bit is set to a 1, the analog loopback path is inside the MC145572. Default after any reset is a 0 or external analog loopback path.

Line Connect

When this bit is a 1, the U–interface line can remain connected during analog loopbacks. When this bit is a 0, the line must be disconnected. Default after any reset is a 0.

$\overline{\text{TSEN}}$ DCH Enable

This bit enables $\overline{\text{TSEN}}$ when D channel data is present on the D_{out} or DCH_{out} pins. When the timeslot assigner is enabled, the $\overline{\text{TSEN}}$ signal is active during the timeslot during which D channel data is transferred.

IDL2 Rate 2

In the IDL2 mode, when IDL2 Rate 2 is set to 1, the IDL2 clock (DCL) rate is 512 kHz. IDL2 Clock Speed (see register BR7) is ignored when this bit is set to 1. In full GCI mode, as a master in the NT mode, the DCL clock rate is selected using the pin input (see CLKSEL description in Section 3.3.4). This bit also sets the clock frequency on FREQREF or $FREF_{out}$ when in NT slave mode.

IDL2 Long Frame Mode

While operating as an IDL2 master, this bit controls whether the FSR and FSX operate in long frame or short frame mode. If this bit is 1, both FSR and FSX operate in long frame mode. As an IDL2 slave, the MC145572 determines the mode based on the length of FSR. See **Section 5.4.2**.

`crc` Corrupt Mode

This bit changes the operating mode of the input control bit `crc` Corrupt in register BR8. When `crc` Corrupt Mode is set to 1, the `crc` Corrupt input is used to corrupt one, and only one, outgoing superframe's CRC. When `crc` Corrupt Mode is set to 0, the `crc` Corrupt behaves as it did in the MC145472, unaligned to the transmit superframe, and continues to affect the `crc` data until explicitly reset.

`febe`/`nebe` Rollover

This bit changes the operating mode of the `febe` and `nebe` counter registers BR4 and BR5. When `febe`/`nebe` rollover is set to 1, the `febe` and `nebe` counter registers do not saturate at all 1s but instead rollover from $FF to $00. When `febe`/`nebe` rollover is set to 0, the `febe` and `nebe` counter registers behave just as they do in the MC145472.

M4 Trinal Mode

This bit changes the operating mode of the persistence checking performed on the `act`, `dea`, `sai`, and `uoa` bits in the deframer. When M4 Trinal Mode is set to 1, the checked M4 bits must be valid for 3 consecutive superframes before asserting Verified `act`, or Verified `dea`, etc. When M4 Trinal Mode is set to 0, the checked M4 bits behave as they did in the MC145472, only checking them as configured in BR9(b5,b4). When operating in full GCI mode, the MC145572 performs trinal checks on the received M4 channel `act`, `dea`, `sai`, and `uoa` bits (see Table 4–11).

4.5.9 OR8: Configuration Register 2

This register is used to control Dump/Restore operation, SFAX and SFAR outputs, and three–state enable for off–chip bus drivers. After a hardware or software reset, all bits default to 0 to maintain MC145472/ MC14LC5472 compatibility.

	b7	b6	b5	b4	b3	b2	b1	b0
OR8	D/R Mode 1 rw	D/R Mode 0 rw	SFAX Output Enable rw	FREQREF Output Enable rw	TSEN BCH Enable rw	Reserved rw	SFAX/ SFAR Enable rw	D Channel Port Enable rw

CAUTION

Reserved bit b2 must be set to 0 at all times.

D/R Mode (1:0)

These bits control the operating mode of the Dump/Restore Access Overlay Register OR12. {0,0} sets the mode for normal dumping and restoring of the internal coefficients via the EYE_{out} interface. {1,0} permits read access to the arctap. {0,1} permits write access to the arctap. {1,1} should be selected to perform dump/restore via the IDL2 or GCI interface depending on the state of the MCU/GCI pin.

SFAX Output Enable

When this bit is set to 1 in LT mode, it forces the SFAX pin to be an output. Normally, in the LT mode, SFAX is an input to control the start of the transmit superframe.

FREQREF Output Enable

When this bit is set to 1 in the NT mode, it forces the pin FREQREF to become an output.

$\overline{\text{TSEN}}$ BCH Enable

When this bit is set to 1, it enables the pin $\overline{\text{TSEN}}$ to operate an off–chip bus driver during the B1 and B2 timeslots. When the timeslot assigner is enabled, the TSEN signal is active during the timeslot in which B1 and B2 channel data is transferred.

SFAX/SFAR Enable

When this bit is set to 1, it enables two pins on the MC145572 to be used to control and/or indicate the location of the transmit and receive superframes relative to the IDL2 interface.

D Channel Port Enable

When this bit is set to 1 and pin MCU/$\overline{\text{GCI}}$ = 1, three pins are enabled on the MC145572 to be used as a D channel port. When the D channel port is enabled, D channel information transmitted on the U–interface is taken from DCH_{in}, and D channel information from the U–interface is transmitted on both DCH_{out} and D_{out}. (Note that D_{out} does not output the D channel data when the IDL2 interface is in timeslot mode, and the TSA D Enable is not set to 1.)

4.5.10 OR9: Configuration Register 3

This register is used to control analog loopback and clocks that are available at MC145572 pins. After a hardware or software reset, all bits default to 0 to maintain MC145472/MC14LC5472 compatibility.

CAUTION

Reserved bit b7 must be set to 0 at all times.

	b7	b6	b5	b4	b3	b2	b1	b0
OR9	Reserved rw	Open Feedback Switches rw	Analog Loopback rw	CLKOUT 2048 rw	4096 Hirate rw	2048 Disable rw	1536 Disable rw	4096 Disable rw

Open Feedback Switches

When this bit is set to 1, it opens the internal feedback path between the transmit (TxP/TxN) and the receive (RxP/RxN) sections. This feature may be used in conjunction with analog loopback.

Analog Loopback

When this bit is set to 1, it invokes a receive analog loopback on the MC145572.

CLKOUT 2048

When this bit is set to a 1, it enables a 20.48 MHz buffered clock output on pin 25 of the MC145572FN and on pin 8 of the MC145572PB.

4096 Hirate

When this bit is set to 1, it causes the 4.096 MHz clock output to cleanly transition to a 10.24 MHz rate. When set back to 0, the clock cleanly transitions to 4.096 MHz.

2048 Disable
When this bit is set to 1, it causes the 20.48 MHz clock output at BUFXTAL to go to high impedance.

1536 Disable
When this bit is set to 1, it causes the 15.36 CLKOUT pin to go high impedance.

4096 Disable
When this bit is set to 1, it causes the 4.096 CLKOUT pin to go high impedance. This bit may only be written to once, following a hardware or software reset. Once the 4.096 CLKOUT pin has been turned off by setting this bit it can only be re–enabled by asserting a hardware or software reset to the MC145572. This bit is reset by hardware reset, NR0 (b3) = 1 or NR0 (b1) = 1.

4.6 D CHANNEL AND DEBUG REGISTERS

4.6.1 OR12: D Channel Data Register

When BR10(b1) is set to 1, this double buffered register takes the place of normal byte register BR12, and the register becomes an 8–bit read–only/write–only register providing access to the D channel. In this Mode, D channel input data present on the pin interfaces of the MC145572 is ignored. Instead, the D channel is sourced strictly from this register. D channel data received from the U–interface is byte aligned to superframe sync, and is readable through OR12, 8 bits at a time. This register is updated with the received D channel data when SFS, NR1(b3) is a one. Data is transferred from OR12 to the U–interface when SFS, NR1(b3), is a one.

IRQ3 is used to indicate when each new 8 bits of data are received. A special code (1111) is loaded in nibble register NR1, to indicate that the source of the interrupt is the D channel access register. Reading OR12 clears the special code (1111) from NR1, but does not affect any updates in activation status. So if there has been a change in activation status, an interrupt is still queued up even though the D channel interrupt has been cleared. Both transmit and receive D channel data is aligned to the transmit and receive superframes. The MC145572 does not perform any HDLC framing/deframing.

D channel data is transmitted to and received from the U–interface most significant bit first.

OR12	D Channel Transmit Bits (7:0)	wo
	D Channel Transmit Bits (7:0)	ro

NOTE

If this register is used when the timeslot assignment is enabled, the D channel timeslot must not be 0 so as to maintain synchronization with the transmit superframe. This is especially important in LT mode when SFAX is used as an input.

4.6.2 OR13: Dump/Restore Test Register

This register takes the place of byte register BR13 when BR10 B(2) is set, and the register becomes a byte–wide access port to the Dump/Restore mechanism of the U–chip. Two more bits in the overlay registers control the operating mode of the Dump/Restore mechanism. See overlay register OR8. This bit is reset by both hardware and software resets. After a hardware or software reset all bits default to 0 to maintain MC145472/MC14LC5472 compatibility.

OR13	Dump Register Write Access	wo
	Dump Register Read Access	ro