3
PIN DESCRIPTIONS

3.1 INTRODUCTION

This section describes the MC145572 pins and their operation. Additionally, quick reference tables are provided. These tables are organized by the three major modes of operation and by package type.

3.2 PIN DESCRIPTION QUICK REFERENCE

The following tables (Tables 3–1 through 3–5) list the MC145572 pins in functional groups and provide brief pin descriptions. For more detailed information, refer to the section indicated in the title.

Table 3–1. Power Supply and Mode Selection Pins (See Sections 3.3.1 and 3.3.2)

Pin Name	Pin No.		Pin Description
	TQFP	PLCC	
Power Supply Pins			
V_{DD}	27	44	Positive power supply, nominally + 5 V.
V_{SS}	29, 5	2, 22	Negative power supply, nominally ground.
V_{DD} Rx, V_{DD} Tx	30, 38	3, 11	Positive power supply for analog circuits, nominally + 5 V.
V_{SS} Rx, V_{SS} Tx	31, 37	4, 10	Negative power supply for analog circuits, nominally ground.
V_{DD} I/O	7, 20	24, 37	Positive power supply for input and output circuits, nominally + 5 V.
V_{SS} I/O	6, 19	23, 36	Negative power supply for input and output circuits, nominally ground.
CAP 3V	28	1	Connection for internal 3 V regulator decoupling capacitor.
Mode Selection Pins			
$\overline{\text{RESET}}$	41	14	Hardware reset when at a logic low, normal operation when at a logic high. This pin has a Schmitt trigger input.
NT/$\overline{\text{LT}}$	42	15	Hardware selection of LT (logic low) and NT (logic high) operating mode.
MCU/$\overline{\text{GCI}}$	26	43	MCU mode versus GCI mode select input.
PAR/$\overline{\text{SER}}$	40	13	Parallel versus serial control port selection. PAR/$\overline{\text{SER}}$ = 1 (logic high) for a parallel port. PAR/SER = 0 (logic low) for serial control port interfacing.

Table 3–2. Time Division Multiplex Interface Pins (See Section 3.3.3)

Pin Name	Pin No.		Pin Description
	TQFP	PLCC	
Time Division Multiplex Data Interface			
M/$\overline{\text{S}}$	43	16	Master/Slave mode select input for the IDL2 or GCI interface. Master mode for M/S=1 (logic high).
FSR/FSC	10	27	The MCU 8 kHz Frame Sync for data transmitted on the D_{out} pin. In GCI operation, this pin serves as the FSC pin.
FSX	11	28	The MCU 8 kHz frame sync for data input to the D_{in} pin. This pin is not used in GCI mode.
DCL	14	31	MCU bit clock, or GCI 2x bit clock.
D_{out}	13	30	Serial data out of MCU or GCI interface.
D_{in}	12	29	Serial data into MCU or GCI interface.

Table 3–3. Digital Data Interface Pins (See Section 3.3.4)

Pin Name			Pin No.		
MCU/ SCP Mode	**MCU/PCP Mode**	**GCI Mode**	**TQFP**	**PLCC**	**Pin Description**
SCPEN	CS	IN1	4	21	In serial port, MCU mode, SCPEN is the active low SCP enable input. In parallel port, MCU mode, CS is the active low chip select. In full GCI mode, defined when MCU/GCI = 0, this input is IN1.
SCPCLK	R/W	IN2	3	20	In serial port, MCU mode, SCPCLK is the serial control port clock input. In parallel port, MCU mode, R/W is the read versus write indication to the parallel port. In full GCI mode, defined when MCU/$\overline{GCI}$ = 0, this input is IN2.
SCP Rx	D0	OUT1	1	18	In serial port, MCU mode, SCP Rx is the serial control port data input. In parallel port, MCU mode, D0 is the LSB of the parallel data bus. In full GCI mode, defined by MCU/GCI = 0, OUT1 is an output reflecting the state of bit 5 as set in BR7.
SCP Tx	D1	OUT2	2	19	In serial port, MCU mode, SCP Tx is the serial control port data output. In parallel port, MCU mode, this is signal D1 of the parallel data bus. In full GCI mode, defined by MCU/GCI = 0, OUT2 is an output reflecting the state of bit 6 as set in BR7
IRQ	IRQ	—	44	17	Open–drain active low output for microcontroller interrupt.
4.096 CLKOUT	D2	4.096 CLKOUT	17	34	4.096 MHz clock out. In parallel port, MCU mode, this is signal D2 of the parallel data bus.
15.36 CLKOUT	D3	15.36 CLKOUT	18	35	15.36 MHz clock out. Not synchronized to recovered clock in the NT mode. In parallel port, MCU mode, this is signal D3 of the parallel data bus.
BUF XTAL	D4	BUF XTAL	21	38	This is a square wave output from the 20.48 MHz oscillator and it is not synchronized to the recovered clock in the NT mode. In parallel port, MCU mode, This is signal D4 of the parallel data bus.
EYEDATA DCHCLK	D5	S2	22	39	In serial port MCU mode, this pin may carry either EYEDATA or DCHCLK. In parallel port MCU mode, this is signal D5 of the parallel data bus. In full GCI mode, this pin is the S2 input.
TXBCLK DCH_{in}	D6	$FREF_{out}$	23	40	In serial port MCU mode, this pin may carry either TXBCLK or DCH_{in}. TXBCLK is an 80 kHz clock output, aligned and synchronized to the transmitted baud. DCH_{in} is the D channel port serial data input. In parallel port MCU mode, this is signal D6 of the parallel data bus. In full GCI mode, operating as a GCI slave, this pin provides 2.048 MHz or 512 kHz synchronized clock output.
RXBCLK DCH_{out}	D7	CLKSEL	24	41	In serial port MCU mode, this pin may carry either RXBCLK or DCH_{out}. RXBCLK is an 80 kHz clock output, aligned and synchronized to the received baud. DCH_{out} is the D channel port serial data output. In parallel port MCU mode, D7 is the MSB of the parallel data bus. In full GCI mode, operating as a GCI master, CLKSEL selects between 512 kHz and 2.048 MHz for DCL. CLKSEL = 1 selects 2.048 MHz.
SYSCLK 20.48 MHz SFAR TSEN	SYSCLK 20.48 MHz SFAR TSEN	S1	8	25	In either MCU mode, this pin may carry either SYSCLK, 20.48 MHz, SFAR, or TSEN outputs. SYSCLK is a 10.24 MHz clock for sampling EYEDATA. SFAR is the receive data superframe alignment output in the NT and LT modes. TSEN is an active low open–drain buffer enable output, used for enabling a bus driver to buffer MCU data out from the MC145572, onto a PCM highway. TSEN is active only when D_{out} is active. In full GCI mode, this pin is the S1 input.
Tx SFS SFAX	Tx SFS SFAX	S0	9	26	In either MCU mode, this pin may carry either Tx SFS output, or SFAX input/output. When this pin is unused connect a 100 kΩ resistor to V_{SS} in LT mode. Tx SFS is provided for compatibility to the MC145472, which provides an absolute transmit superframe reference. SFAX is the transmit data superframe alignment input in the LT mode, or superframe alignment out put in the NT mode. In LT mode SFAX can also be an output. In full GCI mode, this pin is the S0 input.

Table 3–4. 2B1Q Interface Pins (See Section 3.3.5)

Pin Name	Pin No.		Pin Description
	TQFP	PLCC	
TxP, TxN	36, 39	9, 12	Positive and negative outputs of the differential transmit driver.
RxP, RxN	32, 33	5, 6	Positive and negative inputs to the differential receive circuit.
V_{ref} P, V_{ref} N	35, 34	8, 7	Positive and negative signals for internal voltage reference. Connect a 0.1 μF to 1 μF ceramic capacitor between V_{ref}P and V_{ref}N.

Table 3–5. Phase Locked Loop and Clock Pins (See Section 3.3.6)

Pin Name	Pin No.		Pin Description
	TQFP	PLCC	
FREQREF	25	42	LT mode: 8 kHz reference clock input, (Schmitt trigger input). NT mode: optional synchronized clock output, selected by control register in the MCU mode (MCU/GCI = 1).
$XTAL_{in}$, $XTAL_{out}$	16, 15	33, 32	Input and output signals of the 20.48 MHz crystal oscillator amplifier.

3.3 PIN DESCRIPTIONS

The following descriptions are divided into the same functional groups as the Pin Description Quick Reference Tables in Section 3.2 and provide more information about the particular subsystem of the device and the associated pins. Refer to Figure 3–1 for pin assignments.

3.3.1 Power Supply Pins

The MC145572 has five pairs of V_{DD} and V_{SS} power supply pins. Each of these pairs provides power to a specific portion of the integrated circuit to minimize interaction between the various high performance subsystems on the device. All of the negative power supply pins should be connected to the same ground reference point and all of the positive power supply pins should be connected to the same +5 V power supply source.

NOTE

See Appendix C for printed circuit board layout recommendations.

V_{DD}: Positive Power Supply

This is one of the five positive power supply pins and should be connected to +5 V. V_{DD} provides power to the internal digital circuits of the device and should be decoupled with a 0.1 μF ceramic capacitor to V_{SS}.

V_{SS}: Negative Power Supply

Two of the six negative power supply pins are V_{SS}, and they should be connected to ground. These pins provide a ground reference to the internal digital circuits of the device and each should be decoupled with separate 0.1 μF ceramic capacitors to V_{DD}.

V_{DD} Rx, V_{DD} Tx: Positive Analog Power Supply

Two of the five positive power supply pins are V_{DD} Rx and V_{DD} Tx, and they should be connected to +5 V. These pins provide power to the analog receive and transmit subsystems of the MC145572, and each should be decoupled with separate 0.1 μF ceramic capacitors to V_{SS} Rx and V_{SS} Tx, respectively. These two pins are not tied together internally.

V_{SS} Rx, V_{SS} Tx: Negative Analog Power Supply

Two of the six negative power supply pins are V_{SS} Rx and V_{DD} Rx, and they should be connected to ground. These pins provide a ground reference to the analog receive and transmit subsystems of the device, and each should be decoupled with separate 0.1 μF ceramic capacitors to V_{DD} Rx and V_{DD} Tx, respectively.

V_{DD} I/O: Positive Power Supply Input/Output

Two of the five positive power supply pins are V_{SS} I/O, and they should be connected to +5 V. These pins provide power to the digital input and output circuits of the device and each should be decoupled with a 0.1 μF ceramic capacitor to V_{SS} I/O. These pins can also be connected to 3.3 V to provide I/O compatibility with 3 V interface devices.

V_{SS} I/O: Negative Power Supply Input/Output

Two of the six negative power supply pins are V_{SS} I/O, and they should be connected to ground. These pins provide a ground reference to the digital input and output circuits of the device, each should be decoupled with a 0.1 μF ceramic capacitor to V_{DD} I/O.

CAP 3 V: Core Logic Positive Power Supply

This pin is tied to the internal core logic power supply. An external 0.1 μF to 1.0 μF decoupling capacitor should be connected between this pin and ground. Applications requiring a 3 V power supply may source current from this pin. See Section 10.3, ***Electrical Specifications***, for more information on the limit of the source current. This output is at 5 volts until reset is applied to the MC145572.

3.3.2 Mode Selection Pins

These inputs define the mode of operation for the MC145572. More information on the function of the device in specific modes can be obtained from Section 5, ***MCU Mode Device Functionality*** and Section 8, ***GCI Mode Device Functionality***.

$\overline{\text{RESET}}$: Reset Input

A logic 0 applied to this Schmitt trigger input pin holds the device in a hardware reset condition. A logic 1 puts the device into the normal operating state. Register NR0(b3) provides a similar software reset function, thereby allowing control of this mode from the external microcontroller. This pin must be held low for at least six 20.48 MHz clock periods.

CAUTION

Reset must be asserted until V_{DD} is greater than 4.75 V and the oscillator is stable.

During a hardware reset condition, all Serial Control Port Registers are reset to their default state, and the signals output from the DCL and FSR pins when in the MCU Master mode are halted. In addition, the Tx Driver is put into a low impedance state to terminate the U–Interface and the 2B1Q receiver is unable to detect the activation wake–up tone.

NT/$\overline{\text{LT}}$: NT/LT Select Input

A logic 1 applied to this pin puts the device into the NT mode and a logic 0 puts the device into the LT mode. Note that Byte Register 8, bit 0, also controls NT versus LT mode selection, thereby allowing software control of this mode.

Table 3–6. Operation Mode as Indicated by Mode Input Pins

Mode	MCU/GCI	PAR/SER
GCI	0	1 or 0
MCU/PCP	1	0
MCU/SCP	1	1

NOTES: PCP — Parallel Control Port, external MCU uses 8–bit data port to access registers.
SCP — Serial Control Port, external MCU uses 4 signal serial ports to access registers.

MCU/$\overline{\text{GCI}}$: MCU/GCI Select Input

A logic 1 applied to this pin selects the MCU mode. This requires an external MCU to access the internal control/status register of the MC145572. 2B+D data only is transferred over the time division multiplex bus. In MCU mode, four data formats are available on the IDL2 interface. These are short frame, long frame, GCI 2B+D, and timeslot assigner. A logic 0 applied to this pin selects the GCI time division bus mode.

In GCI mode, 2B+D data and control/status information is interfaced to the MC145572 by a single four signal time division multiplexed bus. The SCP interface is not used and those pins are redefined.

PAR/$\overline{\text{SER}}$: Parallel/Serial Select Input

This pin allows parallel versus serial control port selection when the MC145572 is operating in MCU mode. PAR/SER = 1 selects parallel port operation. PAR/SER = 0 selects serial control port operation. This pin is not used when operating in GCI mode (MCU/GCI = 0), but must be tied either high or low.

3.3.3 Time Division Multiplex Data Interface Pins

This section describes the Time Division Multiplex (TDM) data interface pins.

M/$\overline{\text{S}}$: Master/Slave Select Input

The TDM Interface can be configured as a Master or a Slave with the M/$\overline{\text{S}}$ pin. A logic 1 input at this pin selects the Master mode and a logic 0 selects the Slave mode. The polarity of this pin can be inverted using BR7(b1).

When the MC145572 is configured for master timing and MCU mode, the FSR/FSC, FSX, and DCL pins are outputs and their signals are generated internally. As a Master, the U–Interface Transceiver provides a 2.048, 2.56 MHz, or 512 kHz DCL output as selected in BR7(b2) and OR7(b4).

When the MC145572 is configured for slave timing and MCU mode, the FSR/FSC, FSX, and DCL pins are inputs and their signals are provided externally. As a Slave, the TDM Interface block is designed to accept any clock rate from 256 kHz to 4.096 MHz, inclusive.

In GCI Master mode, FSC, D_{out}, and DCL pins are outputs and D_{in} is an input. Either the 512 kHz or 2.048 MHz clock is available on DCL. FSX is not used.

In GCI Slave mode, D_{out} is an output and FSC, DCL, and D_{in} are inputs. FSX is not used. DCL can accept clock rates up to 8.192 MHz.

FSR/FSC

FSR: MCU Mode Frame Synchronization Receive

FSR is the 8 kHz frame sync for the receive data of the TDM interface. In short frame and time slot assigner mode, the signal at this pin is high for one cycle of the DCL signal and is rising edge aligned with the rising edge of the DCL signal. This pin is an input when the TDM Interface is in Slave mode and an output in the Master mode as established by the M/S pin. See Figures NO TAG through NO TAG.

When the MC145572 is in NT mode and M/$\overline{S}$ = 1, this output is phase locked to the signal received at the U–Interface. As an LT in the Master mode, this output is derived directly from the 20.48 MHz master clock. The frequency of the periodic FSR signal is 8 kHz. As a Slave, the FSR signal must occur at an average rate of 8 kHz (125 μs interval) with a maximum phase deviation from a jitter–free sync of ±48 μs.

In Master Mode, FSR and FSX output the same wave form. In slave mode, both FSR and FSX inputs must be driven by external circuitry. FSR and FSX inputs can be tied together in slave mode and a common sync can be used to drive both inputs.

FSC: GCI Mode Frame Synchronization Receive

In full GCI mode and in GCI 2B+D mode, this pin serves as the FSC pin, and the signal is high for two cycles of the DCL signal and the rising edge is aligned with the rising edge of the DCL signal. This pin is an input when the TDM Interface is in Slave mode and an output in the Master mode as established by the M/S pin. FSC indicates a superframe boundary by going high for one DCL clock. This happens once every 12 ms.

When the MC145572 is in NT mode and M/$\overline{S}$ = 1, this output is phase locked to the signal received at the U–Interface.

As an LT in the Master mode, this output is derived directly from the 20.48 MHz master clock. The frequency of the periodic FSR signal is 8 kHz.

As a Slave, the FSC signal must occur at an average rate of 8 kHz (125 μs interval) with a maximum phase deviation from a jitter free sync of ±48 μs.

FSX: MCU Mode Frame Synchronization Transmit

FSX is the 8 kHz frame sync for the transmit data of the MCU interface. This pin is not used in the GCI mode. The formatting of FSX is mode dependent.

This pin is an input when the TDM Interface is in Slave mode and an output in the Master mode, as established by the M/S pin.

When the MC145572 is in NT mode and M/$\overline{S}$ = 1, this output is phase locked to the signal received at the U–Interface. As an LT in the Master mode, this output is derived directly from the 20.48 MHz master clock. The frequency of the periodic FSR signal is 8 kHz. As a Slave, the FSX signal must occur at an average rate of 8 kHz (125 μs interval) with a maximum phase deviation from a jitter free sync of ±48 μs.

In Master mode, FSR and FSX output the same wave form. In Slave mode, both FSR and FSX inputs must be driven by external circuitry. FSR and FSX inputs can be tied together in slave mode and a common sync can be used to drive both inputs.

DCL: Data Clock Input/Output

This pin is an input when the TDM Interface is in the Slave mode and an output in the Master mode, as established by the M/S pin.

As a timing master in the MCU–NT mode, this pin provides a 2.048 MHz, 512 kHz, or a 2.56 MHz MCU clock output. This choice is programmed in BR7(b2) and OR7(b4). Also see Section 5.4.

When configured as a slave in MCU mode, this pin accepts any clock frequency from 256 kHz to 4.096 MHz, inclusive.

In GCI Mode, this pin provides clock outputs 2.048 MHz or 512 kHz, as selected by CLKSEL. In GCI Slave mode, this pin accepts clock frequencies of 512 kHz to 8.192 MHz inclusive.

In NT master timing of operation, recovered timing is conveyed over DCL by adjusting the width of the clock. The adjustment is made by the internal digital PLL and occurs during two consecutive 8 kHz frames once per U–Interface basic frame. The adjustment consists of adding or subtracting a single 20.48 MHz clock period during the high time of DCL. Since this occurs during two consecutive 8 kHz frames the total adjustment is ± 97 ns once every basic frame. See electrical specifications for the locations of the timing adjustment.

D_{out}: Data Transmit Output

This pin is the output for the 2B+D data received at the U–Interface. The formatting of the data is mode dependent. In GCI mode D_{out} is an open drain output and must be connected to V_{DD} through a pullup resistor. In IDL–2 mode D_{out} goes high impedance when the 2B+D transfer is complete. Refer to Section 5, ***MCU Mode Device Functionality,*** and Section 8, ***GCI Mode Functional Description,*** for more information.

D_{in}: Data Receive Input

This pin is the input for the 2B+D data to be transmitted at the U–Interface. The formatting of the data is mode dependent. Refer to Section 5, ***MCU Mode Device Functionality,*** and Section 8, ***GCI Mode Functional Description,*** for more information. In GCI mode D_{in} must be connected to V_{DD} through a 1.5 kΩ pull-up resistor.

3.3.4 Control/Status Interface Pins

These pins provide a digital transfer interface for the MC145572 when configured for MCU mode. In GCI mode, control and status information is provided over the GCI interface.

$\overline{SCPEN}/\overline{CS}$/IN1

$\overline{SCPEN}$: Serial Control Port Enable Input

This pin, when held low, selects the Serial Control Port (SCP) for the transfer of control, status, and M channel data information into and out of the U–Interface Transceiver. SCPEN should be held low for 8 or 16 periods of the SCPCLK signal in order for information to be transferred into or out of the MC145572. The SCP Interface disregards any SCP operation that is not exactly 8 or 16 SCPCLK clock pulses in length. If the MC145572 is the only SCP device in the system this pin can be tied low and bursted SCP clock can be used to access the register.

$\overline{CS}$: Parallel Control Port Chip Select

In Parallel Control Port mode, this pin acts as an active low Chip Select input.

IN1: Input 1

In full GCI mode, defined when MCU/$\overline{GCI}$ = 0, this is an input bit. IN1 may be read via BR7. In NT mode, IN1 is transmitted as PS1 in the M4 maintenance bits.

SCPCLK/R/$\overline{W}$/IN2

SCPCLK: Serial Control Port Clock Input

This is an input to the device used for clocking data into and out of the SCP Interface. Data is clocked into the MC145572 from SCP Rx on rising edges of SCPCLK. Data is shifted out of the MC145572 SCP Tx pin on falling edges of SCPCLK. SCPCLK can be any frequency from 0 up to 4.096 MHz. An SCP transaction takes place when SCPEN is brought low. Note that SCPCLK is ignored when SCPEN is high (i.e., it may be continuous or it can operate in a burst mode). If the MC145572 is the only SCP device used, the SCPEN pin can be tied low and bursted clocks applied to SCPCLK.

R/$\overline{W}$: Parallel Control Port Read/Write

In Parallel Control Port mode, this pin functions as read versus write indication where write is active low.

IN2: GCI Mode Input 2

IN2 may be read via BR7. In NT mode, IN2 is transmitted as PS2 in the M4 channel maintenance bits.

SCP Rx/D0/OUT1

SCP Rx: Serial Control Port Receive Input

SCP Rx is used to input control, status, and M–channel data information to the U–Interface Transceiver. Data is shifted into the MC145572 on rising edges of SCPCLK. SCP Rx is ignored when data is being shifted out of SCP Tx or when SCPEN is high.

D0: Data 0

In Parallel Control Port mode, this pin functions as bit 0, LSB, of the data bus.

OUT1: GCI Mode Output 1

In full GCI mode, defined by MCU/$\overline{\text{GCI}}$ = 0, OUT1 is an output reflecting the state of the bit as set in BR7. OUT1 is also set high when the GCI Command/Indicate channel command LTD1 is active.

SCP Tx/D1/OUT2

SCP Tx: Serial Control Port Transmit Output

SCP Tx is used to output control, status, and M channel data information from the MC145572 U–Interface Transceiver. Data is shifted out of SCP Tx on the falling edge of SCPCLK, most significant bit first.

D1: Data 1

In Parallel Control Port mode, this pin functions as bit 1 of the data bus.

OUT2: GCI Mode Output 2

In full GCI mode, defined by MCU/$\overline{\text{GCI}}$ = 0, OUT2 is an output reflecting the state of the bit as set in BR7. OUT2 is also set high when the GCI Command/Indicate channel command LTD2 is active.

$\overline{\text{IRQ}}$: Interrupt Request Output

The $\overline{\text{IRQ}}$ pin is an active low, open drain output used to signal an external microcontroller that an interrupt condition exists in the MC145572. On clearing the interrupt condition, the pin is returned to the high–impedance state. See the description for **Nibble Register 3, Section 4.3.4**, for descriptions of the sources of interrupt conditions.

4.096 CLKOUT/D2

4.096 CLKOUT: 4.096 MHz Buffered Clock Output

This pin provides a buffered 4.096 MHz clock output that can be used for a microcontroller clock. This clock is not locked to the recovered clock timing. This output can be disabled by writing a ‘1’ to OR9(b0).

D2: Data 2

In Parallel Control Port mode, this pin functions as bit 2 of the data bus.

15.36 CLKOUT/D3

15.36 CLKOUT: 15.36 MHz Buffered Clock Output

This pin provides a buffered 15.36 MHz clock output that can be used for the MC145474/75 and MC145574 S/T Transceiver clocks. Register BR14(b0) or Register BR15A(b2) must be set to enable this output. This clock is a 20.48 MHz clock with every fourth clock cycle removed. This clock is not locked to the recovered clock timing. This output can be disabled by writing a ‘1’ to OR9(b1). This output can be cleanly transitioned to 10.24 MHz by writing a ‘1’ to OR9(b3).

NOTE

This pin does not provide a 50% duty cycle output. It does provide a clock that the MC145474/75 and MC145574 can use. Figure 10.14 shows the timing of this signal.

D3: Data 3

In Parallel Control Port mode, this pin functions as bit 3 of the data bus.

BUF XTAL/D4

BUF XTAL: Buffered Crystal Output

BUF XTAL is the buffered square wave output from the 20.48 MHz oscillator. After reset, this signal is active. This output can be set to a high–impedance state by setting OR9(b2) to a 1. This signal is available in both MCU/SCP and GCI modes of operation.

CAUTION

In NT mode operation, this signal is not phase locked to recovered timing.

D4: Data 4

In Parallel Control Port mode, this pin functions as bit 4 of the data bus.

EYEDATA/DCHCLK/D5/S2

EYEDATA: Eye Pattern Data Output

Eye Pattern Data is a serial data output that provides a digital word once per received 2B1Q baud. This data word represents the recovered 2B1Q received bauds and can be used to reconstruct a conventional eye pattern on an oscilloscope with the use of a digital–to–analog converter. Control bit BR15A(b0) must be set to 1 to enable this pin. See Appendix D for applications information concerning this feature.

DCHCLK: D Channel Clock

DCHCLK is the D channel port clock output. It is enabled by setting D channel port enable in the Init Group Register OR8 (b0).

D5: Data 5

In Parallel Control Port mode, this pin functions as bit 5 of the data bus.

S2: GCI Mode Slot Selection 2

In full GCI mode, this pin is an input for the time slot selection, S0–S2. See Table 3–7 for more information.

Table 3–7. GCI Time Slot Assignment as Set by S0–S2

GCI Time Slot	S2	S1	S0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Tx BCLK/DCH_{in}/D6/$FREF_{out}$

Tx BCLK: Transmit Baud Clock Output

This 80 kHz clock indicates the timing of the transmitted and received 2B1Q bauds. Control bits BR14(b0) or BR15A(b0) must be set to logic 1 to enable this signal.

DCH_{in}: D Channel Data In

DCH_{in} is the D channel port serial input. It is enabled by setting D channel port enable in the Init Group Register OR8(b0).

D6: Data 6

In Parallel Control Port mode, this pin functions as bit 6 of the data bus.

$FREF_{out}$: GCI Mode Locked Frequency Output

In full GCI mode, operating as a slave, this pin provides 2.048 MHz or 512 kHz synchronized clock output as selected by CLKSEL. When the MC145572 is configured as a GCI timing master, $FREF_{out}$ does not provide a clock since the clock is present on DCL. It is not necessary to set any register bits to enable this output in GCI slave mode.

Rx BCLK/DCH_{out}/D7/CLKSEL

Rx BCLK: Transmit Baud Clock Output

This 80 kHz clock indicates the timing of the transmitted 2B1Q bauds. Control bits BR14(b0) or BR15A(b0) must be set to logic 1 to enable this signal.

DCH_{out}: D Channel Data Out

DCH_{out} is the D channel port serial output. It is enabled by setting D channel port enable in the Init Group register OR8(b0).

D7: Data 7

In Parallel Control Port mode, this pin functions as bit 7 of the data bus.

CLKSEL: Clock Select

When operating as a GCI timing master in full GCI mode, CLKSEL selects between 512 kHz and 2.048 MHz for DCL. CLKSEL = 1 selects 2.048 MHz.

When operating as a GCI timing slave in full GCI–NT mode, CLKSEL selects between phase locked 512 kHz and 2.048 MHz clocks appearing at $FREF_{out}$.

SYSCLK/SFAR/$\overline{TSEN}$/S1

SYSCLK: System Clock Output

System Clock Output is a 10.24 MHz clock that is used to clock Eye Pattern Data. Control bits BR14(b0) or BR15A(b0) must be set to '1' to enable this signal. See **Appendix D** for applications information concerning this pin.

SFAR: Superframe Alignment Receive

SFAR provides a superframe alignment output signal in the NT and LT modes. This signal is only available when the MC145572 is in MCU mode. Setting OR8 (b1) enables this output. This signal is one MCU clock wide and occurs during the DCL clock following FSR. See **Section 5.4.7**.

$\overline{TSEN}$: Open–Drain Buffer Enable Output

TSEN is an open–drain buffer enable output, used for enabling a bus driver to buffer TDM data out from the MC145572 onto a PCM highway. When the MC145572 is configured for MCU mode, TSEN is active during the B1, B2, and D channel time slots, regardless of where they occur. When the MC145572 is configured for GCI 2B+D electrical–only interfacing while in MCU mode, TSEN is active during the B1, B2, and D channel time slots only. TSEN is also available when the MC145572 is configured for time slot assigner operation. When separate D channel serial port option is enabled, TSEN is active only during the B1 and B2 channel time slots. This pin is enabled when OR7(b5)=1 or OR8(b3)=1.

S1: GCI Mode Slot Selection 1

In full GCI mode, this pin is an input for the time slot selection, S0–S2.

Tx SFS/SFAX/S0

Tx SFS: Transmit Superframe Sync Output

This output pulses high 8 bauds prior to the transmit sync word separating the first and second transmitted basic frames in a superframe. Control bits BR14(b0) and BR15A(b3) must both be set to a 1 to enable this pin. The Tx SFS output is coincident with the Tx Baud Clock.

TX SFS is provided for compatibility to the MC145472, which provides an absolute transmit superframe reference.

SFAX: Superframe Alignment Transmit

SFAX is the transmit superframe alignment input in the LT mode, or superframe alignment output in the NT mode. SFAX is enabled by setting SFAX/SFAR Enable in the Init Group Register OR8 (b1). SFAX may be configured as an output in LT mode by setting OR8 (b5). See **Sections 4.5.9** and **5.4.7.** When GCI 2B+D mode is enabled, OR6(b3) = 1, the SFAX function is superceded by modulation of the FSC input.

WARNING

For MCU–LT mode a 100 kΩ pull–down resistor must be connected to this pin if either TxSFS or SFAX functions are not enabled prior to start of activation.

S0: Slot Selection 0

In full GCI mode, this pin is an input for the time slot selection, S0–S2.

3.3.5 2B1Q Line Interface Pins

These pins form the 2B1Q Interface of the MC145572 U–Interface Transceiver. Refer to **Section 5.7** and **Appendix B** for information on the line interface.

TxP and TxN: Transmit Positive and Transmit Negative Outputs

These are the differential analog output pins of the transmit line driver.

RxP and RxN: Receive Positive and Receive Negative Inputs

These are the differential analog input pins to the 2B1Q receiver.

$V_{ref}P$ and $V_{ref}N$: Reference Voltage Positive and Reference Voltage

Connect a 0.1 μF ceramic capacitor between these pins.

3.3.6 Crystal Oscillator and Phase Locked Loop (PLL) Pins

In the LT mode, the MC145572 derives its 20.48 MHz master clock from a clock reference using an on–chip PLL with an 8 kHz clock reference applied to pin FREQREF.

In the NT mode, no reference clock is required, since timing is recovered from the line. External circuitry is the same for both NT and LT modes.

FREQREF: Frequency Reference

This Schmitt trigger digital input pin accepts the 8 kHz reference frequency for the analog phase locked loop in LT mode. For ISDN central office applications, the frequency applied at this pin should be stable to ± 5 ppm to meet ANSI T1.601–1992 requirements. Some ANSI and ETSI applications require a ± 32 ppm reference.

LT Mode: In the LT mode, an 8 kHz clock is used for the reference clock. Typically, this clock can be the same 8 kHz synchronization input as connected to FSR or FSX.

NT Mode: In the NT mode, FREQREF is normally not used, but can be enabled as an output. In a slave–slave application where the MC145572 is in slave mode (i.e., M/S = 0), and configured for NT operation, a clock output that is synchronized to the loop is required so that external circuitry can generate frame sync and clock signals. FREQREF or $FREF_{out}$ can be used to provide a clock output locked to the recovered data from which IDL or GCI bus timing can be derived.

MCU Mode: In MCU/$\overline{GCI}$ = 1 mode, FREQREF is enabled as an output when the MC145572 is configured for NT mode by setting OR8(b4) to a '1'. Also see descriptions for BR7(b2) and OR7(b4).

GCI Mode: In MCU/$\overline{\text{GCI}}$ = 0 mode, a separate pin, FREF_{out}, provides the synchronized clock and is available for all configurations except for when Tx BCLK is enabled. The rate is selectable between 512 kHz and 2.048 MHz in NT mode.

XTAL_{in} and XTAL_{out}: Crystal Input and Crystal Output

A 20.48 MHz pullable crystal is connected between XTAL_{in} and XTAL_{out} to form a voltage–controlled crystal oscillator in the LT or NT modes. No other external components are required. See Section H.3 for information on how to characterize the pullable crystal.

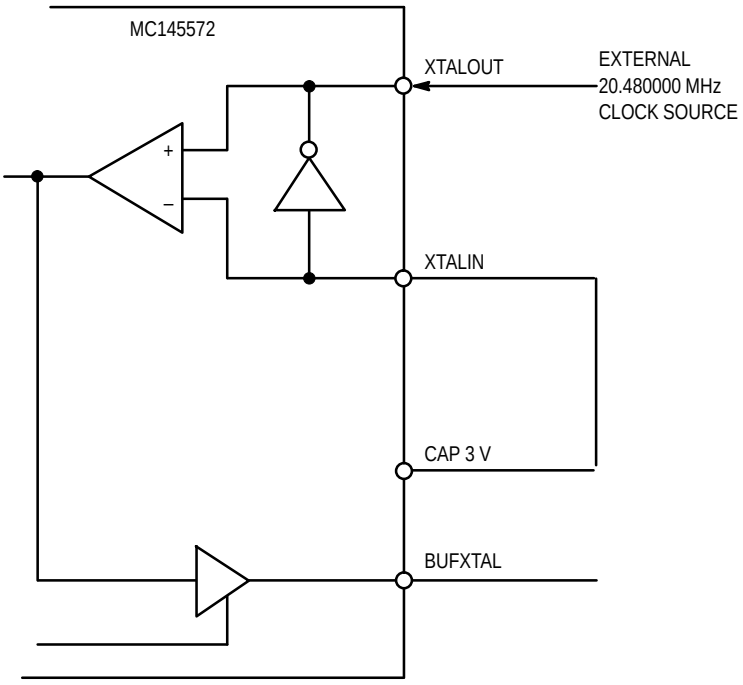

Figure 3–1. Method to Drive MC145572 with External Clock