C
PRINTED CIRCUIT BOARD LAYOUT

C.1 INTRODUCTION

The MC145572 is manufactured using high speed CMOS VLSI process technology to implement the mixed signal processing functions required in the device. The U–interface transceiver has a high resolution sigma–delta analog–to–digital converter (ADC) and a precision digital–to–analog converter (DAC) in addition to three high speed digital signal coprocessors. The fully differential analog circuit design techniques used for this device result in superior performance for the ADC, DAC, and Tx Driver sections. Special attention was given to the design of the MC145572 to reduce sensitivity to noise, including power supply rejection, and susceptibility to radio frequency noise. This special attention to circuit design results in an ADC with greater than 84 dB dynamic range on the same monolithic chip as the digital signal coprocessors clocking at 10.24 MHz, all of which operates on a single 5 volt power supply. This device was designed to ease the task of printed circuit board layout, but due to the wide analog dynamic range and high digital clock rate, special care should be taken during PCB layout to assure optimum transmission performance.

NOTE

When laying out the PCB, do not run any digital signals through the line interface region of the board. Switching noise from the digital signals can be coupled into the line interface and reduce performance, especially on long loops. Wire wrap is not recommended for prototyping.

C.2 PRINTED CIRCUIT BOARD MOUNTING

The device should be soldered to the PC board for production manufacturing. If the device is to be used in a socket, it should be placed in a low parasitic pin capacitance socket of 1.5 pF or less.

C.3 POWER SUPPLY, GROUND, AND NOISE CONSIDERATIONS

This device is often used in digital switching equipment applications which require plugging the PC board into a rack with power applied. This is referred to as “hot–rack insertion”. In these applications, care should be taken to limit the voltage on any pin from going positive relative to the V_{DD} pins or negative relative to the V_{SS} pins. One method to accomplish this is to extend the ground and power contacts of the PCB connector so that power is applied prior to any other pins having voltage applied. The device has input protection on all pins and may source or sink a limited amount of current without damage. See Section 10.1, Absolute Maximum Ratings, for more information concerning the current into or out of the device pins. Current limiting may be accomplished by series resistors between the signal pins and the connector contacts.

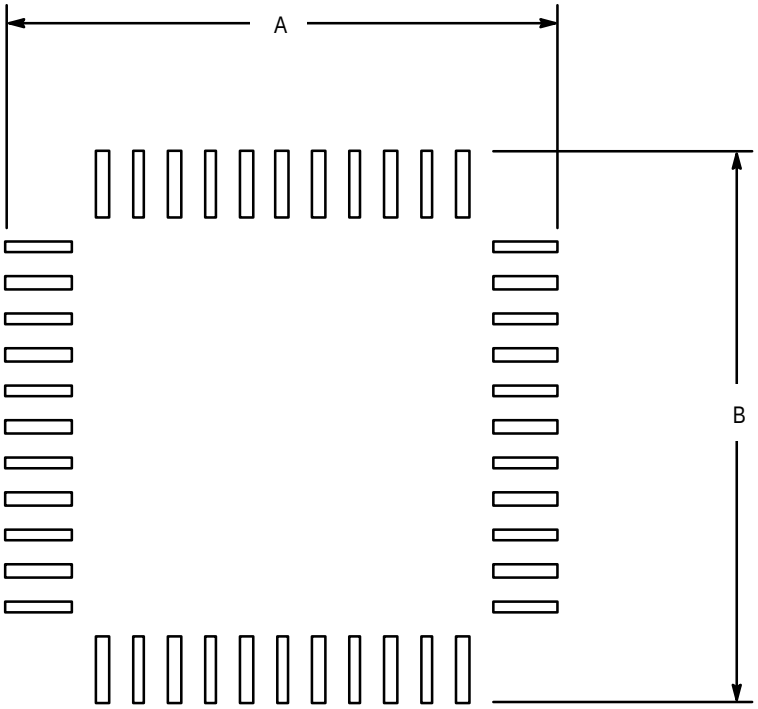
The most important considerations for PCB layout deal with noise. This includes noise on the power supply, noise generated by the digital circuitry on the device, and coupling digital signals into the analog signals. The best PCB layout methods to prevent noise induced problems are:

1) Keep digital signals as far away from analog signals as possible.
2) Use short, low inductance traces for the analog circuitry to reduce inductive, capacitive, and radio frequency noise sensitivities.
3) Use short, low inductance traces for digital circuitry to reduce inductive, capacitive, and radio frequency radiated noise.
4) Bypass capacitors should be connected between the V_{DD} and V_{SS} pairs with minimal trace length. These capacitors help supply the instantaneous currents of the digital circuitry in addition to decoupling the noise that may be generated by other sections of the device or other circuitry on the power supply.

5) Use short, wide, low inductance traces to connect all of the V_{SS} ground pins together and, with one trace, connect all of the V_{SS} ground pins to the power supply ground. Depending on the application, a double sided PCB with a V_{SS} ground plane under the device connecting all of the digital and analog V_{SS} pins together would be a good grounding method. A multi–layer PCB with a ground plane connecting all of the digital and analog V_{SS} pins together would be the optimal ground configuration. These methods will result in the lowest resistance and the lowest inductance in the ground circuit. This is important to reduce voltage spikes in the ground circuit resulting from the high speed digital current spikes. Suppressing these voltage spikes on the integrated circuit is the reason for multiple V_{SS} ground leads.
6) Use short, wide, low inductance traces to connect all of the V_{DD} power supply pins together and, with one trace, connect all of the V_{DD} power supply pins to the 5 volt power supply. Depending on the application, a double sided PCB with V_{DD} bypass capacitors to the V_{SS} ground plane under the device, as described in 5) above, may complete the low impedance coupling for the power supply. For a multi–layer PCB with a power plane, connecting all of the digital and analog V_{DD} pins to the power plane would be the optimal power distribution method. The integrated circuit layout and packaging considerations for the 5 volt V_{DD} power circuit are essentially the same as for the ground circuit.
7) Motorola recommends that a four layer board be used. It is possible to use a two layer board but special care must be taken. See Figure C–1.
8) The 20.48 MHz crystal must be located as close as possible to the MC145572 package. This is required to minimize parasitic capacitances between crystal traces and ground.

Figure C–1 shows a suggested board layout for a two layer board. This drawing is not done to scale. Trace vias are shown. Depending on the application other pins may need to be connected to V_{DD} or V_{SS}. All bypass capacitors should be located as close as possible to the V_{SS}/V_{DD} pins. The suggested layout shows the power feed to the MC145572 coming from a common point. This is important in a two layer implementation. The 10 μF electrolytic capacitor is recommended to filter out any ripple or noise that may be on the board in a two layer application. Even though the MC145572 has very high power supply rejection, good power supply decoupling is recommended.

If a four layer board with full power and ground planes is used, the V_{DD} and V_{SS} pins can be connected directly to the appropriate plane by vias.



NOTE: Dimensions given in millimeters are hard metric numbers and PCB pad designs must be done in metric. Likewise dimensions given in inches must be designed in inches. This is especially important on conversions involving lead pitch where a small fractional error, repeated many times across the width of a package, will make it impossible to align all leads to pads.

Package	Lead Pitch	Pad Size	Dimension A	Dimension B	Device	Units
44 PLCC	0.050	0.025 x 0.075	0.705	0.705	MC145572FN	inches
44 TQFP	0.8	0.5 x 1.6	13	13	MC145572PB	mm

Figure C–1. MC145572 Printed Circuit Board Footprint Dimensions

C.4 OSCILLATOR LAYOUT GUIDELINES

All traces must be as short as possible to reduce stray capacitance and inductance. The traces to XTAL IN and XTAL OUT must be kept as short as possible with minimal width to keep stray capacitance less than 1 pF. Other digital signals should not be routed near the crystal traces. Any passive components for the oscillator or PLL should have short leads and should be soldered to the PC board. Wherever possible the layout should be symmetrical so the stray capacitances from each pin of the crystal to ground are equal.

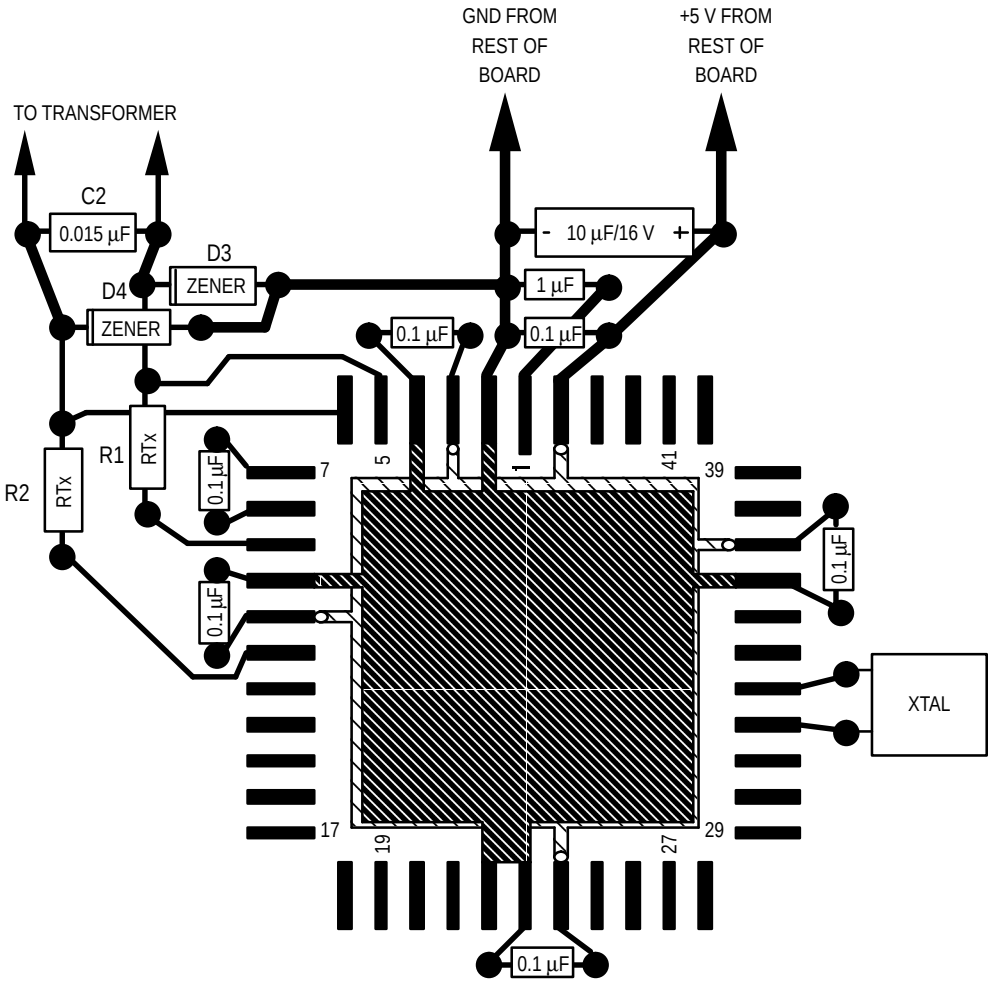
When a four layer board is used do not route ground or power plane material underneath the 20.48 MHz crystal oscillator circuitry. This is to minimize parasitic capacitances between the 20.480 MHz oscillator traces and the power or ground plane. Excessive parasitic capacitance between the traces and power/ground planes decreases the pull range of the 20.48 MHz Oscillator.

C.5 2B1Q INTERFACE GUIDELINES

The line interface into and out of the device is differential, implying symmetry. It is recommended that the layout of the 2B1Q interface be as symmetrical as possible to avoid any imbalances to this circuit. Do not run any digital traces through the line interface region of the printed circuit board.

C.6 PACKAGE FOOTPRINTS FOR PRINTED CIRCUIT BOARDS

Figure C–2 gives suggestions for a two–layer printed circuit board layout of surface mount packages used for the MC145572FN package.



NOTES:
1. Figure is shown for 44 PLCC package.
2. Figures 5–38(a) and 5–38(b) are used for reference.

Figure C–2. MC145572 Suggested PCB Layout