# 7

# MCU MODE MAINTENANCE CHANNEL OPERATION

## 7.1 INTRODUCTION

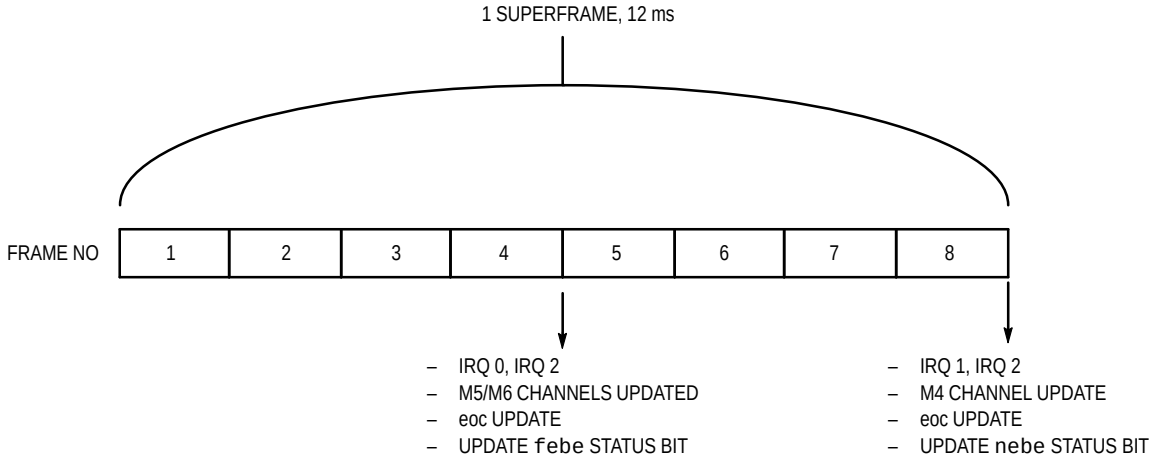
When configured for MCU mode operation the MC145572 provides a very flexible interface to the 4 kbps maintenance channel (M channel) defined in ANSI T1.601–1992. The maintenance channel consists of 48 bits sent by both the LT and NT configured U–interface transceivers during the course of a superframe. These 48 bits are divided into six subchannels designated M1 through M6, each consisting of eight bits per superframe. The Embedded Operations Channel (eoc) consists of M1, M2, and M3. The overhead bits, such as `crc`, `febe`, `act`, and `dea`, are contained in subchannels M4, M5, and M6.

An external microcontroller can read from or write to the maintenance channel via the SCP or PCP Interfaces. Interrupts to an external microcontroller can be enabled when an eoc, M4, M5, or M6 channel register is updated. Maintenance channel registers can be configured to update when a new value is detected between successive superframes, when a bit changes, or when two or three successive superframes of a new value are detected. The M4 channel `act` bit, BR1(b7), can also be configured to automatically enable or disable customer data when in NT or LT mode of operation. The M4 channel `dea` bit, BR1(b6), can also be configured to automatically issue a deactivation request in NT mode of operation. The maintenance channel registers are updated only when Superframe Sync, NR1(b1), is set to 1.

Sections 7.5 and 7.6 provide information of interest to designers of LULT/LUNT type line cards for use in digital loop carrier systems using end to end performance monitoring.

See the BR9 description in subsection 7.4.10 for more details on the maintenance channel register operations. Figure 7–1 shows the relationship between the received superframe and when the interrupt line is asserted when the appropriate interrupts have been enabled.

The text in this section is based on an ANSI T1.601 compliant application. Due to the flexibility of the MC145572 register interface, it can easily be used in proprietary applications.




NOTE: Since the eoc register, R6, is updated after basic frames 4 and 8, IRQ 2 can occur at either location, or both, depending on setting of BR9(B7:b6).

**Figure 7–1. Maintenance Channel Interrupt Timing**

## 7.2 EMBEDDED OPERATIONS SUBCHANNEL

The eoc subchannel can operate in one of three modes. The eoc register R6 can be updated and an interrupt generated on every received eoc frame and on a successful trinal check of a new eoc frame. This applies to the NT and LT modes of operation. In the NT mode, the MC145572 also provides an Automatic eoc Processor for automatic decoding and response to the ANSI T1.601–1992 eoc messages. The R6 update occurs only when Superframe Sync, NR2(b1), has been detected and set to 1. When the microcontroller writes to the eoc register, R6, the new eoc word is loaded into the Superframe Framer on the next eoc frame boundary assuming the automatic eoc mode is not enabled. These modes are selected by eoc Control 1 and eoc Control 0, BR9(b7:b6).

In the trinal check mode, R6 is updated when three consecutively received eoc frames are the same. When the automatic eoc mode with trinal check has been selected and the U–interface transceiver is operating as an NT, the decoded eoc is acted upon when a valid trinal check has occurred and R6 is updated.

R6 can be configured to update on every eoc frame by setting eoc Control 1 and eoc Control 0, BR9(b7:b6), each to 1. The update occurs every 6 ms even if no change has been detected between eoc frames. This mode must be used for proprietary and non–ISDN Basic Rate applications.

**CAUTION**

Read text in section 4.4.10 concerning trinal check mode very carefully.

R6 is updated in all modes of operation. This permits an external microcontroller to monitor eoc messages when the Automatic eoc Processor is enabled in NT mode. R6 is updated at the mid–point or at the end of a superframe.

Regardless of the mode of operation, an update of R6 generates an interrupt whenever Enable IRQ 2, NR4(b2), is set to 1.

## 7.3 M4 SUBCHANNEL AND DATA TRANSPARENCY

The M4 subchannel operates in one of four modes set in BR9(b5:b4). The received M4 data from the Superframe Deframer is available in BR1. The transmitted M4 subchannel data is written to Byte Register BR0. See BR9 in section 4.4.10 and Verified `act` and Verified `dea`, BR3(b2:b1), in section 4.4.4 for more details on the M4 channel register operations. When set to a 1, the M4 Trinal Mode bit, OR7(b0), configures the M4 `uoa`, `sai`, `dea` and `act` bits to be updated after a trinal check. See descriptions for BR0, BR9 and OR7 for more details.

M4 Control mode 0,0 is the dual consecutive mode of operation with automatic verification of the M4 `act` bit in the LT and NT modes and automatic verification of the M4 `dea` bit in NT mode. In this mode, once Superframe Sync, NR2(b1), is set to 1, BR1 and Verified `act`, BR3(b2), are updated when the Superframe Deframer detects that an M4 channel bit has changed state and has remained in that state for two consecutive superframes. The M4 maintenance subchannel bits `act`, `dea`, `sai` and `uoa` can be configured for trinal checking by setting OR7(b0) to a 1.

When OR7(b0) is set to 1, the received M4 bit positions in BR1 corresponding to `act`, `dea`, `sai` and `uoa` are updated on a trinal check regardless of the programmed M4 CONTROL bits in BR9(b5, b4). The remaining bits in BR1 are updated according to the programmed M4 CONTROL bits in BR9(b5, b4). Note that the Verified `act`/`dea` mode BR9(b5, b4) = 0,0 operates on trinal checked M4 `act` and `dea` bits when OR7(b0) is a 1. See Table 4–7 and sections 4.4.10 and 4.5.9.

In either the LT or NT modes of operation, customer data transparency is achieved by the logical OR of Verified `act`, BR3(b3), and Customer Enable, NR2(b0). This means when the received M4 `act` bit is a 1 and the M4 channel is configured in the Verified `act`/`dea` mode, data transparency is automatically enabled. If the Verified `act`/`dea` mode is not enabled Customer Enable, NR2(b0), must be set to a 1 to permit transmission of 2B+D data onto the U–interface.

When Customer Enable, NR2(b0), is set to a 1, data transparency occurs on the next IDL frame boundary, not the next superframe boundary. The recommended procedure is for firmware in the NT1 to assert the `act` bit, BR0(b7), to a 1 after it has determined that the NT1 is ready for layer two transmission. This should be immediately followed by setting Customer Enable, NR2(b0), to a 1. Section 6.4.6.6

of ANSI T1.601–1992 indicates that data transparency may occur during the last superframe having its act bit equal to 0 or during the first superframe having its act bit equal to 1.

In the NT mode of operation, the M4 dea bit is checked for a 0 and the logical OR of Verified dea, BR3(b1), and deactivation Request, NR2(b2), ensures that the NT U–interface transceiver deactivates in a controlled manner and will re–activate in warm start mode on a subsequent activation attempt. An interrupt is generated when BR1 is updated if Enable IRQ 1, NR4(b1), is set to a 1.

M4 Control mode 0,1 is the dual consecutive mode of operation. BR1 is updated when the Superframe Deframer detects that an M4 subchannel bit has changed state and has remained in that state for two consecutive superframes and Superframe Sync, NR2(b1), is set to 1. An interrupt is generated at this time if Enable IRQ 1, NR4(b1), is set to a 1.

M4 Control mode 1,0 is the delta mode of operation. The M4 channel register is updated with new M4 channel data whenever any single bit changes between received M4 frames. An interrupt is generated at this time if Enable IRQ 1, NR4(b1), is set to 1.

M4 Control mode 1,1 updates the M4 channel register BR1 on every received superframe. In this mode, the Superframe Deframer does not check for a change in data between received M4 frames. An interrupt is generated at this time if Enable IRQ1, NR4(b1), is set to 1.

## 7.4 M5 AND M6 CHANNELS

The M5 and M6 channels operate in the same modes as the M4 channel bits except for the automatic verification mode. The received M5 and M6 data from the Superframe Deframer is available in BR2. See BR9 for details on the operating modes of the M5 and M6 channels. These channels are configured as a pair. An interrupt is generated when BR2 is updated and Enable IRQ 0, NR4(b0), is set to 1. As defined by ANSI T1.601–1992 these are reserved maintenance channels and should be initialized to 1s. The M5 and M6 maintenance channels are available for proprietary applications which do not have to comply with ANSI T1.601.

## 7.5 febe AND nebe BITS

The MC145572 has extensive febe (Far End Block Error) and nebe (Near End Block Error) maintenance capabilities. The state of the received computed nebe and of the received febe is available through the register interface. Also, two independent febe and nebe counters are available for performance monitoring purposes.

The received febe from the last completed superframe is available in Received febe, BR3(b4). It is updated at the end of each superframe when both Superframe Sync and Linkup, NR1(b3, b1), are set to 1.

The febe/nebe Control bit, BR9(b1), controls operation of the transmitted febe status bit. When BR9(b1) is set to 1, the transmitted febe bit is set to whatever is set in the febe input, BR2(b4). When BR9(b1) is reset to 0, the transmitted febe is set active if the computed nebe is active or if febe Input, BR2(b4), is active. In this case “active” means 0. BR9(b1) reset to 0 is the normal mode of operation and no intervention is required by an external MCU for the MC145572 to send the outgoing febe bit.

In NT and LT mode operation when BR9(b1) is set to 1, BR2(b4) must be cleared to a 0 at the end of reception of basic frame 8 when it is desired to force an outgoing febe. BR2(b4) must be set to a 1 at the end of reception of basic frame 8 when no outgoing febe is required. Software should always configure BR2(b4) for the correct outgoing febe once each superframe. In digital loop carrier applications, this guarantees that there will be a one to one correspondence between the febe status received from the digital carrier system and the febe transmitted on the U–interface. The febe is transmitted at the end of basic frame 2. See Figure 7–1 for interrupt timing information. Please read Section 7.7.

The computed nebe of the last completed superframe is available in Computed nebe, BR3(b3). This bit is set or cleared as a result of a cyclic redundancy check (crc) of the last superframe received. This bit is updated at the end of each superframe. The Computed nebe is reset to 0 when a crc error is detected and is set to 1 when no crc error is detected. When either Superframe Sync or Linkup, NR1(b3, b1), are reset to 0 the Computed nebe bit is forced to 0.

The current febe count is maintained in BR4. The count in BR4 is incremented only when the received febe bit is detected active (0) at the end of the superframe. When OR7(b1) is a 0 the febe counter does not wrap around when the count reaches $FF. When OR7(b1) is a 1 the febe counter wraps around and continues counting from 0. Also, BR4 should be reset to 00 after Linkup is detected during activation. This is done by the external microcontroller writing 00 to BR4. The count is incremented when both Superframe Sync and Linkup in NR1(b1, b3) are set to 1 and the received febe bit is a 0. Received febe is available in BR3(b4) and is a 0 when active.

The current nebe count is maintained in BR5. The count in BR5 is incremented only when the Computed nebe bit is detected active (0) at the end of the superframe. The count is also incremented once per superframe during loss of synchronization, i.e., if Superframe Sync, NR2(b1), drops to a 0 when Linkup, NR2(b3), is set to 1. When OR7(b1) is a 0 the nebe counter does not wrap around when the count reaches $FF. When OR7(b1) is a 1 the nebe counter wraps around and continues counting from 0. Also, BR5 should be reset to 00 after Linkup is detected during activation. This is done by the external microcontroller writing 00 to BR5. The count is incremented when both Superframe Sync and Linkup in NR1(b1, b3) are set to 1 and when an error is detected in the received crc. A Computed nebe is active when the received crc does not exactly match the calculated crc on the received superframe data. The Computed nebe is available in BR3(b3) and is a 0 when a crc error has been detected.

## 7.6 FORCE CORRUPT crc

The MC145572 provides a mechanism where the outgoing crc can be corrupted. The transmitted crc is corrupted when BR8(b3) is set to a 1. The crc corruption is accomplished by inverting the transmitted crc bits. The next two paragraphs are of particular interest to designers of digital loop carrier system LULT and LUNT type line cards.

In NT mode operation, when it is desired to corrupt the outgoing crc, BR8(b3) should be set at the end of reception of basic frame 4 and must be cleared at the end of reception of basic frame 8. This inverts the outgoing crc in transmitted basic frames 4, 5, 6 and 7 of the current transmitted superframe. See Figure 7–2. When crc Corrupt Mode, OR7(b2), is set to a 1 it is not necessary to clear BR8(b3) since it is cleared automatically at the end of the transmitted superframe. This guarantees that the corrupt crc will be transmitted only in the current superframe and that there will be a one to one correspondence between the corrupt crc status received from a digital carrier system and the corrupt crc transmitted on the U–interface. Please read Section 7.7.

In LT mode operation, when it is desired to corrupt the outgoing crc, BR8(b3) should be set at the end of reception of basic frame 8 and must be cleared at the end of reception of basic frame 8. This inverts the outgoing crc in transmitted basic frames 1 through 8 of the current transmitted superframe. See Figure 7–3. When crc Corrupt Mode, OR7(b2), is set to a 1 it is not necessary to clear BR8(b3) since it is cleared automatically at the end of the transmitted superframe. This guarantees that the corrupt crc will be transmitted only in the current superframe and that there will be a one to one correspondence between the corrupt crc status received from a digital carrier system and the corrupt crc transmitted on the U–interface. Please read Section 7.7.

The crc CORRUPT MODE bit, OR9(b2), modifies the operation of crc CORRUPT, BR8(b3). When OR9(b2) is a one the operation of the crc CORRUPT bit, BR8(b3), is modified so that a corrupt crc is transmitted only to the end of the current U–interface superframe. Then BR8(b3) is cleared to a 0. If it is desired to corrupt the transmitted crc again then BR8(3) must be set to a 1 again. This is very useful for digital loop carrier applications since software does not have to clear BR8(b3) in order to guarantee a one–to–one correspondence between crc received from the digital loop carrier system and crcs transmitted onto the U–interface. For digital loop carrier applications BR9(b1) is set to a 1 if it is desired to have end to end performance monitoring. The outgoing febe should be updated at the same time that the outgoing M4 channel register is updated. This update should be done for every superframe.

**Table 7–1. Transmitted crc Configuration**

| BR8(b3) | OR9(b2) | Effect on transmitted cyclic redundancy check (crc) |
|---|---|---|
| 0 | X | No effect, transmitted crc is a good crc and far end transceiver receives it correctly. This is the default mode after any reset. |
| 1 | 0 | Transmitted crc is continuously corrupted by inverting the crc symbols. This causes the far end transceiver to detect crc errors. BR8(b3) must be returned to a 0 to stop the transmission of bad crcs. |
| 1 | 1 | Transmitted crc is corrupted only until the end of the current U–interface superframe. Then BR8(b3) is cleared to 0. |

## 7.7 MAINTENANCE CHANNEL INTERRUPTS AND UPDATES

This section provides details on when interrupts are generated and when the internal superframe framer reads maintenance channel registers to include their contents in the outgoing transmitted superframe. This information is particularly useful when designing LUNT and LULT line cards for digital loop carrier systems. The basic frames and Quat positions are numbered as in the ANSI T1.601 specification. A Quat is the ANSI T1.601 term for the symbols transmitted over the U–interface. Basic frames are numbered from 1 through 8. The Quats in each basic frame are numbered from 1 through 120.

The M4, M5/M6, and eoc maintenance subchannels can be used for signalling in proprietary applications. When the M4 or M5/M6 subchannels are configured to update on every received frame in the subchannel the update interval is 12 ms or once every superframe. The receive data interrupt for the M5/M6 subchannel occurs at the end of basic frame 4. The receive data interrupt for the M4 channel occurs at the end of the superframe or basic frame 8. See Figures 7–1, 7–2, and 7–3 and the register BR9 description for more details.

When the eoc subchannel is configured to update on every received eoc frame the update interval is 6 ms or twice each superframe. The eoc receive data interrupt can occur at the end of basic frame 4 or at the end of basic frame 8. See the register description for BR9 for more details.

The receive and transmit registers for the maintenance channels are double buffered. Figure 7–2 indicates where maintenance channel registers are updated from the superframe received at the NT. Figure 7–2 also indicates the points where the U–interface transceiver transfers data from the maintenance channel registers into the transmitted superframe when the MC145572 is configured for NT mode. Figure 7–3 indicates where maintenance channel registers are updated from the superframe received at the at the LT end of the loop. Figure 7–3 also indicates the points where the U–interface transceiver transfers data from the maintenance channel registers into the transmitted superframe when the MC145572 is configured for LT mode.

For digital loop carrier applications the maintenance channel registers R6, BR1, and BR3 must be programmed to update on every received frame. Do not use trinal or dual consecutive checking. The reason for this is that intermediate nodes need to do local processing of the eoc messages and must transmit the messages upstream or downstream on a frame by frame basis. See explanations for Byte Register 9. Note that the eoc maintenance subchannel R6 is updated with a new received eoc message twice each superframe. The MC145572 should be configured so that interrupts are generated when BR1, BR3, and R6 are updated. See explanations for Nibble Registers 3 and 4. The interrupt for BR3 (IRQ0) may not need to be enabled since BR3 is updated at the same time as R6 at the end of a superframe. When an interrupt occurs, data can be read from the appropriate maintenance channel register (BR1, BR3 or R6) and transmitted over the digital loop carrier system. At this time the maintenance channel data that has been received from the digital loop carrier system can be written to the registers for the outgoing superframe (BR0, BR2, or R6).

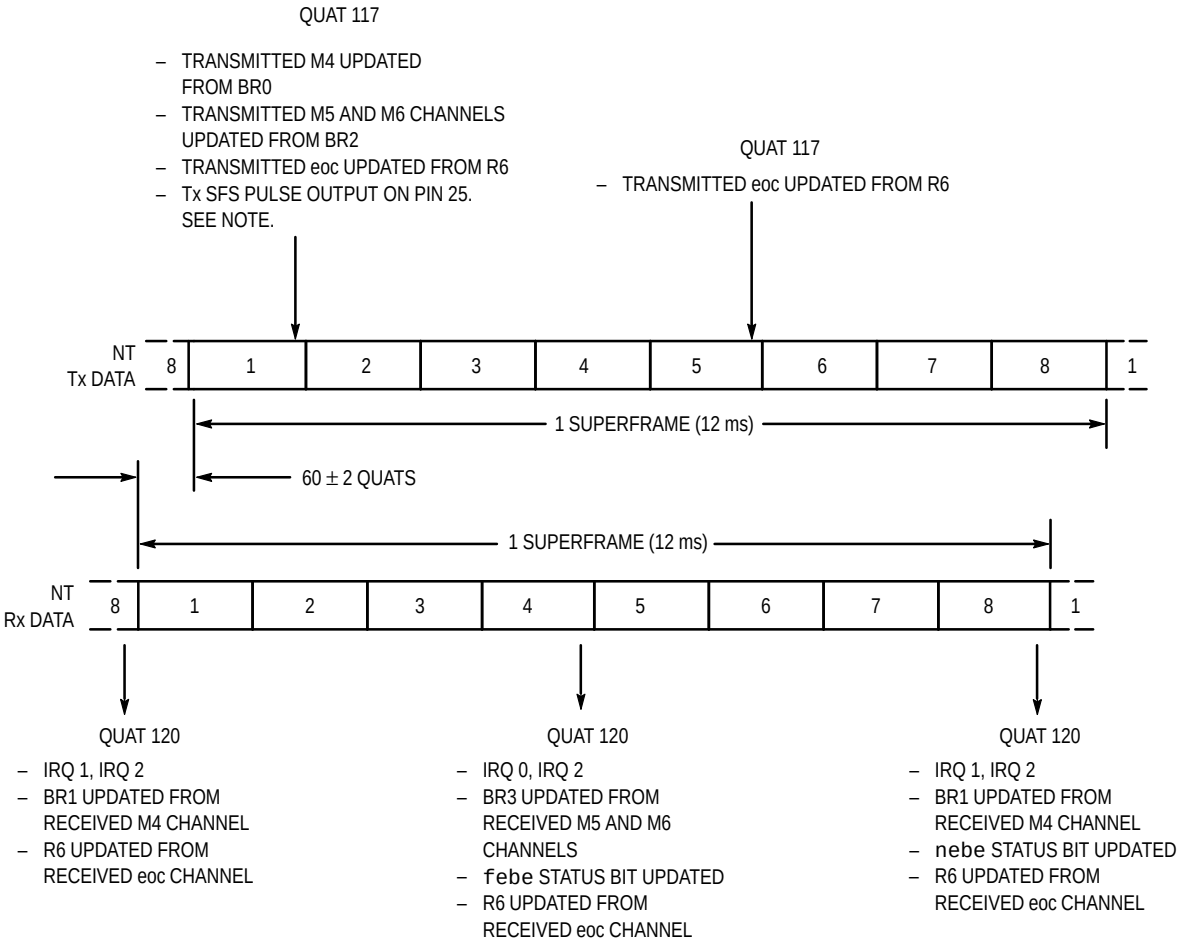
If the M4 channel and eoc interrupts are enabled to occur on the reception of every frame it is possible for the software to determine if the eoc interrupt has occurred at the end of basic frame 4 or at the end of basic frame 8. When the eoc interrupt occurs at the end of basic frame 4 the eoc interrupt status bit, NR3(b2) is set and the M4 channel interrupt status bit, NR3(b1) is clear assuming that the M4 channel register BR1 was read immediately following the previous M4 channel interrupt. When the eoc interrupt and the M4 interrupts occur at the end of basic frame 8 both NR3(b2) and NR3(b1) are set.

The MC145572 does not provide any direct mechanism whereby an external microcontroller can determine when registers for outgoing maintenance data can be updated. This timing must be derived from

the interrupts generated when the receive maintenance subchannel registers are updated. Figures 7–2 and 7–3 show the appropriate timings. It is possible to configure the Tx SFS/SFAX/S0 pin as SFAX and use the pulse to generate a 12 ms periodic interrupt. Note though that SFAX indicates the 2B+D frame in the IDL2 interface that will be transmitted onto the first 2B+D position in basic frame 1 of the U–interface superframe. Due to the internal FIFOs it is not possible to guarantee a fixed time between SFAX and the location of the superframe marker on the U–interface.

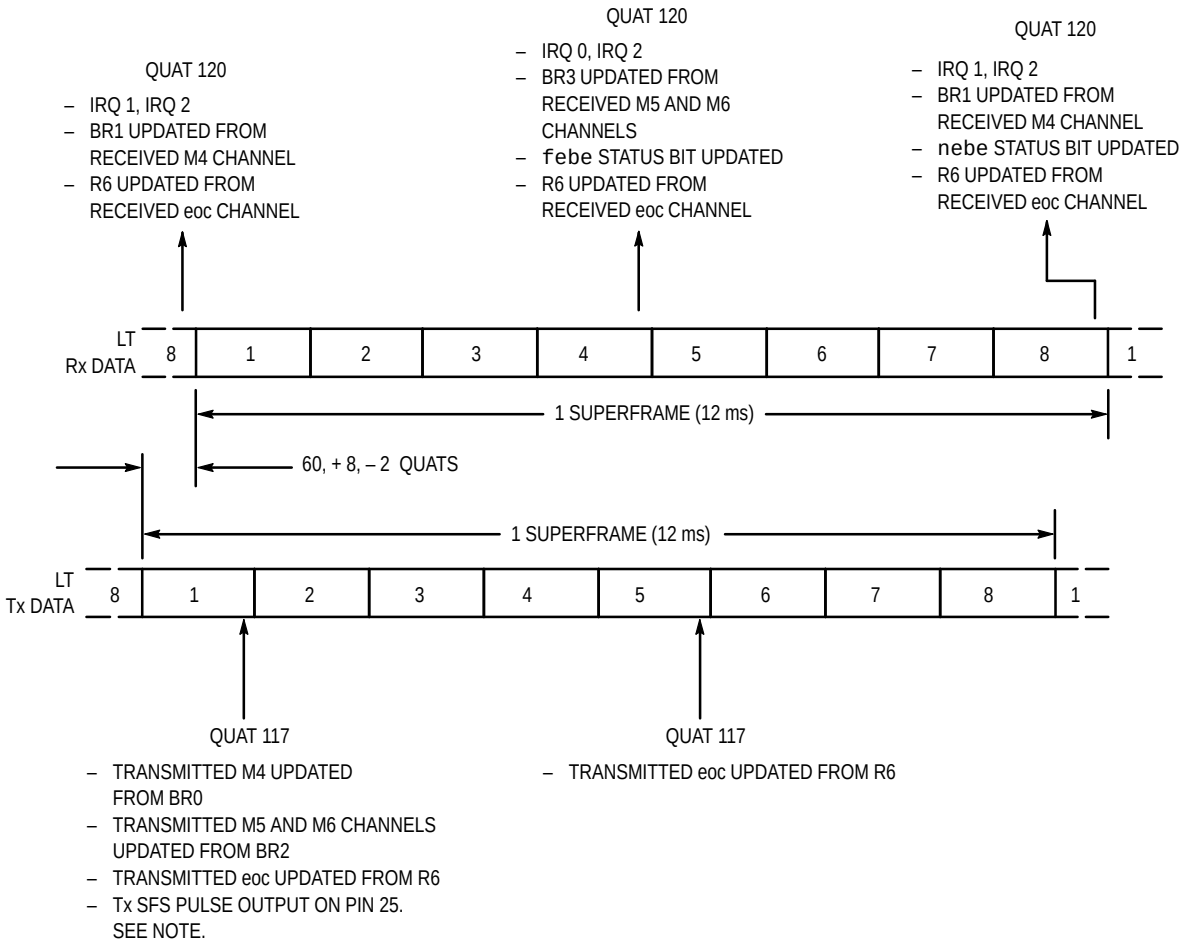
At the NT end the ANSI T1.601 specification requires a turn around delay of 60 ± 2 quats. The MC145572 has a 60 quat turn around time. This means that the transmitted superframe sync word occurs 60 quats later than the received superframe sync word. From an interrupt service routine point of view, updating BR0, BR2, and R6, the worst case time should be assumed to be 60 quats + 117 quats = 177 quats, or 2.2 ms. The system software designer should allow extra margin to be safe. A quat is 12.5 μs in duration.

At the LT end of the loop the received superframe sync word is 60 – 2 + 8 quats later than the transmit superframe sync word. The 2 quat uncertainty comes from the ANSI T1.601 specification for NT turn around time of 60 ± 2 quats on a 0 length loop. The + 8 figure includes worst case propagation delay on an 18,000 foot loop. From an interrupt service routine point of view, the worst case assumption is that the receive superframe sync word occurs 68 quats after the transmitted superframe sync word. For example, from Figure 7–3, the time between when R6 is updated with the receive eoc data and when R6 must be updated with the transmitted eoc data can be calculated as follows: 117 – 68 = 49 quats or 612.5 μs. The system software designer should leave extra margin to be safe.




NOTE: Due to internal delays the actual sync word marker on the TxP and TxN pins occurs 8 quats later than the Tx SFS pulse. See Figure 10–15A.

**Figure 7–2. NT Mode Maintenance Channel Updates**




NOTE: Due to internal delays the actual sync word marker on the TxP and TxN pins occurs 8 quats later than the Tx SFS pulse. See Figure 10–15A.

**Figure 7–3. LT Mode Maintenance Channel Updates**