1
INTRODUCTION

1.1 INTRODUCTION

The MC145572 U–interface transceiver is a single chip device for Integrated Services Digital Network Basic Access Interface that conforms to the American National Standard ANSI T1.601–1992. The device, which can be configured for LT (Line Termination) or NT (Network Termination) applications, performs all necessary Layer 1 functions while utilizing 2B1Q line coding.

The MC145572 is a redesign of the MC145472 and MC14LC5472 U–interface transceivers. The internal signal processing algorithms are the same as for the original MC145472 to maintain its industry–leading performance. The control and time division multiplex interfaces have been significantly enhanced to serve the needs of the growing ISDN marketplace. The use of the latest process technologies permits the MC145572 to be made available in 44–lead PLCC and TQFP packages.

The MC145572 is designed to be easily retrofit into existing MC145472/MC14LC5472 designs with no software changes and few hardware changes. New designs can take advantage of enhanced digital interface features of the MC145572, such as the timeslot assigner and the availability of superframe alignment signals.

The MC145572 can operate in many different modes. The control of these various modes is provided via special purpose pins and the Serial Control Port (SCP) or the Parallel Control Port (PCP). The SCP conforms to the Motorola Serial Control Peripheral Interface standard, an industry standard serial microprocessor interface. The PCP is a standard microprocessor bus port. The designer may choose between using GCI or the Motorola IDL–type time division 2B+D data interface. A timeslot assigner is also provided on the MC145572.

The customer data crossing the U reference point consists of two 64 kbps B channels and one 16 kbps D channel in each direction. Maintenance and framing overhead is also included for a total 160 kbps data (80 Kbaud signaling) rate.

1.2 SUPPLEMENTAL DOCUMENTATION

In addition to descriptions of the ISDN network and basic MC145572 device functionality, this document also contains several appendices:

Appendix A, *MC145572EVK ISDN U–Interface Transceiver Evaluation Kit*, provides a brief overview of the extremely versatile MC145572EVK, which is available to assist with design–in of the MC145572. All developers of MC145572–based products are strongly encouraged to make use of this inexpensive but valuable tool.

Appendix B, *Component Sourcing Information*, lists specifications and potential sources for key external components such as line interface transformers.

Appendix C, *Printed Circuit Board Layout*, provides recommendations for PCB layout.

Appendix D, *Eye Pattern Generator*, details design information to construct an eye pattern generator.

Appendix E, *Coupling Circuit Component Value Calculations*, provides a design example on how to calculate component values for the line interface circuit.

Appendix F, *Applications*, provides an example of how to configure two MC145572 U–Interface Transceivers as a repeater and how to connect MC14LC5540 ADPCM or MC14LC5480 PCM codecs for pair gain applications.

Appendix G, *Performance*, shows graphs of typical line interface circuit performance.

Every effort has been made to make this a complete and easy to use document; however, contact your local sales office or the factory applications staff if you require any further assistance.

Information regarding the generic 2B1Q U–Interface requirement is readily available in standards documents such as ANSI T1.601–1992 and therefore has not been included in this document. The U–Interface equipment designer will find the ANSI document to be a useful reference.

1.3 FEATURES

Key features of the MC145572 U–Interface Transceiver include:

- Single Chip 2B1Q Echo Canceling Adaptively Equalized Transceiver
- Conforms to ANSI T1.601–1992, *Integrated Services Digital Network (ISDN)–Basic Access Interface for Use on Metallic Loops for Application on the Network Side of the NT (Layer 1 Specification)* of the American National Standards Institute.
- Compliant to ETSI ETR 080
- Warm Start Capability
- NT synchronizes to and operates with 80 kHz ± 32 ppm received signal from LT
- Supports Master, Slave, and Slave–Slave Timing Modes
- On–Chip FIFOs for Transmit and Receive Directions
- 2B+D Customer Data Provided by the Industry Standard Interchip Digital Link
- General Circuit Interface (GCI)
- Timeslot Assigner
- Control, Status, and Extended Maintenance Functions Provided through the Serial Control Port (SCP)
- Microprocessor Bus Compatible Parallel Port Available as Pin Selectable Option
- On–Chip Conformance with Activation and Deactivation as Specified in ANSI T1.601
- Automatic Handling of Basic Maintenance Functions
- Automatic Internal Compliance with the Embedded Operations Channel (eoc) Protocol as Specified in the American National Standard
- Complete Set of Loopbacks for Both the IDL and U Reference Point Directions
- Pin Selectable for Line Termination or Network Termination Applications
- On–Chip 2.5 V Transmit Driver Meeting 1992 Requirement
- 8 kHz Reference Frequency in LT Mode
- High Performance CMOS Process Technology
- 5 V Power Supply

1.4 REVISIONS

This revision (MC145572/D, Rev. 2) of the MC145572 data book uses change bars to indicate significant changes or additions to the book with respect to Rev. 1. Several figures and tables have been added to this book. All references below pertain to MC145572/D, Rev. 2.

The list of sections, tables, and figures with changes follows.

Sections:

1.3

1.4

3.3.2 RESET:

3.3.3 D_{in}:

3.3.6 FREQREF: NT Mode

4.3.1 Software Reset

Sections, continued:

4.3.3	Activation Request and Deactivation Request
4.4.7	BR6
4.4.8	IDL2 Speed
4.4.10	Automatic eoc Processor Mode
4.5.8	OR7 Internal Analog Loopback and Line Connect
4.5.10	4096 Disable
5.6.3	Pseudo Code modified
5.6.5	Added section on releasing analog loopback.
8.3.2.3	
9.2.2	
9.2.3	
10.5	
10.6.2	
10.10.4	Item 108
B.3.1	
B.3.2	
B.5	

Figures:

5–13	Changed 100 kΩ to 10 kΩ.
8–6	Monitor Channel Register Write Sequence
8–7	Monitor Channel Register Read Sequence
8–8	Monitor Channel Multiple Interrupt Indications Sequence
8–17	
9–2	
10–4	
10–5	
F–2	Now is a diagram for a two–device NT1.
F–4	ISDN Smart NT1
F–5	ISDN U–ifc to LAN Server

Tables:

4–3	OR7 bit additions
4–5	
4–6	
4–7	
5–3	
5–8	
8–6	
B–2	Peak Winding Current value