8
GCI MODE FUNCTIONAL DESCRIPTION

8.1 FUNCTIONAL OVERVIEW

The MC145572 is configurable for General Circuit Interface or GCI operation. GCI is a time division multiplex bus that combines the ISDN 2B+D data and control/status information onto four signal pins. There are two clocks per data bit and a single frame synchronization pulse, FSC.

In GCI mode the MC145572 supports the full set of commands and indications over the Command/Indicate channel. The monitor channel is used for sending and receiving maintenance channel messages and accessing the internal MC145572 registers.

As a GCI slave the MC145572 accepts clock frequencies between 512 kHz and 8.192 MHz. As a GCI master the MC145572 operates at either 512 kHz or 2.048 MHz. Figure 8–1 is a typical configuration for the MC145572 in GCI mode. The MC145572 is configured for GCI operation when the MCU/GCI pin is tied low. The PAR/SER pin is a don't care but must be tied either high or low.

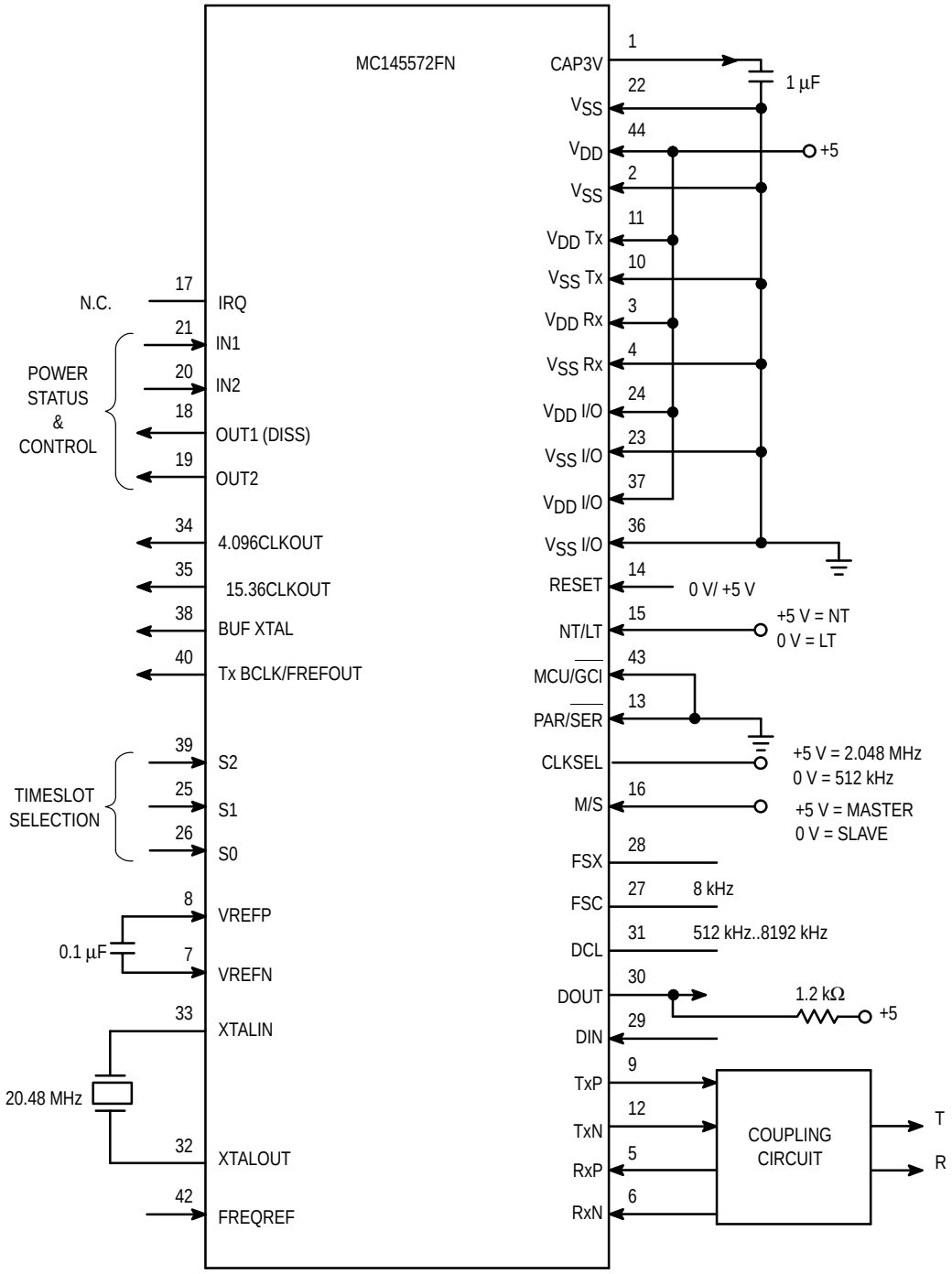


Figure 8–1. MC145572 Configuration for GCI Operation

Table 8–1. GCI Master Mode Clock Rate Selection

Clock Rate	CLKSEL
512 kHz	0
2.048 MHz	1

8.2 INTERFACE SIGNALS

Seven signal pins are available for the time division multiplex bus interface in GCI mode. They are:

S2, S1, S0; Used to select the active GCI channel in multiplexed GCI frames.

DCL; 2x data clock

FSC; The 8 kHz frame synchronization pulse.

DIN; The MC145572 reads data from the GCI interface into this pin during the active GCI channel selected by S2, S1, S0.

DOUT; In GCI mode this pin is an open drain output and must be pulled to V_{DD} through a resistor. The MC145572 outputs data to the GCI interface from this pin during the active GCI channel selected by S2, S1, S0.

During all other GCI channels, if present, DOUT is off. DIN accepts data during the channel selected by S0, S1 and S2. During other GCI channels, if present, DIN ignores any data that is present.

8.3 GCI FRAME STRUCTURE

The GCI interface supports two types of frame formats. These are the single GCI channel and the multiplexed GCI channel formats. A single GCI channel has the following subchannels: two B channels, a Monitor channel, the ISDN D channel, the Command/Indicate channel and the A and E bits. See Figure 8–2.

Referring to Figure 8–2 the two B channels are used to convey customer data between the MC145572 and other GCI devices. The Monitor channel bits are used to convey register and maintenance information between the MC145572 and other GCI devices. The D bits carry the ISDN basic access D channel. The Command/Indicate, (C/I), bits are used for activation and deactivation of the MC145572 and for control functions. The A and E bits are used as handshake signals during the transfer of monitor channel messages.

A multiplexed GCI frame contains from two to eight GCI frames in each 125 μs period. Table 8–2 summarizes the number of GCI frames that can be multiplexed into a 125 μs period. Figure 8–3 shows how multiple GCI frames are multiplexed into a 125 μs period.

Table 8–2. Multiplexed GCI Frame Configuration

Mode	Clock	Maximum GCI Frames in Multiplex
GCI Master	512 kHz	1
GCI Master	2.048 MHz	4
GCI Slave	512 kHz	1
GCI Slave	4.096 MHz	8

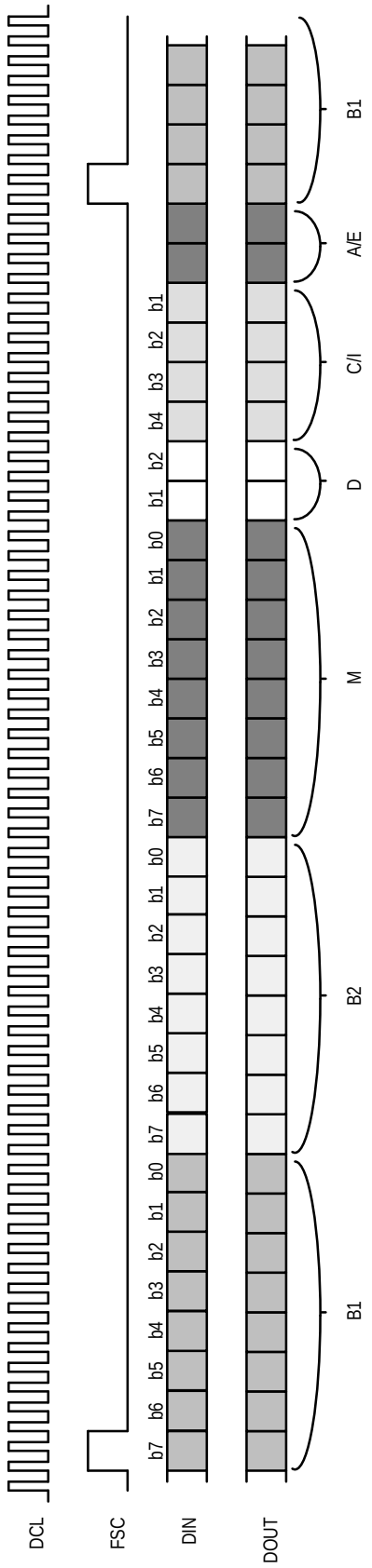


Figure 8–2. Single Channel GCI Format

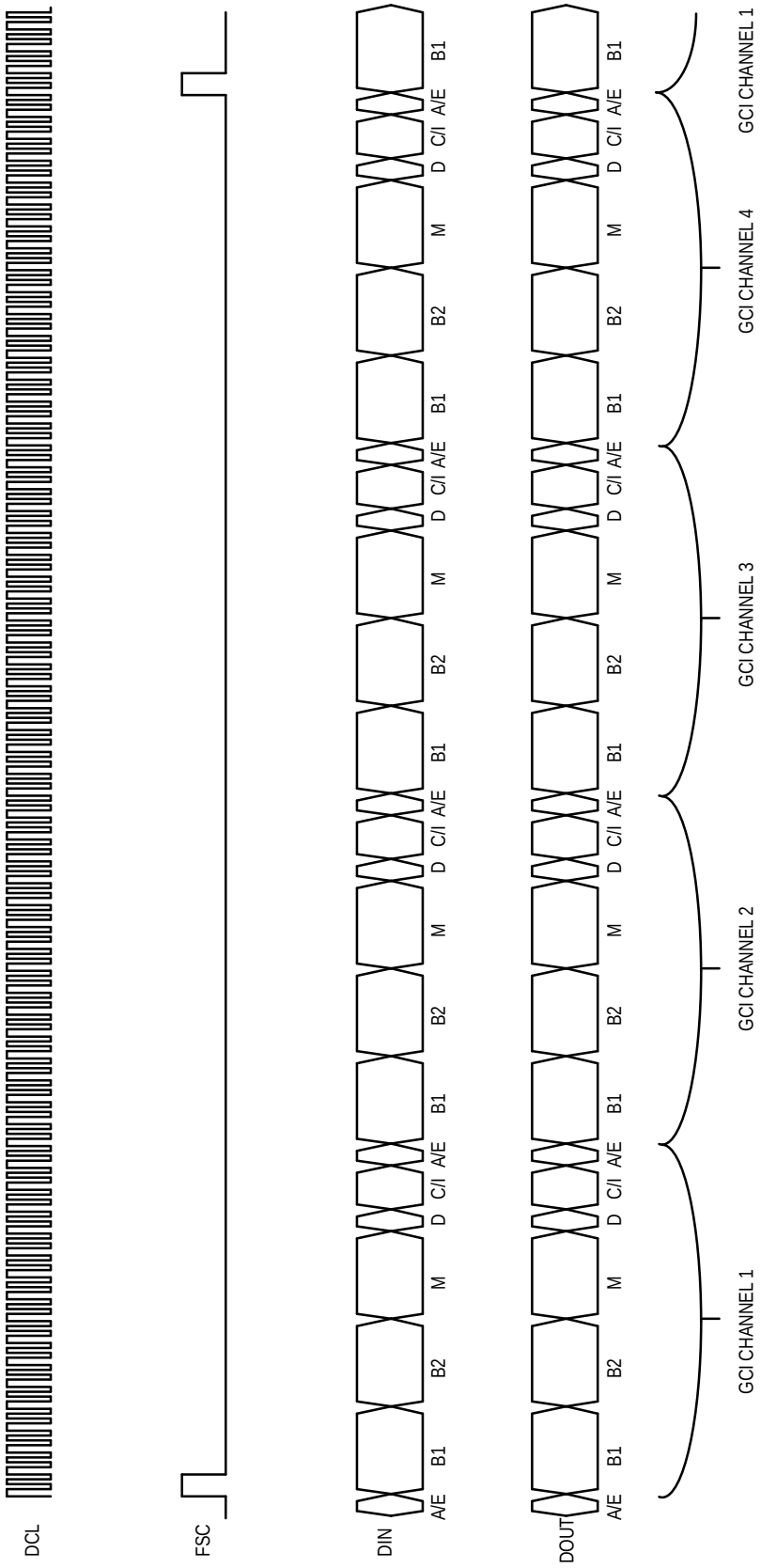


Figure 8–3. Multiplexed GCI Format Example

8.3.1 Monitor Channel Operation

The Monitor Channel is used to access the internal registers of the MC145572 in order to support U–interface maintenance channel operations. All Monitor Channel messages are two bytes in length. Each byte is sent twice to permit the receiving GCI device to verify data integrity. In ISDN applications the monitor channel is used for access to the U–interface maintenance messages.

The A and E bits in the GCI channel are used to control and acknowledge monitor channel transfers between the MC145572 and another GCI device. When the Monitor channel is inactive the A and the E bit times from DOUT are both high impedance. The A and E bits are active when they are driven to V_{SS} during their respective bit times. Pull-up resistors are required on DIN and DOUT. The E bit indicates the transmission of a new monitor channel byte. The A bit from the opposite direction is used to acknowledge the monitor channel byte transfer.

An idle Monitor Channel is indicated by both A and E bits being inactive for two GCI frames. The A and E bits are high impedance when inactive. The monitor channel data is $FF.

The originating GCI device transmits a byte onto the Monitor Channel after receiving the A and E bits equal to 1 for at least two consecutive GCI frames. The originating GCI device also sets its outgoing E bit to 0 in the same GCI frame as the byte that is transmitted. The transmitted byte is repeated for at least two GCI frames or is repeated in subsequent GCI frames until the MC145572 acknowledges receiving two consecutive GCI frames containing the same byte.

Once the MC145572 acknowledges the first byte the sending device sets E to high impedance and transmits the first frame of the second byte. Then the second byte is repeated with the E bit low until it is acknowledged. See Figures 8–4, 8–5, 8–6, and 8–7 for details of Monitor Channel procedure.

The destination GCI device verifies that it has received the first byte by setting the A bit to 0 towards the originating GCI device for at least two GCI frames. Successive bytes are acknowledged by the receiving device setting A to high impedance on the first instance of the next byte followed by A being cleared to 0 when the second instance of the byte is received.

The entire register set of the MC145572 can be accessed via the Monitor Channel. All M4 channel activity is automatically handled by the MC145572 when configured for GCI mode. The MC145572 issues Monitor Channel messages whenever the received eoc, M4 or M5/M6 messages received from the U–interface change, and appropriate dual–checking or trinal–checking of bits has been done. In normal GCI operation it is not necessary to read or write the internal registers of the MC145572.

If the receiving GCI device does not receive the same Monitor Channel byte in two consecutive GCI frames it indicates this by leaving A=0 until two consecutive identical bytes are received. The last byte of the sequence is indicated by the originating GCI device setting its E bit to 1 for two successive GCI frames. Figure 8–5 shows an example of an delayed GCI Monitor Channel message.

8.3.2 Monitor Channel Messages and Commands

The MC145572 supports three basic types of Monitor Channel Messages. The first group of messages are commands that read or write the internal register set of the MC145572. See Section 4 for a complete description of the MC145572 register set. The second group of messages are responses from the MC145572. These responses are transmitted by the MC145572 after it receives a register read or write command over the monitor channel. The third group of Monitor channel messages are Interrupt Indication Messages. These are transmitted by the MC145572 whenever a change is detected in the maintenance channel receive registers BR1, BR3 or R6.

8.3.2.1 Monitor Channel Commands

A GCI device transmits Monitor Channel commands to a receiving MC145572 to gain access its internal register set. The receiving MC145572 then transmits a Monitor Channel Response Message onto the monitor channel for commands that request data to be read from an internal register. Commands that write data to an internal MC145572 register are accepted and acted upon but the MC145572 does not issue a response message. The monitor channel commands are given in Table 8–3.

The MC145572 acknowledges all messages it receives over the Monitor channel. If an invalid message is received the MC145572 acknowledges it but does not take any action.

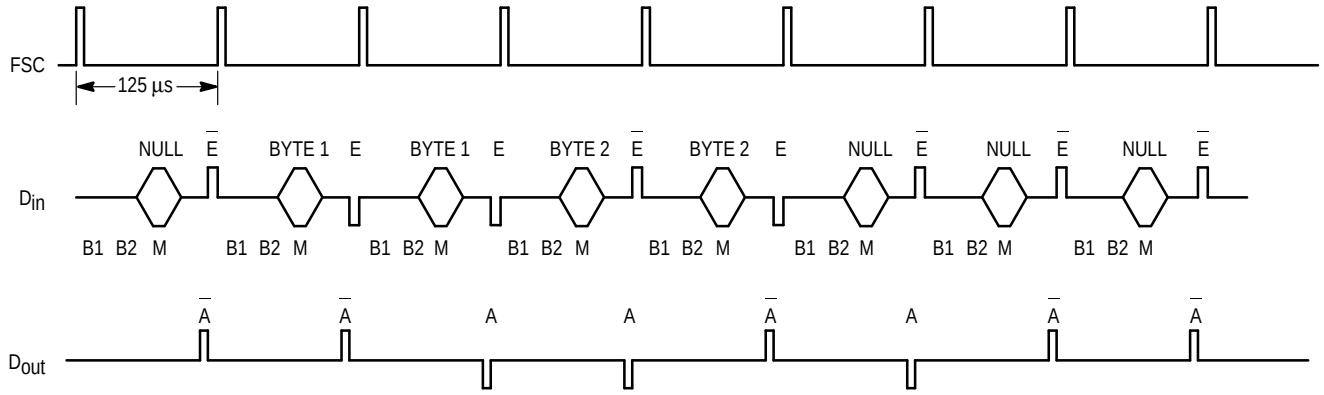


Figure 8–4. Monitor Channel Access Protocol

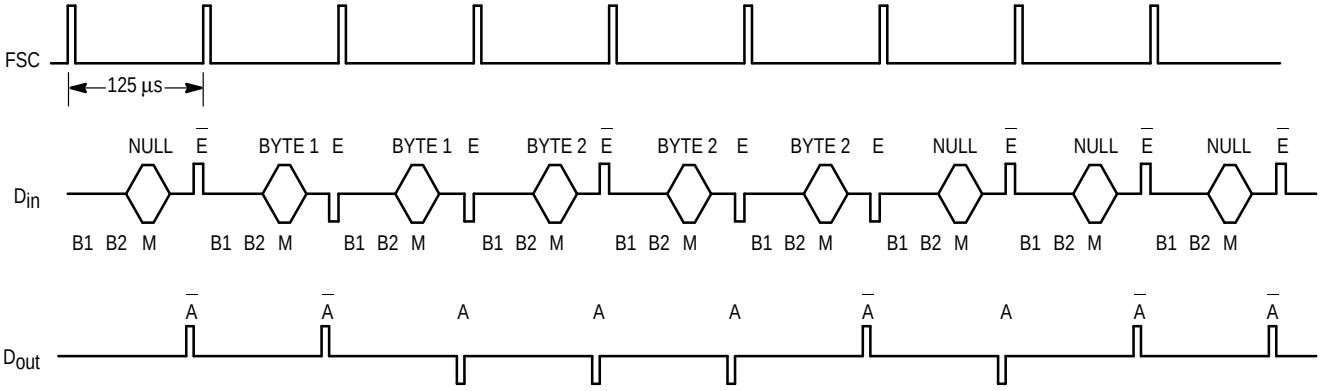


Figure 8–5. Monitor Channel Protocol with Delay

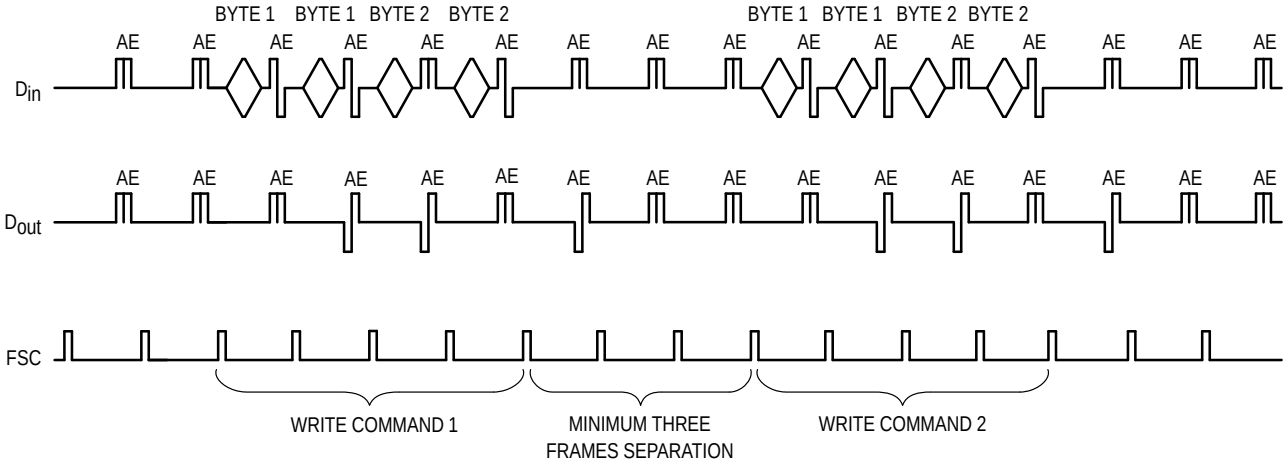


Figure 8–6. Monitor Channel Register Write Sequence

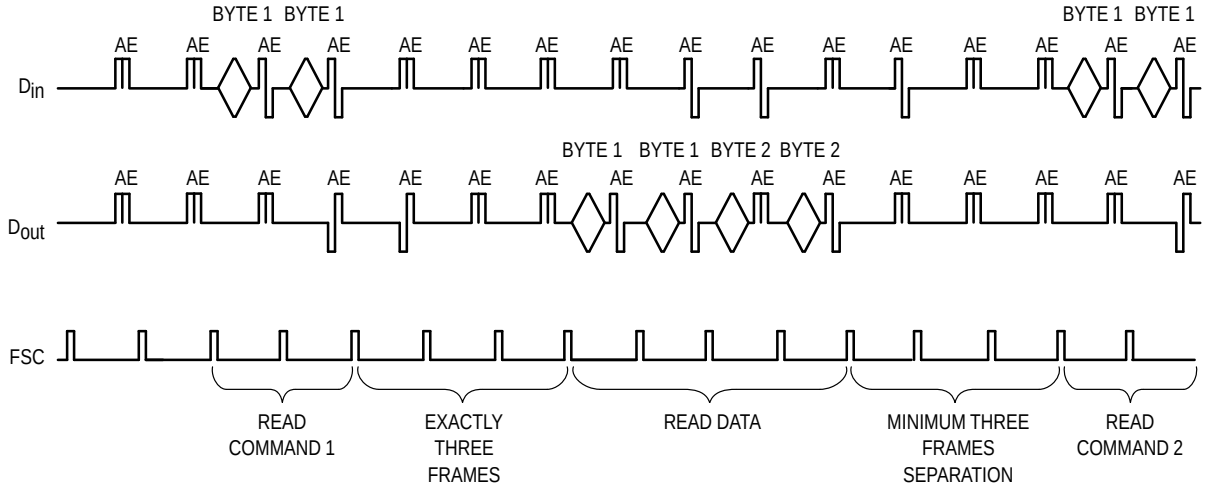


Figure 8–7. Monitor Channel Register Read Sequence

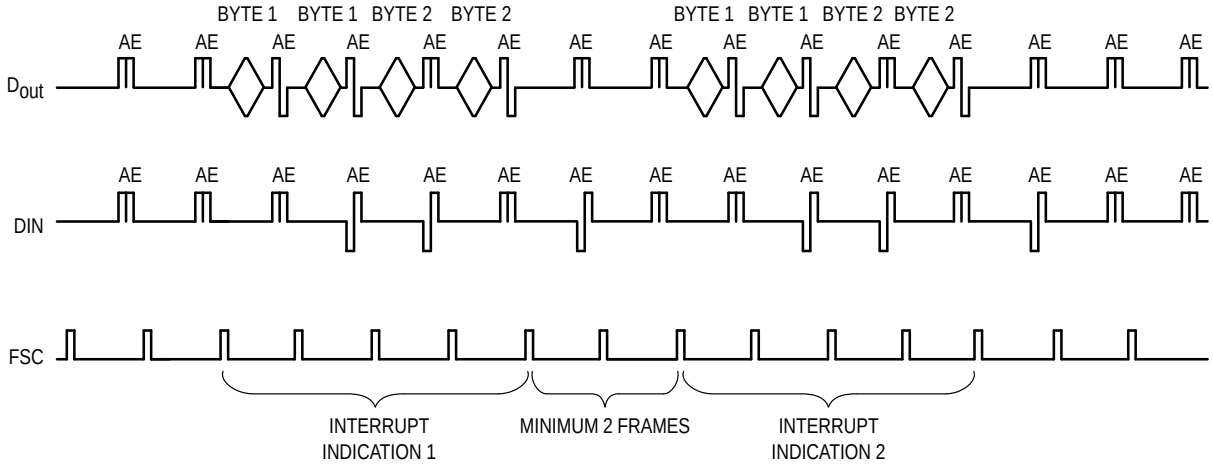


Figure 8–8. Monitor Channel Multiple Interrupt Indications Sequence

Table 8–3. Monitor Channel Commands

Byte 1								Byte 2								
msb							**lsb**	**msb**							**lsb**	
b17	**b16**	**b15**	**b14**	**b13**	**b12**	**b11**	**b10**	**b27**	**b26**	**b25**	**b24**	**b23**	**b22**	**b21**	**b20**	
0	0	0	0	ba3	ba2	ba1	ba0	d7	d6	d5	d4	d3	d2	d1	d0	Byte Write
0	0	0	1	ba3	ba2	ba1	ba0									Byte Read
0	0	1	0	na3	na2	na1	na0	d3	d2	d1	d0	x	x	x	x	Nibble Write
0	0	1	1	na3	na2	na1	na0									Nibble Read
0	1	0	1	0	0	0	0									eoc Read
0	1	1	0	a1	a2	a3	dm	i1	i1	i3	i4	i5	i6	i7	i8	eoc Write
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Device Identification

NOTES:

1. For byte register accesses the address range of ba3, ba2, ba1, ba0 is hexadecimal 0 – F. The bits d7 through d0 are data that is written to the byte register.
2. For nibble register accesses the address range of na3, na2, na1, na0 is hexadecimal 0 – 5. The bits d3 through d0 are data that is written to a nibble register.
3. The bits a1 through a3, dm and i1 through i8 are data that is written to the eoc register.
4. For non ISDN applications the data written to the eoc register uses the convention that bit a1 is the most significant bit and bit i8 is the least significant bit.
5. The receiving device does not issue a response to a register write command.
6. Byte or nibble read commands consist of byte 1 only. Byte 2 is not transmitted to the MC145572. In response to a read command, the MC145572 responds with two bytes as indicated in Table 8–4. See Figure 8–7.

8.3.2.2 Monitor Channel Response Messages

The monitor channel response messages are transmitted onto the GCI monitor channel by the MC145572 in response to a register read command. The monitor channel response messages are given in Table 8–4.

Table 8–4. Monitor Channel Response Messages

b17	b16	b15	b14	b13	b12	b11	b10	b27	b26	b25	b24	b23	b22	b21	b20	
0	0	0	1	ba3	ba2	ba1	ba0	d7	d6	d5	d4	d3	d2	d1	d0	Byte Read
0	0	1	1	na3	na2	na1	na0	d3	d2	d1	d0	x	x	x	x	Nibble Read
0	1	0	1	a1	a2	a3	dm	i1	i1	i3	i4	i5	i6	i7	i8	eoc Read
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Device Identification

NOTES:
1. If a maintenance channel is updated in the MC145572 receive deframer at the same time a register read command is received then an interrupt indication message is issued first. The indication message takes priority over requests for register reads. All queued interrupt indication messages are issued before the response to the register read message. It is important for software to always check the message code in byte 1 of any received message.
2. The bits a1 through a3, dm and i1 through i8 are data that is read from the eoc register. The bits d7 through d0 are data that is read from a register.
3. For non ISDN applications the data written to the eoc register uses the convention that bit a1 is the most significant bit and bit i8 is the least significant bit.

8.3.2.3 Monitor Channel Interrupt Indication Messages

The Monitor channel interrupt indication messages are **automatically** transmitted onto the GCI monitor channel by the MC145572 when its receiver deframer updates one of the maintenance channel registers BR1, BR3 or the eoc register R6. The maintenance channel registers are updated when the trinal checking of bits or messages has been completed. All outstanding interrupt indication messages are transmitted prior to any response messages being transmitted. The Monitor Channel Interrupt Indication messages are given in Table 8–5.

Table 8–5. Monitor Channel Interrupt Indication Messages

b17	b16	b15	b14	b13	b12	b11	b10	b27	b26	b25	b24	b23	b22	b21	b20	
0	0	0	0	0	0	0	0	d7	d6	d5	d4	d3	d2	d1	d0	M5/M6 int.
0	0	1	0	0	0	0	0	d7	d6	d5	d4	d3	d2	d1	d0	M4 int.
0	1	0	0	a1	a2	a3	dm	i1	i1	i3	i4	i5	i6	i7	i8	eoc int.

NOTES:
1. The bits a1 through a3, dm and i1 through i8 are data that is read from the eoc register R6.
2. For non ISDN applications the data read from the eoc register uses the convention that bit a1 is the most significant bit and bit i8 is the least significant bit.
3. The data byte returned by the M5/M6 interrupt corresponds to the byte as read from Byte Register BR3 in the SCP interface mode register map. The bits d7 through d0 are data that is read from a register.
4. The data byte returned by the M4 interrupt corresponds to the byte as read from Byte Register BR1 in the SCP interface mode register map.

8.3.3 Command/Indicate Channel Operation

The Command/Indicate or C/I channel is used to activate and deactivate the MC145572. Some control functions such as loopbacks are also supported over the C/I channel. C/I codes are four bits in length and must be received for two consecutive GCI frames before they are acted upon.

C/I channel bits are numbered bit four through one with bit four being the most significant bit. The C/I/ channel bits are transmitted starting with bit four.

C/I channel commands are used to activate, or deactivate the MC145572. They are also used to implement loopbacks and perform control functions. Some C/I channel commands may cause the MC145572 to issue a C/I channel response. Table 8–5 summarizes the C/I channel commands and indications.

C/I channel indications are used to notify a layer two device that certain events have occured such as a change in activation status.

In normal GCI operation the M4 channel `act`, `dea`, `uoa`, `sai`, `ps1`, `ps2` and reserved status bits are handled automatically. It is possible to set bits in the MC145572 register map using monitor channel commands that will over ride the automatic operation of the M4 channel.

Table 8–6. C/I Channel Commands and Indications

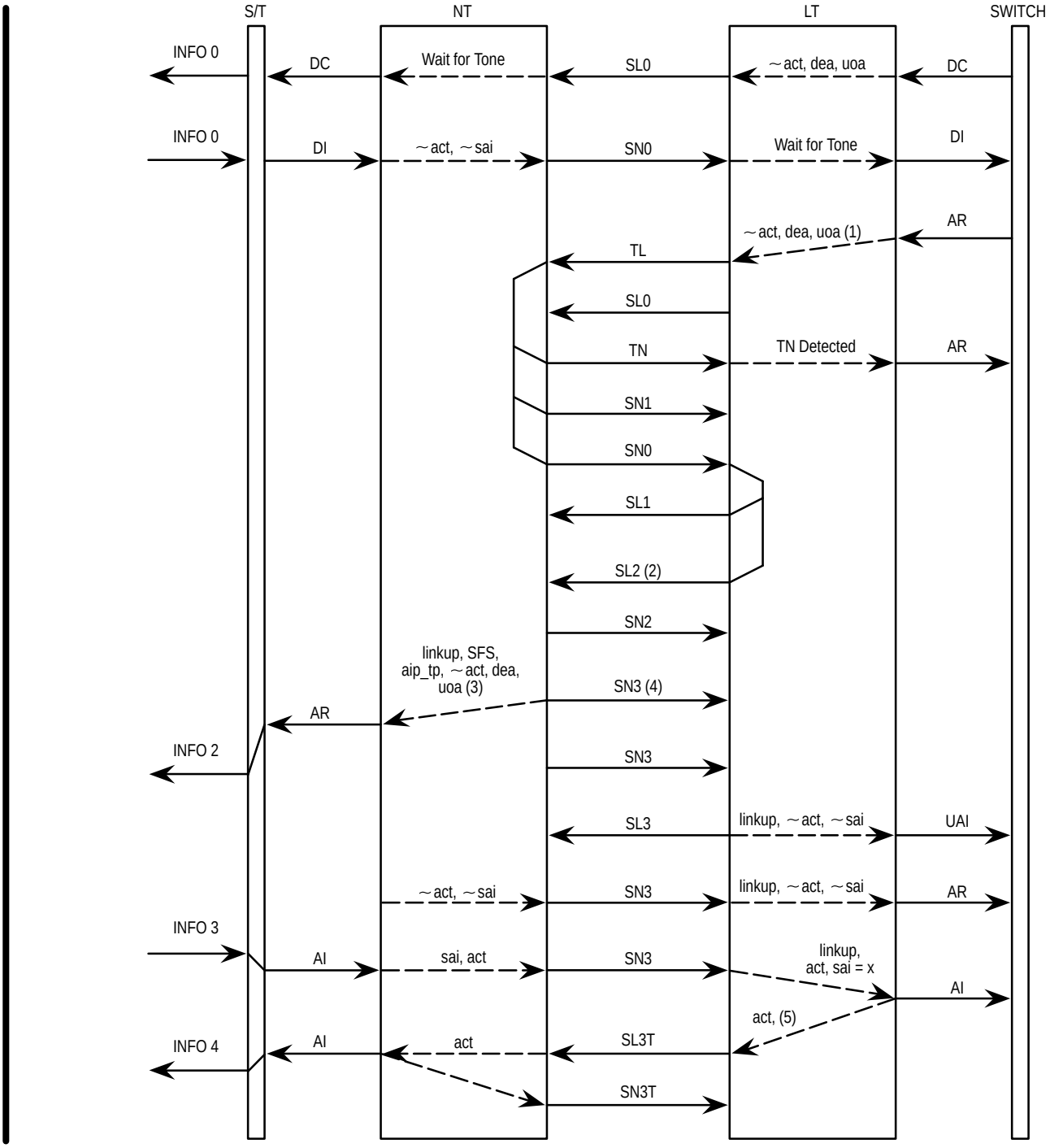
C/I Codeword				LT Mode	LT Mode	NT Mode	NT Mode
b4	b3	b2	b1	Command	Indication	Command	Indication
0	**0**	0	0	**DR**	**–**	**–**	**DR**
0	**0**	0	1	**RES**	**DEAC**	**RES**	**–**
0	**0**	1	0	**LTD2**	**–**	**NTD2**	**–**
0	**0**	1	1	**LTD1**	**–**	**NTD1**	**–**
0	**1**	**0**	**0**	**–**	**RSY**	**–**	**RSY**
0	**1**	**0**	**1**	**–**	**EI2**	**–**	**EI2**
0	**1**	**1**	**0**	**–**	**–**	**–**	**–**
0	**1**	**1**	**1**	**UAR**	**UAI**	**–**	**–**
1	**0**	0	0	**AR**	**AR**	**AR**	**AR**
1	**0**	0	1	**–**	**–**	**–**	**–**
1	**0**	1	0	**ARL**	**–**	**ARL**	**–**
1	**0**	1	1	**–**	**–**	**–**	**–**
1	**1**	**0**	**0**	**–**	**AI**	**AI**	**AI**
1	**1**	**0**	**1**	**–**	**–**	**–**	**–**
1	**1**	**1**	**0**	**–**	**–**	**–**	**AIL**
1	**1**	**1**	**1**	**DC**	**DI**	**DI**	**DC**

NOTES:

AI	Activation indication	AR	Activation request
AIL	2B+D loopback received over eoc channel. Perform loopback at S/T interface in 2–chip NT1.	DC	Deactivation confirm
		DI	Deactivation indication
ARL	Activation request with local analog loopback	EI2	Error indication
DEAC	Deactivation request accepted	LTD2	(LT mode), NTD2 (NT mode) Set pin “OUT2” high when command is active.
DR	Deactivation request		
LTD1	(LT mode), NTD1 (NT mode) Sets pin “OUT1” high when command is active.	RSY	Loss of sync – resync. requested
		UAR	U–Only activation request
RES	Reset		
UAI	U–Only activation indication		

8.4 GCI ACTIVATION AND DEACTIVATION TIME DIAGRAMS

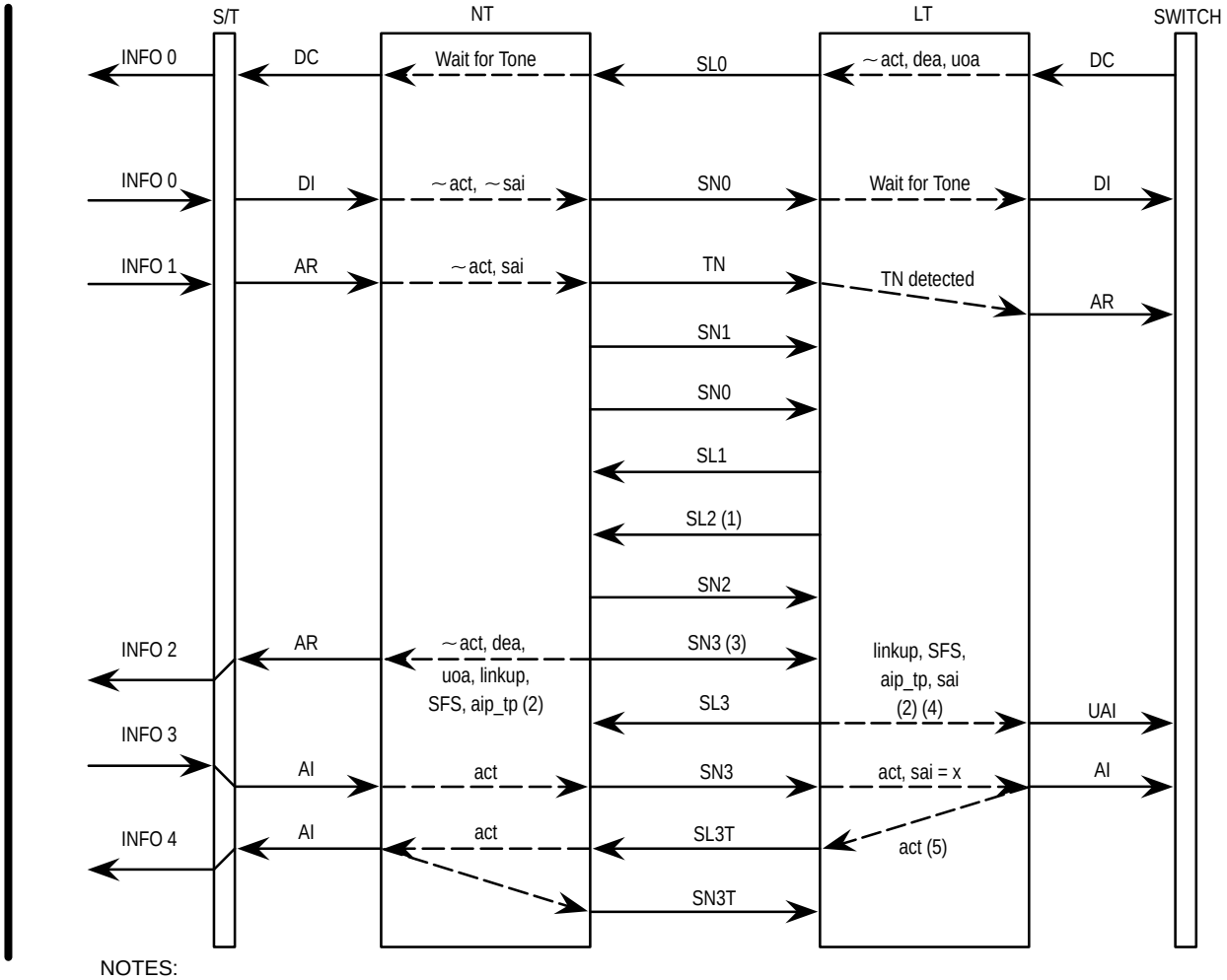
This section contains the time flow diagrams that detail the various activation and deactivation scenarios for the MC145572 U–interface transceiver. Figures 8–9 through 8–15 are the activation diagrams for the MC145572 operating in GCI mode. Figures 8–16 and 8–17 are the activation state diagrams for LT and NT mode operation.



NOTES:

1. No change in transmitted maintenance bits at this time.
2. Maintenance bits are sent with meaningful data (‘Normal’ field in Table 5, T1E1.4).
3. linkup, SFS, aip_tp correspond to NR1 bits 3, 1, and 0 respectively.
4. No change in upstream maintenance bits; act = 0, sai = 0.
5. The downstream act bit is set by issuance of the AI indication.

Figure 8–9. Time Diagram for Total Activation Initiated by the Network



NOTES:

1. Maintenance bits are sent with meaningful data (‘Normal’ field in Table 5, T1E1.4).
2. linkup, SFS, aip_tp correspond to NR1 bits 3, 1, and 0 respectively.
3. No change in upstream maintenance bits; act = 0, sai = 0.
4. Because the upstream sai bit was set by the (upstream) AR command, the indication UAI will never be issued, and AR continues to appear on the C/I channel.
5. The downstream act bit is set by issuance of the AI indication.

Figure 8–10. Time Diagram for Total Activation Initiated by the Terminal Equipment

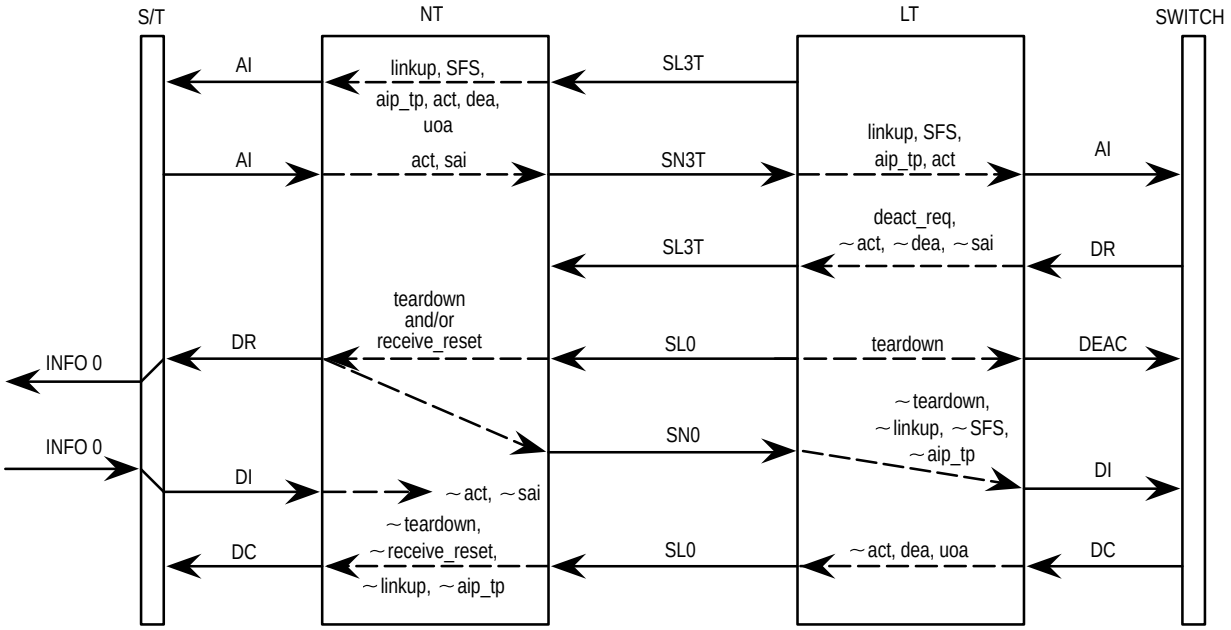


Figure 8–11. Time Diagram for Deactivation (Always Initiated by the Network)

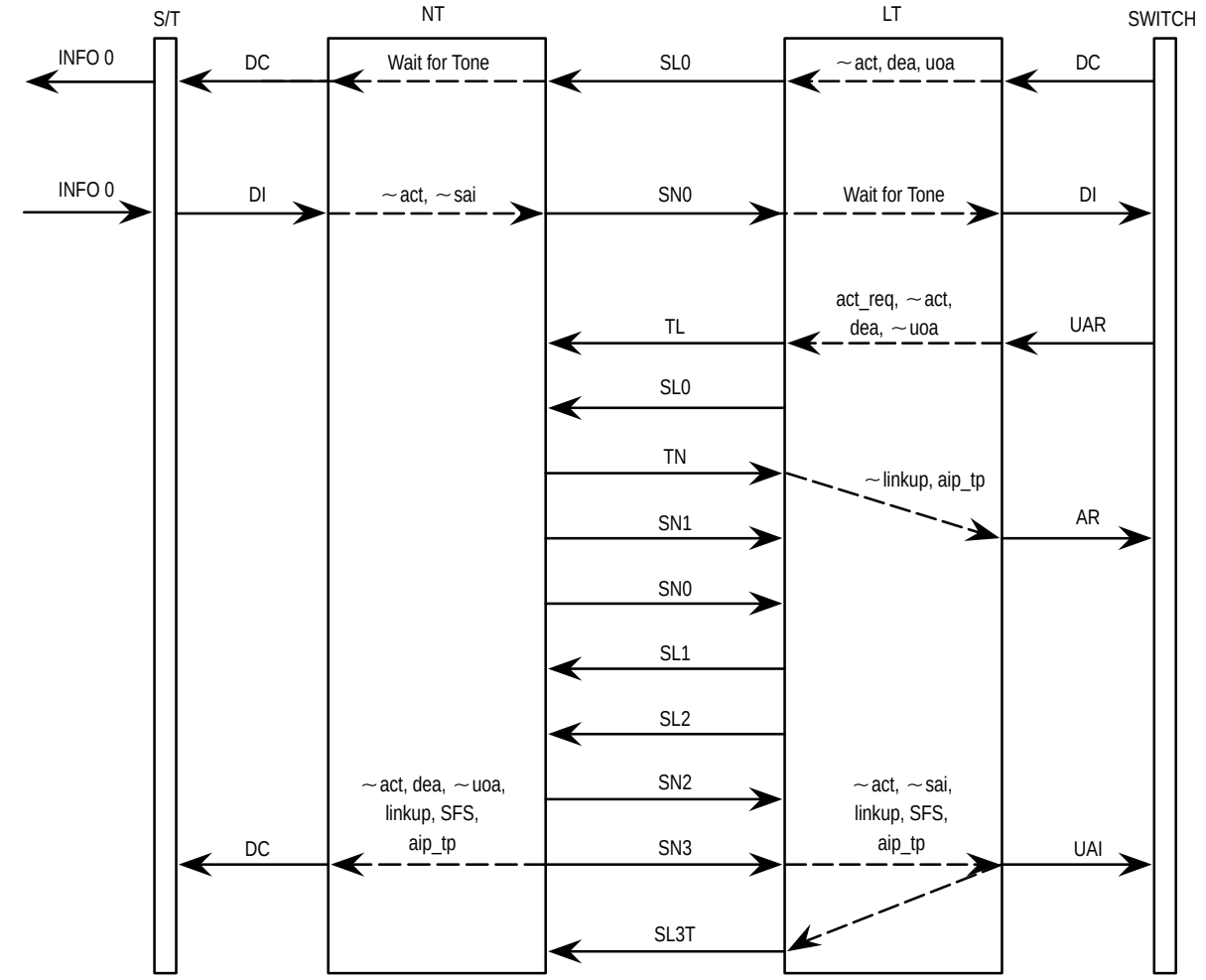


Figure 8–12. Time Diagram of a U–Only Activation (Always Initiated by the Network)

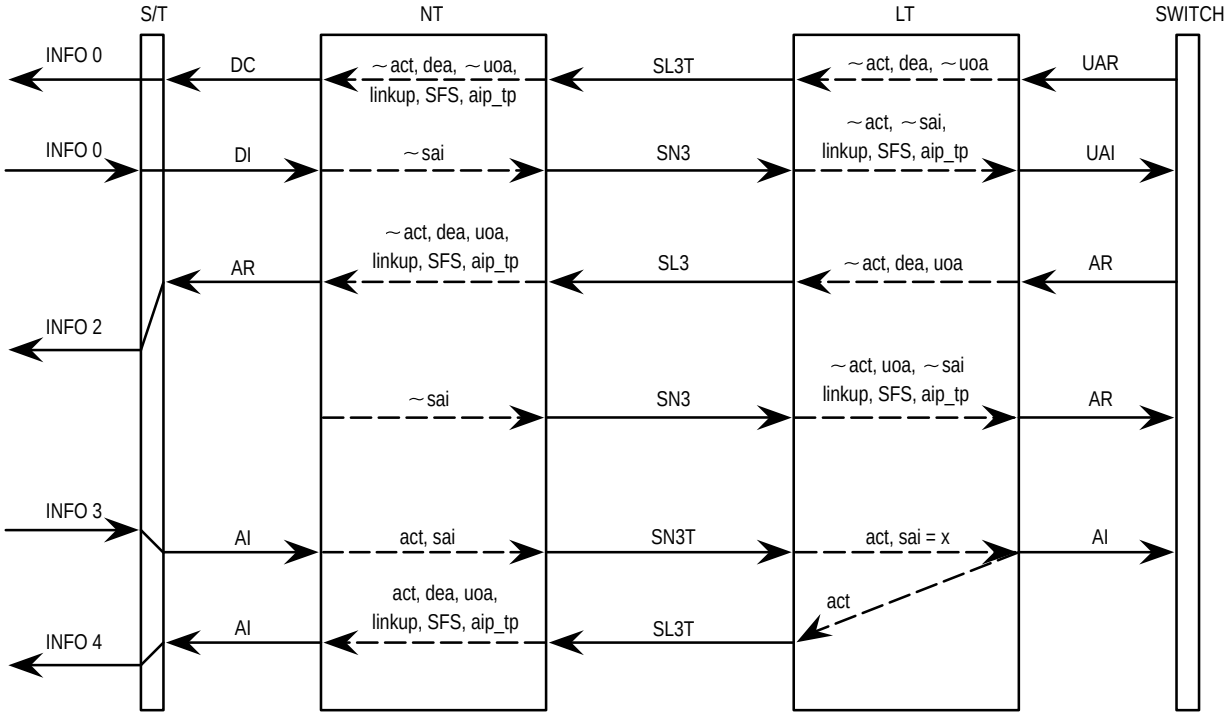


Figure 8–13. Time Diagram for a Transition from DSL–Only Activation to Total Activation Initiated by the Network

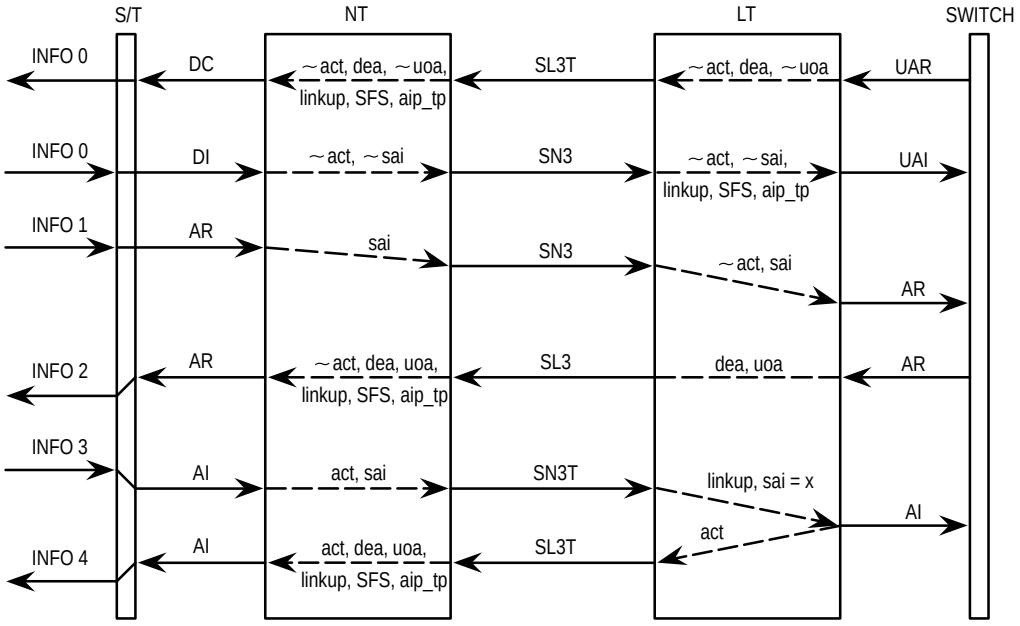
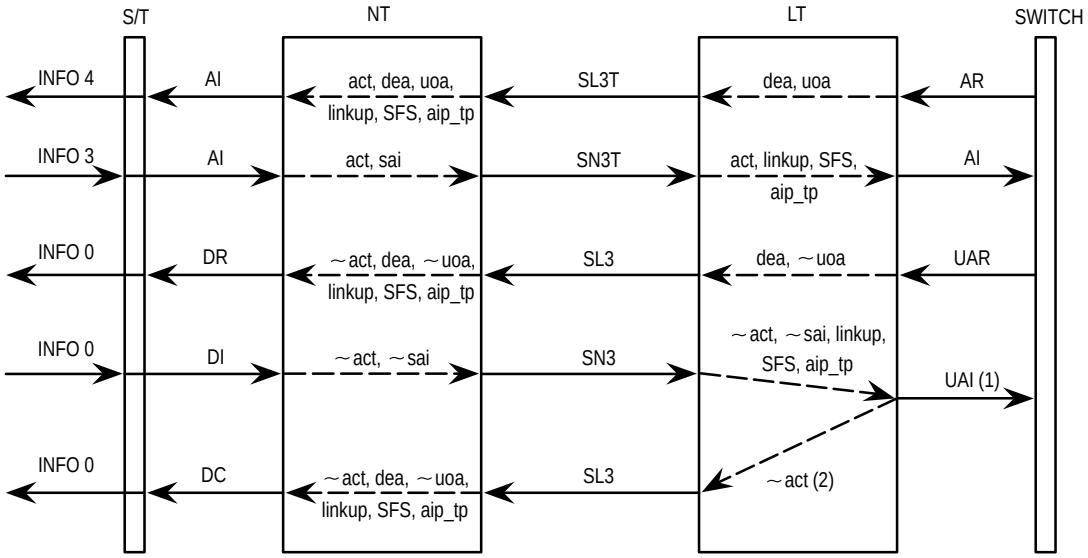


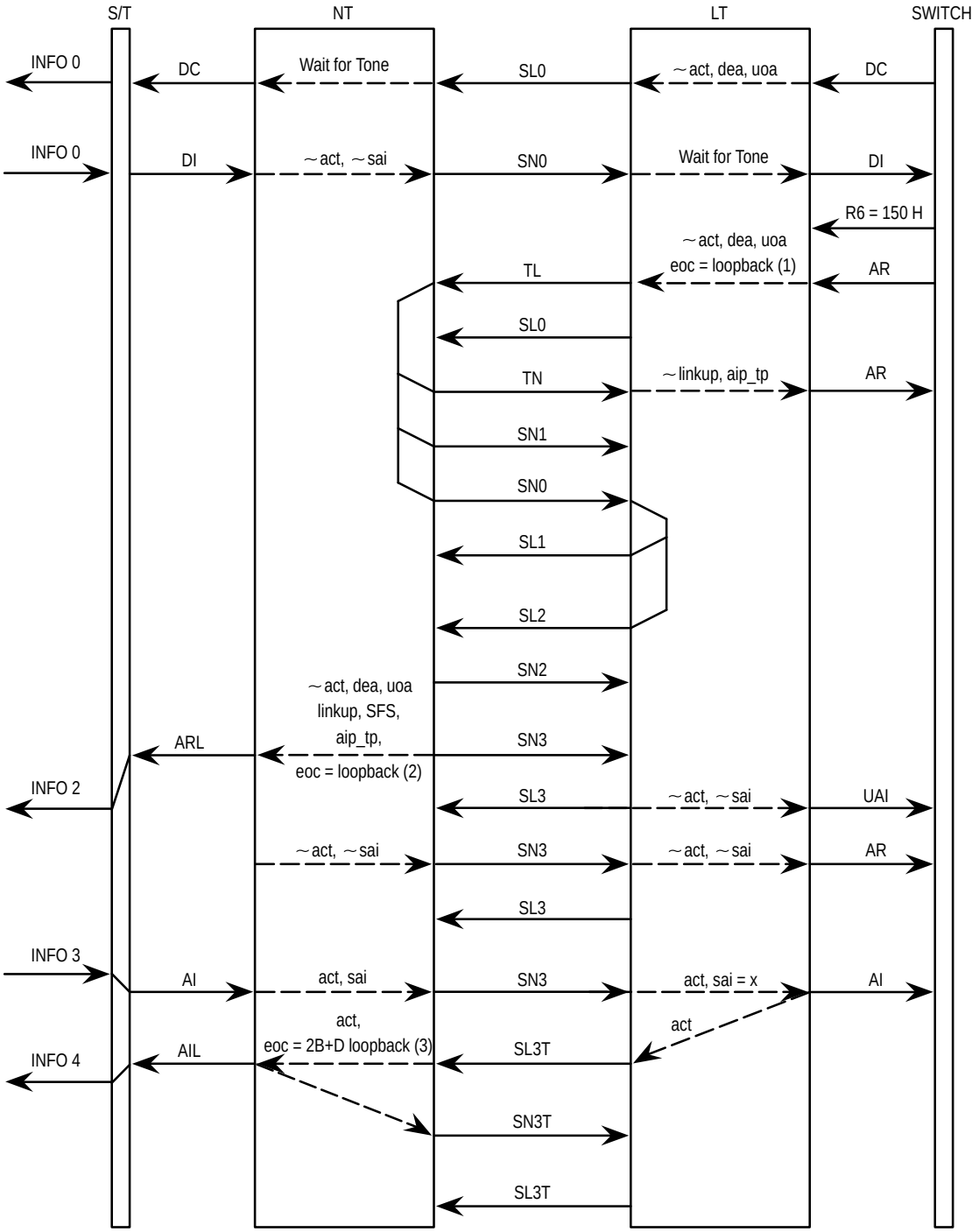
Figure 8–14. Time Diagram for a Transition from DSL–Only Activation to Total Activation Initiated by the Terminal Equipment



NOTES:

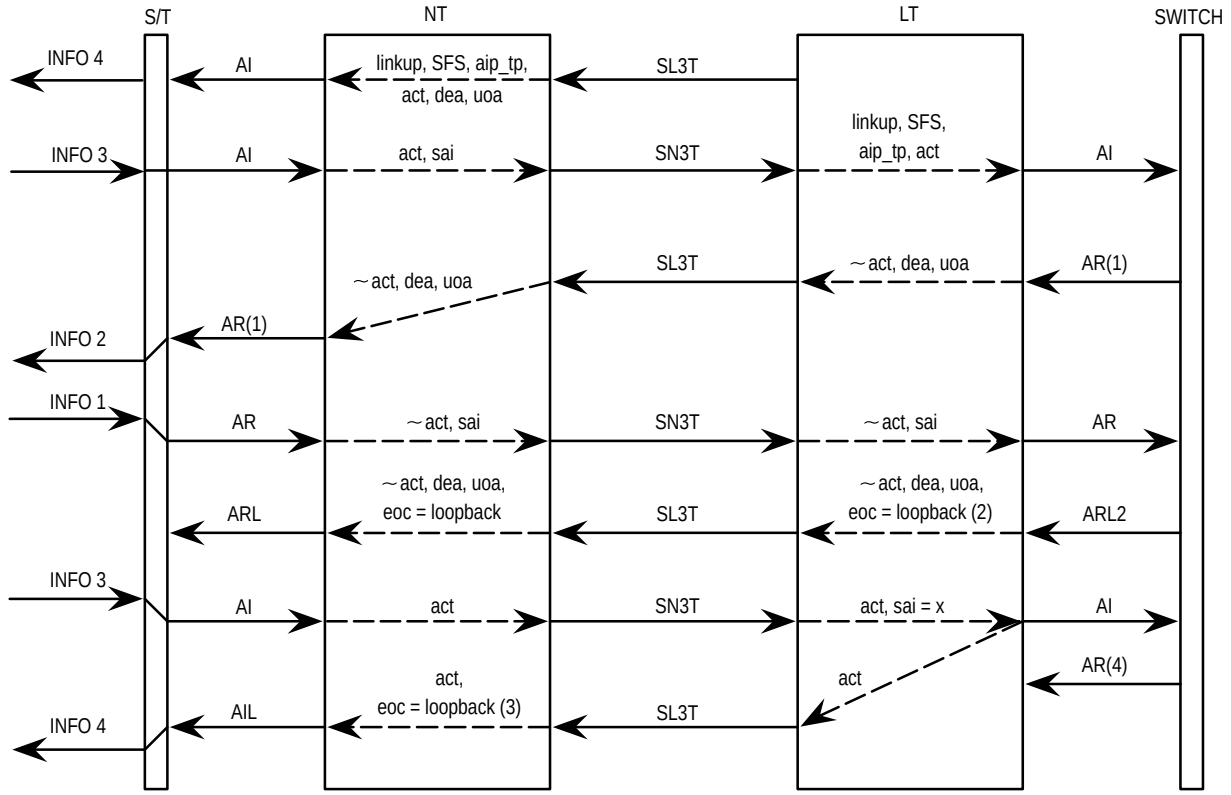
1. In the event that received act = 0 and sai = 0 do not occur at the same time in the LT, it is possible that prior to the UAI indication, AR will be issued by the LT, until the moment in which both maintenance bits are zero in the LT. Then, UAI will be issued, as shown.
2. The state of the act bit is automatically reset by the MC145572, without the need to issue a special command to do this.

Figure 8–15. Time Diagram for a Transition from Total Activation to DSL–Only Activation (Always Initiated by the Network)



NOTES:
1. Monitor channel is used to write eoc 2B+D loopback command to R6 prior to activation.
2. In NT mode the MC145572 may detect the trinal checked eoc message about the same time it validates first set of received maintenance bits. Then it shall issue ARL indication instead of AR.
3. The MC145572 issues AIL indication for as long as loopback is active.

Figure 8–16. Time Diagram for Activation with Loopback 2 (Always Initiated by the Network)



NOTES:

1. According to recommendation T1E1.4/92–194, LT initiates request by lowering act bit.
2. LT requests loopback by means of eoc message.
3. Part will issue AIL indication for as long as loopback is active.
4. LT will hold sending the downstream act bit until the eoc loopback message is acknowledged.

Figure 8–17. Time Diagram for Execution of Loopback 2 Once Link is Active (Always Initiated by the Network)

8.5 GCI MASTER AND SLAVE MODE OPERATION

The MC145572 can be configured for GCI master or GCI slave operation independently of LT or NT configuration. When the pin M/S is pulled low to $V_{SS,}$ GCI slave operation is selected. When the pin M/S is pulled high to V_{DD} GCI master operation is selected. When configured as a slave FSC is an input driven by external circuitry. FSC must be synchronized to the clock applied to DCL. When configured as a master the MC145572 drives FSC as an output.

8.6 U-INTERFACE SUPERFRAME ALIGNMENT

The MC145572 uses the FSC signal to indicate superframe alignment. In LT mode as a GCI slave the FSC pin is used to force alignment of the transmitted U–interface superframe. Normally the FSC pulse is two DCL clocks in duration. Alignment of the transmitted superframe can be forced by driving FSC with a one DCL clock wide pulse once every 96 GCI frames. The 2B+D data read into the DIN pin following the single clock wide FSC corresponds to the first 2B+D transmitted onto the U–interface. If superframe alignment is not input to FSC the MC145572 aligns the outgoing U–interface superframe.

When configured for master mode and either LT or NT operation reception of the first 2B+D data from the U–interface superframe is indicated by the MC145572 outputting a FSC pulse that is one DCL clock wide. This happens once every 96 GCI frames.

In NT mode, IDL2 slave operation, any superframe alignment information that may be present on FSC is ignored. ANSI T1.601 defines when the NT transmitted superframe occurs with respect to the received superframe.

WARNING

If FSC is to be used to set the alignment of the transmitted superframe in LT mode it must be stable prior to activating the MC145572.

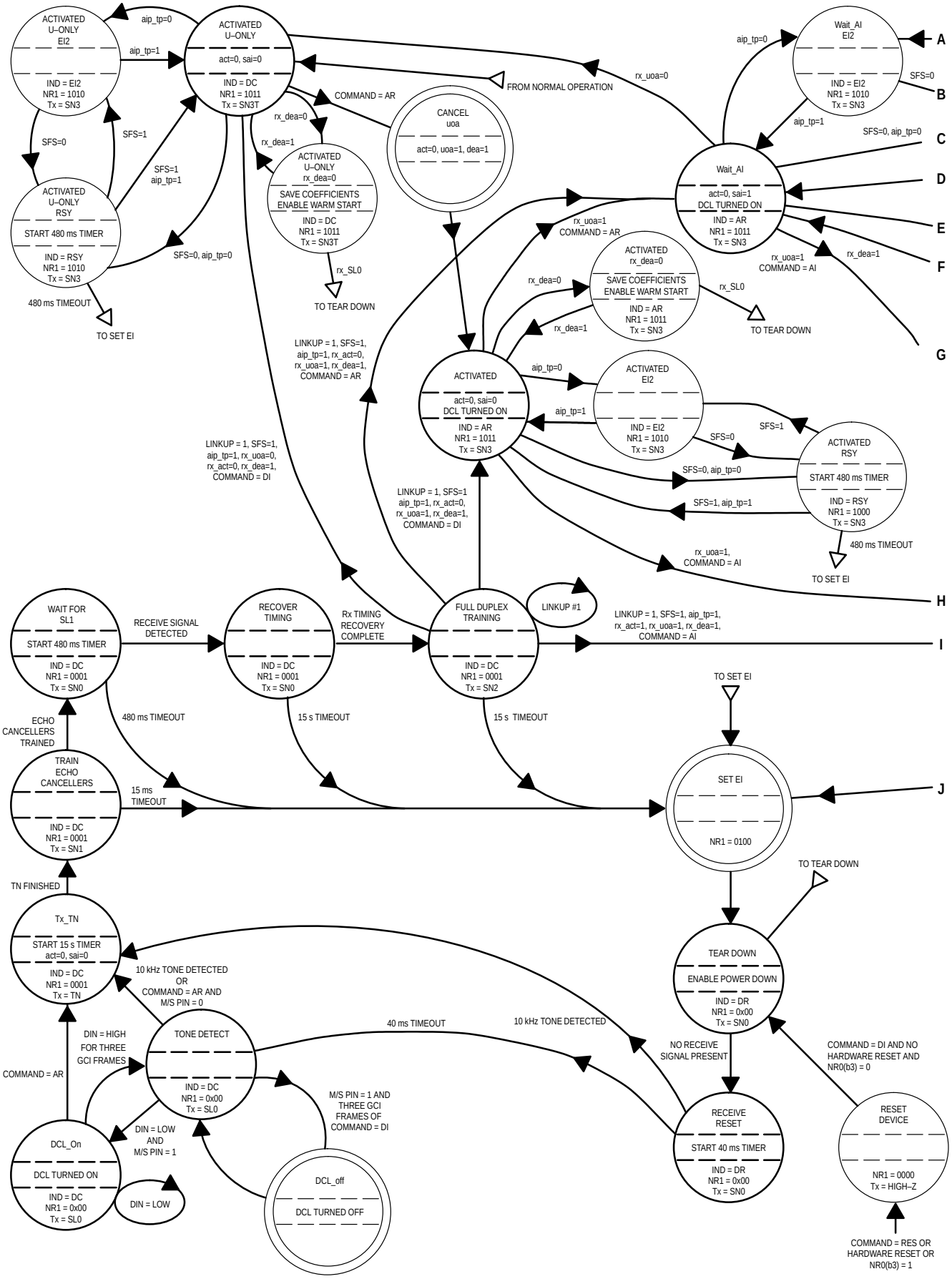
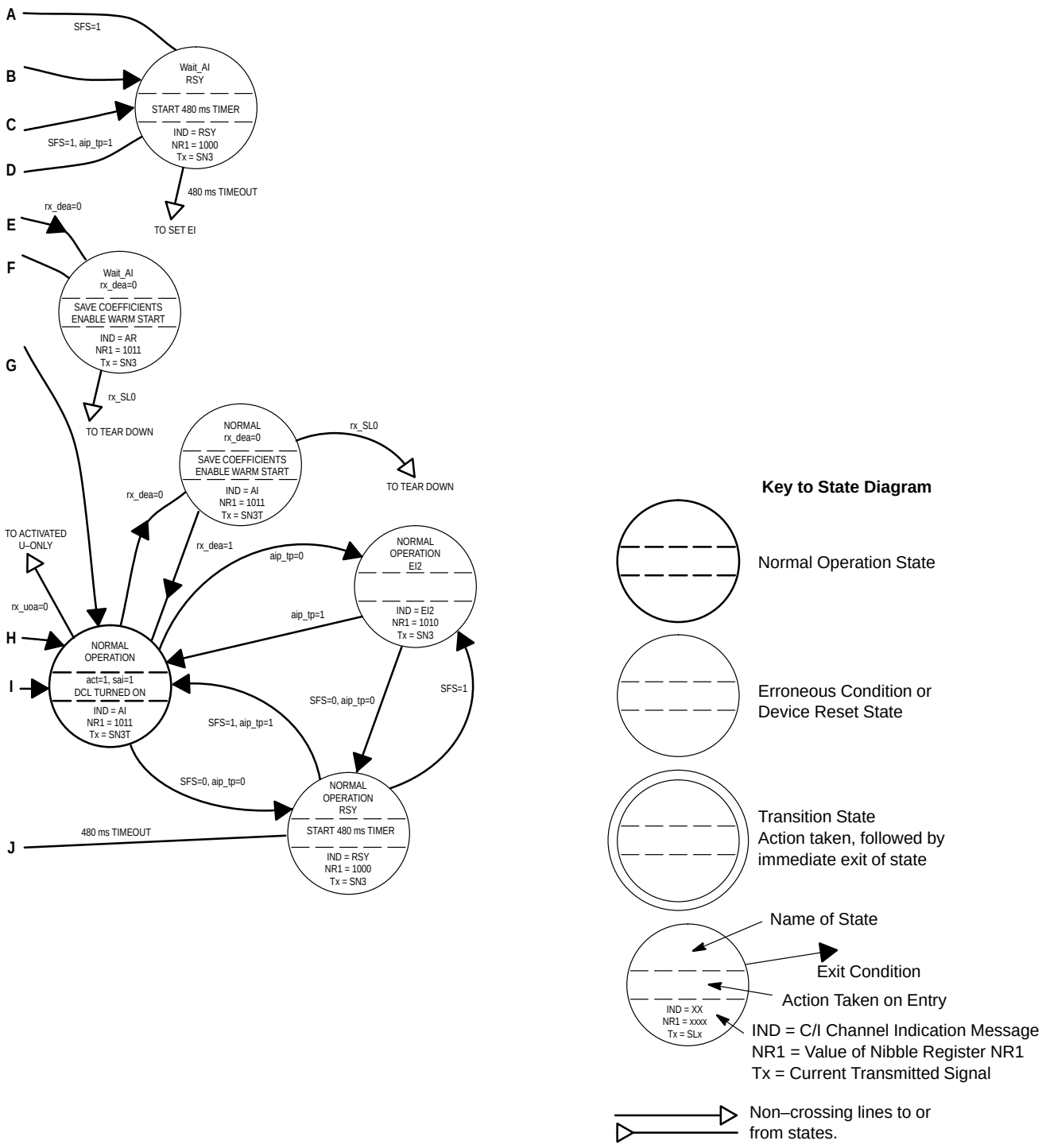


Figure 8–18. NT Mode GCI State Diagram (Sheet 1 of 2)



NOTES:

1. An “x” in the NR1 bit means that the bit remains unchanged from its value in a previous state.
2. The transmitted M4 channel bits remain unchanged between states unless a change is explicitly indicated.
3. SL3T is SL3 with transparent data transmission.
4. The state “Normal Operation” is the state in which the MC145572 operates when it is fully activated, transmitting 2B+D with transparency enabled.
5. Linkup=NR1(b3), SFS=NR1(b1), aip_tp=NR1(b0).
6. Warm start is only enabled when the MC145572 transitions from the four states that enable warm start directly to the “Tear Down” state. Any other transition disables warm start.

Figure 8–18. NT Mode GCI State Diagram (Sheet 2 of 2)

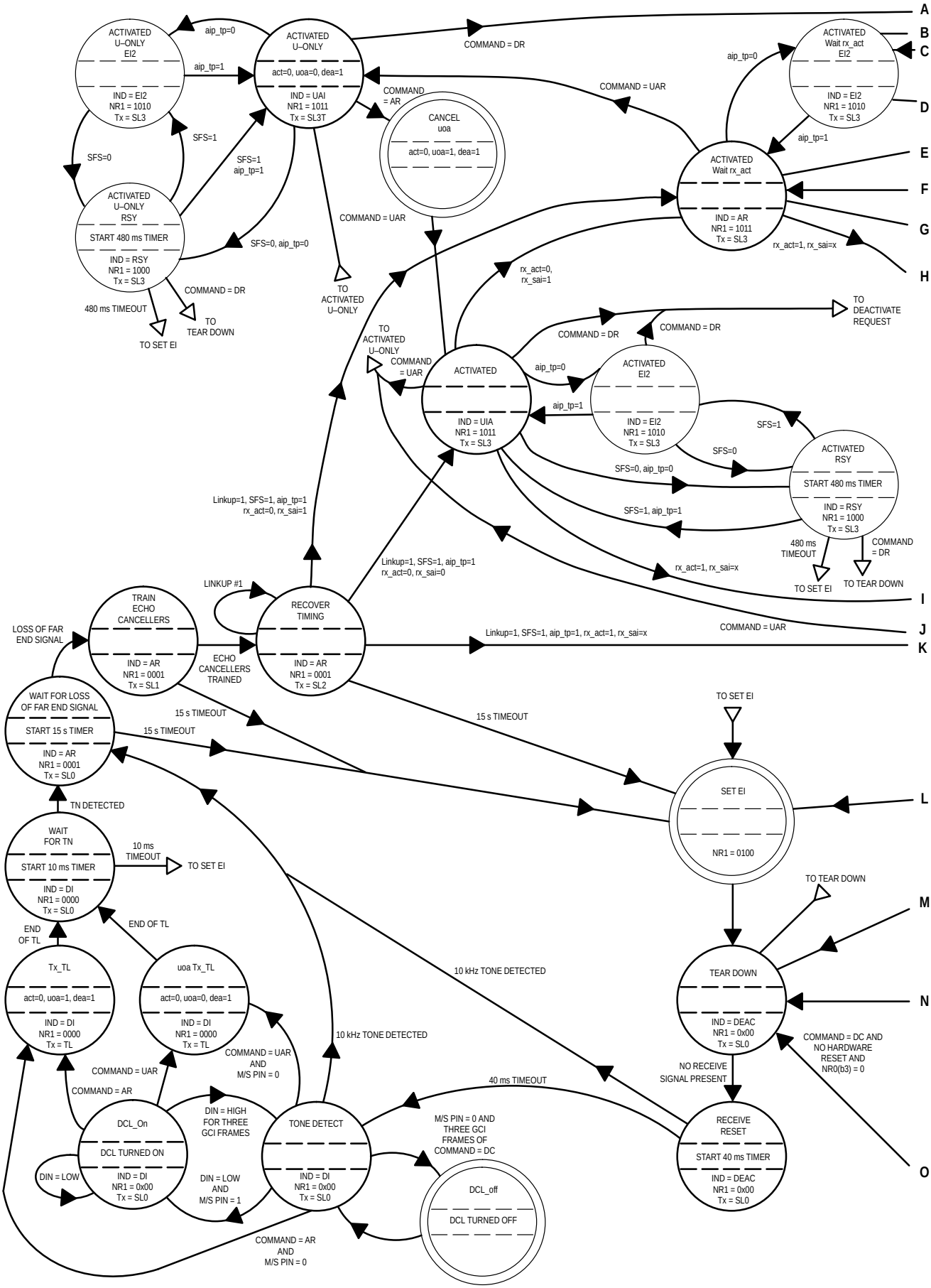
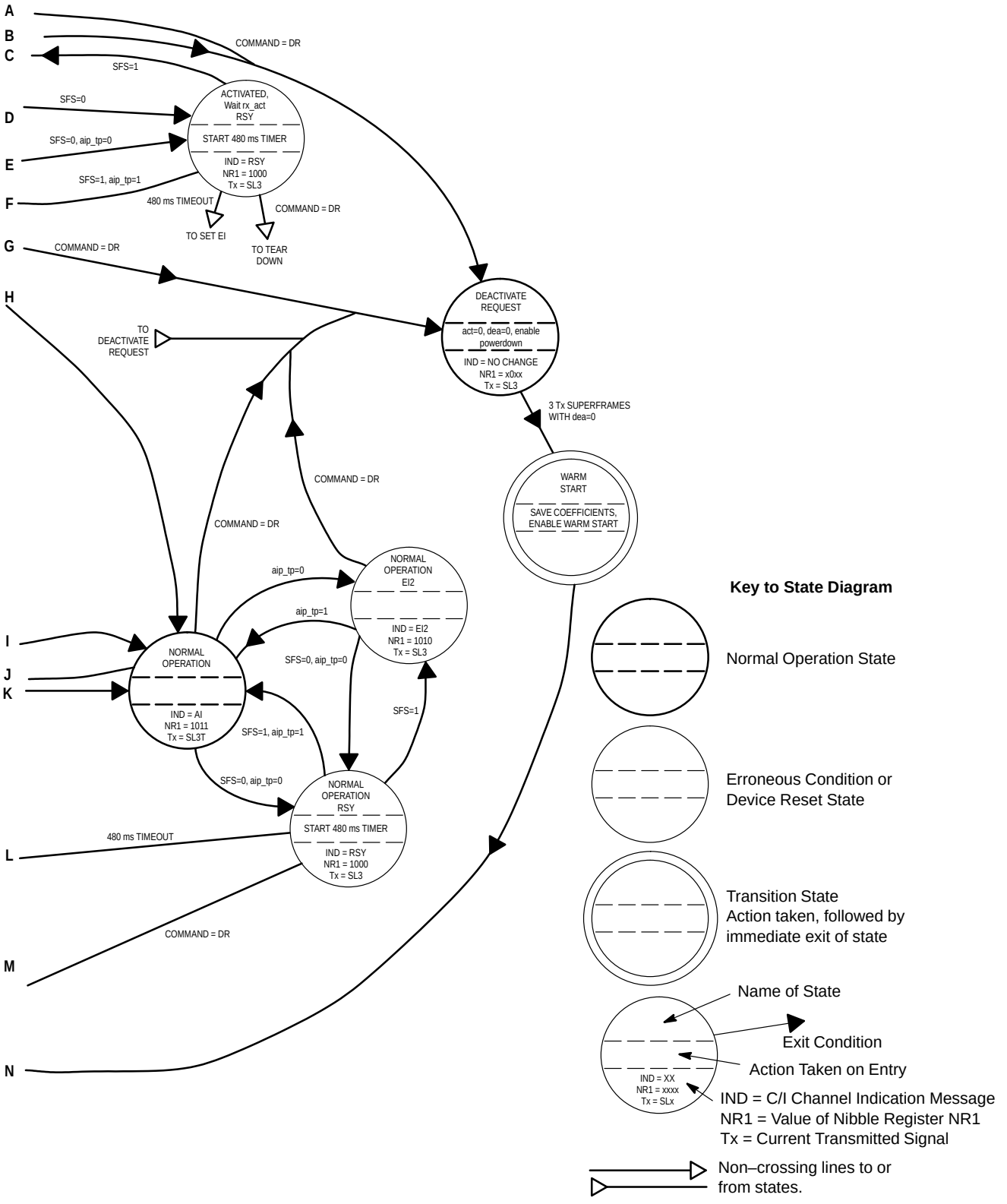


Figure 8–19. LT Mode GCI State Diagram (Sheet 1 of 2)



NOTES:

1. An “x” in the NR1 bit means that the bit remains unchanged from its value in a previous state.
2. The transmitted M4 channel bits remain unchanged between states unless a change is explicitly indicated.
3. SL3T is SL3 with transparent data transmission.
4. The state “Normal Operation” is the state in which the MC145572 operates when it is fully activated, transmitting 2B+D with transparency enabled.
5. Linkup=NR1(b3), SFS=NR1(b1), aip_tp=NR1(b0).

Figure 8–19. LT Mode GCI State Diagram (Sheet 2 of 2)