5
MCU MODE DEVICE FUNCTIONALITY

5.1 FUNCTIONAL OVERVIEW

This section describes operation of the MC145572 when operated in MCU mode.

A functional block diagram of the MC145572 U–interface transceiver is shown in Figure 5–1. This device utilizes mixed analog and digital signal processing circuit technology to implement an adaptively equalized echo canceling full–duplex transmitter/receiver or transceiver.

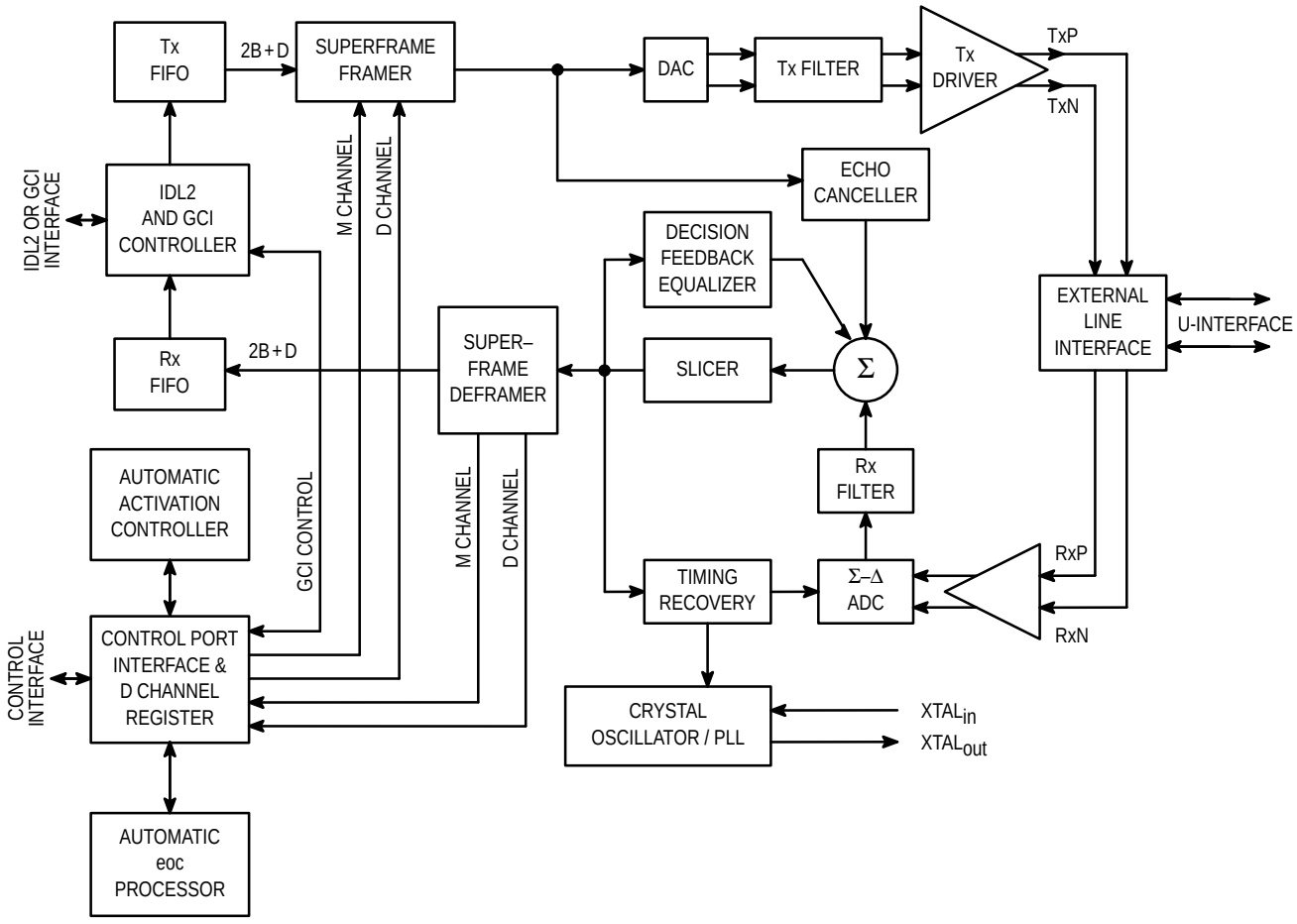


Figure 5–1. MC145572 Functional Block Diagram

The 2B+D data is input to the device at the D_{in} pin of the time division multiplexed data interface. This data is passed through a three frame deep FIFO prior to being formatted and scrambled in the Superframe Framer. The resulting 160 kbps binary data stream is converted to an 80 kbaud dibit stream which is subsequently converted to four analog amplitudes by the DAC (digital–to–analog converter). The resulting pulse amplitude modulated signal is band limited by the Tx Filter prior to entering the Tx Driver which differentially drives the line coupling circuit to the twisted wire pair.

From the twisted wire pair, information from the far end U–interface transceiver is coupled through the external line interface circuit to the differential receiver inputs RxP and RxN. (In this two wire environment, the transmitted signal is also coupled into the receiver inputs.) This combined analog signal

is converted to a digital word in the Σ–Δ (sigma–delta) ADC (analog–to–digital converter). After filtering, an adaptively generated replica of the transmitted signal, calculated by the echo canceler, is subtracted from the combined signal leaving only the far end signal. In addition, phase distortion present in the far end signal is corrected by the Decision Feedback Equalizer. The resulting four level signal is decoded by the slicer to produce a 160 kbps data stream. Timing information is also recovered from the far end signal. The Superframe Deframer descrambles and disassembles the received superframes and passes the received 2B+D data through a three IDL frame deep FIFO to the IDL Interface where it is available at the D_{out} pin of the time division multiplexed data interface.

The MC145572 permits the designer to select one of three options for control of the device and access to its register set. When operating in MCU mode the MC145572 can be configured for either Serial Control Port or Parallel Port mode of operation. In Serial Control Port mode control and status of the device is handled via the Serial Control Port (SCP), a standard four wire serial microcontroller interface. In Parallel Control Port mode the MC145572 is configured to provide an eight bit wide data port with a chip select and read/write pin. In either case the internal register set of the MC145572 gives an external microcontroller access to the 4 kbps Maintenance Channel provided across the U–interface.

When the MC145572 is configured for GCI mode the Command/Indicate channel of the GCI interface is used for control and status messages. The GCI Monitor channel is used to send and receive maintenance channel messages. The Monitor channel also permits the internal registers of the MC145572 to be read from or written to if it is desired to bypass the normal operation of the GCI interface.

The Embedded Operations Channel (eoc) portion of the M–channel can be handled automatically with the internal Automatic eoc Processor. In addition, activation and deactivation of the MC145572 is handled by an Automatic Activation Controller.

The MC145572 requires a single 20.48000 MHz pullable crystal connected between the $XTAL_{in}$ and $XTAL_{out}$ pins. No other external components are required for the crystal oscillator. Internal crystal pulling circuitry adjusts the crystal frequency in both the LT and NT modes of operation.

Detailed descriptions of the various interfaces and user accessible sections are provided in this section.

5.2 MC145472/MC14LC5472 COMPATIBILITY

After either a hardware or software reset the MC145572 maintains basic pin function and register compatibility with the MC14LC5472 U–interface transceiver when configured for MCU mode and using the Serial Control Port interface. There are differences between the MC14LC5472 and the MC145572 in exact signal requirements and outputs for these pins.

Most software written for the MC14LC5472 will operate the MC145572 without requiring any modifications. The MC145572 has an extended register set which provides access to the on chip timeslot assigner, I/O pin configuration bits, the D Channel, and internal parameters of the device. The extended registers are accessed by setting bits in register BR10 that were reserved bits for the MC14LC5472. The new registers then overlay the original registers and are referred to in this document as Overlay Registers OR0 through OR9, OR12 and OR13. Register BR10 is common to both register sets permitting software to switch between the basic register set and the overlay register set as required. Tables 4–1, 4–2 and 4–3 detail the register set of the MC145527. See Section 4, ***Register Description*** for details on the register set.

Tables 5–1 and 5–2 contain the MC145572 pin function charts. The MC145572 requires a line interface transformer having a turns ratio of 1 : 1.25 where the 1.25 is on the tip and ring side of the transformer. The MC14LC5472 used a line interface transformer having a 1 : 2 turns ratio.

When operated in MCU mode with the Serial Control Port the MC145572 has clock outputs enabled on the 15.36 CLKOUT and BUF XTAL pins after a hardware or software reset. On the MC14LC5472 these clocks were disabled after a hardware or software reset. Due to this change the function of bits BR15A(b2, b1) have changed in the MC145572. In the MC14LC5472 these two bits enabled the 15.36 CLKOUT and BUF XTAL outputs respectively when set to a ‘1’. In the MC145572 these bits are reserved and writing a ‘1’ to either of these bits to enable a clock leaves the clock(s) enabled. To disable one or both of these clocks software must set either bit b2 or bit b1 in Overlay Register OR9.

Table 5–1. Mode Pin Breakout Summary and Comparison

Function	PLCC Pin #	TQFP Pin #	MC145572	MC14LC5472
V_{DD}	44	27	+5 V	+5 V
V_{SS}	2, 22	29, 5	Connect to Ground	Connect to Ground
V_{DD} I/O	24, 37	7, 20	+5 V or +3 V	+5 V
V_{SS} I/O	23, 36	6, 19	Connect to Ground	Connect to Ground
V_{DD} Rx	3	30	+5 V	+5 V
V_{SS} Rx	4	31	Connect to Ground	Connect to Ground
V_{DD} Tx	11	38	+5 V	+5 V
V_{SS} Tx	10	37	Connect to Ground	Connect to Ground
TxP/TxN	9, 12	36, 39	Transmit Output	Transmit Output
RxP/RxN	5, 6	32, 33	Receive Input	Receive Input
$V_{ref}N/V_{ref}P$	7, 8	34, 35	Voltage Reference	Voltage Reference
$XTAL_{in}/XTAL_{out}$	33, 32	16, 15	Pullable Crystal Only	Pullable Crystal and Other Components
FREQREF	42	25	8 kHz Reference Input	Accepts One of 8 Reference Frequencies
RESET	14	41	Reset When Low	Reset When Low
MCU/GCI	43	26	MCU When = 1 GCI When = 0.	Not Applicable
NT/LT	15	42	NT Mode When = 1 LT Mode When = 0	NT Mode When = 1 LT Mode When = 0
M/S	16	43	Master Mode when = 1 Slave Mode when = 0	Master Mode when = 1 Slave Mode when = 0
PAR/$\overline{SER}$	13	40	Select MCU Parallel Control Port When = 1 Select MCU Serial Control Port When = 0.	Not Applicable

Table 5–2. Pin Function per Mode and MC14LC5472 Comparison

MC145572 Function						MC14LC5472
PLCC Pin #	**TQFP Pin #**	**MCU/SCP Mode**	**MCU/PCP Mode**	**GCI Master Mode**	**GCI Slave Mode**	**Function**
17	44	$\overline{IRQ}$	$\overline{IRQ}$	Not Used	Not Used	$\overline{IRQ}$
21	4	$\overline{SCPEN}$	$\overline{CS}$	IN1 (Note 8)	IN1	$\overline{SCPEN}$
20	3	SCPCLK	R/$\overline{W}$	IN2 (Note 8)	IN2	SCPCLK
18	1	SCP Rx	D0	OUT1 (Note 9)	OUT1 (Note 9)	SCP Rx
19	2	SCP Tx	D1	OUT2	OUT2	SCP Tx
27	10	FSR (Note 1)	FSR (Note 1)	FSC	FSC	IDL SYNC
28	11	FSX (Note 2)	FSX (Note 2)	Not Used	Not Used	Not Applicable
31	14	DCL	DCL	DCL	DCL	IDL CLK
29	12	D_{in}	D_{in}	D_{in}	D_{in}	IDL RX
30	13	D_{out}	D_{out}	D_{out}	D_{out}	IDL TX
34	17	4.096 CLKOUT	D2	4.096 CLKOUT	4.096 CLKOUT	4.096 CLKOUT
35	18	15.36 CLKOUT	D3	15.36 CLKOUT	15.36 CLKOUT	15.36 CLKOUT
38	21	BUF XTAL	D4	BUF XTAL	BUF XTAL	BUF XTAL
26	9	Tx SFS (Note 3)	Tx SFS (Note 3)	S0	S0	Tx SFS
25	8	SYSCLK (Note 4)	SYSCLK (Note 4)	S1	S1	SYS CLK
39	22	EYE_{out} (Note 5)	D5	S2	S2	EYE DATA
40	23	TxBCLK (Note 6)	D6	Not Used	$FREF_{out}$	Tx BAUD CLK
41	24	RxBCLK (Note 7)	D7	CLKSEL	Not Used	Rx BAUD CLK

NOTES: 1. When the IDL2 interface is operating in the GCI electrical mode, this pin is named FSC.
2. When the IDL2 interface is operating in the GCI electrical mode, this pin is unused.
3. SFAX is muxed onto this pin.
4. 20.48 MHz, SFAR, and TSEN are muxed onto this pin.
5. DCHCLK and TxOFF are muxed onto this pin.
6. DCH_{in} and TxMAG are muxed onto this pin.
7. DCH_{out} and TxSIGN are muxed onto this pin.
8. In the NT mode, IN1 and IN2 carry PS1 and PS2 data.
9. DISS is OR'd into this output.

5.3 CONTROL INTERFACES

When operated in MCU mode the MC145572 has two configurations that provide MCU access to its internal register set. The Serial Control Port mode is a four wire serial interface that clocks data into or out of the MC145572 at data rates up to 4 Mbps. This interface is compatible with National's MICRO WIRE™ interface. The Parallel Control Port mode configures the MC145572 to have an eight bit parallel data port that can be located anywhere in processor memory. The Parallel Control Port mode is enabled when the MCU/GCI pin is tied to a '1' and the PAR/SER pin is tied to a '1'. The Serial Control Port mode is enabled when the MCU/GCI pin is tied to a '1' and the PAR/SER pin is tied to a '0'.

NOTE

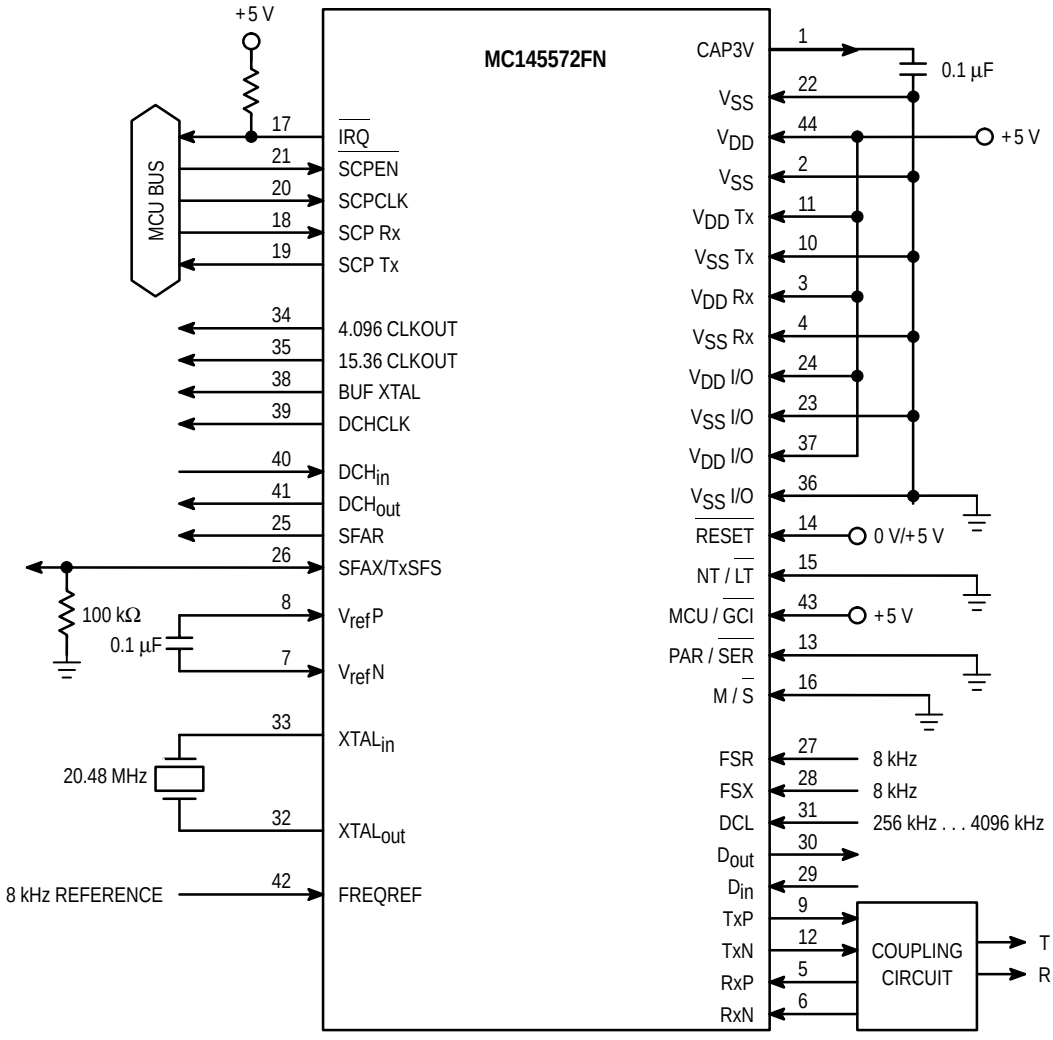
When the MC145572 is configured for MCU operation it is possible to put the IDL2 interface pins into the GCI Electrical mode which accepts GCI timing for transfer of 2B+D data only. This is done by setting bit OR6(b3) GCI Mode Enable. Access to the MC145572 register set is via the the Serial Control Port or the Parallel Port. In GCI Electrical mode the pin names and functions for the IDL2 interface pins correspond to the GCI names and function.

5.3.1 Serial Control Port Mode

The MC145572 is equipped with an industry standard Serial Control Port Interface. The Serial Control Port (SCP) is used by an external controller, such as an M68HC05 family microcontroller, MC145488 Dual Data Link Controller, or MC68302 Integrated Multiprotocol Processor, to communicate with the U–interface transceiver.

The SCP is a full–duplex four wire interface with control and status information passed to and from the U–interface transceiver. The Serial Control Port Interface consists of a transmit output, a receive input, a data clock, and an enable signal. These device pins are known as SCP Tx, SCP Rx, SCPCLK, and SCP EN, respectively. The SCP Clock determines the rate of exchange of data in both the transmit and receive directions, and the SCP Enable signal governs when this exchange is to take place. The four wire SCP Interface is supplemented with an interrupt request line, IRQ, for external microcontroller notification of an event requiring service.

The operation and configuration of the U–interface transceiver is controlled by setting the state of the control registers within the U–interface transceiver and monitoring the status registers. The control, status, and M–channel data registers reside in six 4–bit wide Nibble Registers, one 12–bit wide Nibble Register, and twenty nine 8–bit wide Byte Registers. A complete register map and detailed register descriptions can be found in Section 4. Figure 5–2 shows pin configurations to operate the MC145572 in IDL2 mode using the Serial Control Port for access to the register set. See Chapter 10 for the SCP timing diagrams.



NOTE: In LT mode the 100 kΩ resistor on SFAX/TxSFS is required when none of these pin functions is enabled.

Figure 5–2. MCU Mode with Serial Control Port Configuration

5.3.1.1 NIBBLE REGISTER OPERATION

The 4–bit Nibble Registers are accessed via an 8–bit SCP Interface operation as shown in Figure 5–3 for a write operation and Figure 5–4 for a read operation. The first bit of the transfer on SCP Rx is a read/write (R/W) bit indicating the purpose of the operation. This is followed by a 3–bit address field (A2:A0) which specifies nibble address 0 through nibble address 5. (Nibble addresses 6 and 7 have other purposes which are described later.) For a write operation, the 4–bit data word (D3:D0) follows. For a read operation, the 4–bit data word (D3:D0) follows on the SCP Tx pin.

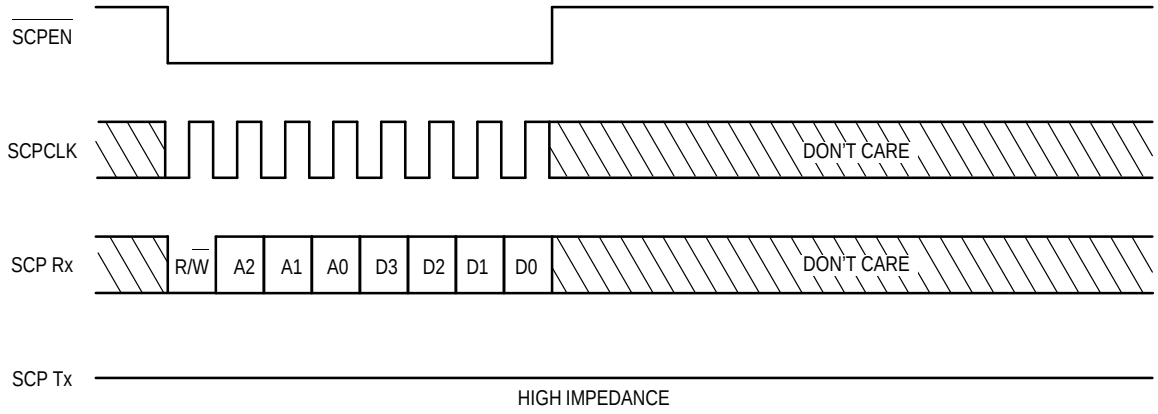


Figure 5–3. SCP Nibble Register 0 – 5 Write Operation

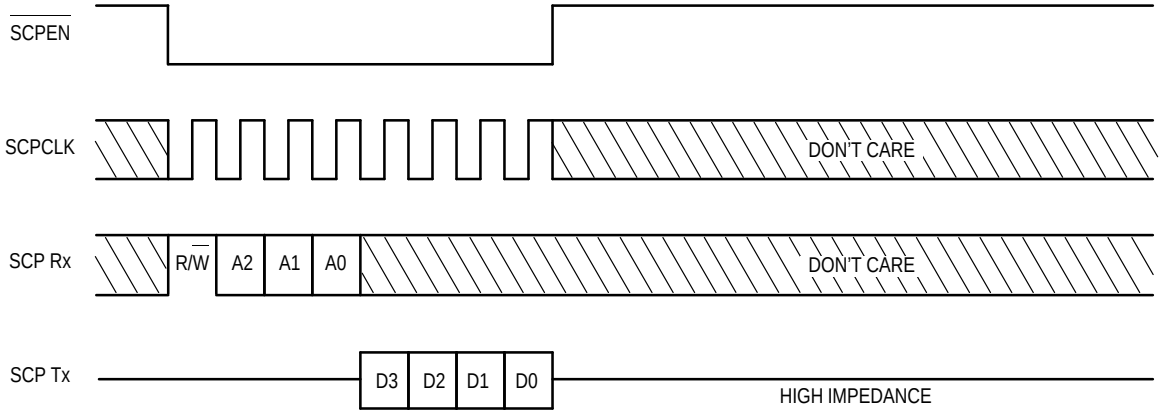


Figure 5–4. SCP Nibble Register 0 – 5 Read Operation

5.3.1.2 REGISTER R6 OPERATION

The 12–bit Nibble Register 6 is located at nibble register address 6 and can be accessed with two sequential 8–bit SCP Interface operations as shown in Figures 5–5 and 5–6. In this case, the second 8–bit operation accesses the last 8 data bits (D7:D0) as shown. Alternatively, this register can be accessed with a single 16–bit operation as shown in Figures 5–7 and 5–8. See Register R6 description in **Section 4.3.7** for correspondence between the ANSI defined eoc bits and the data bits transferred over the SCP interface.

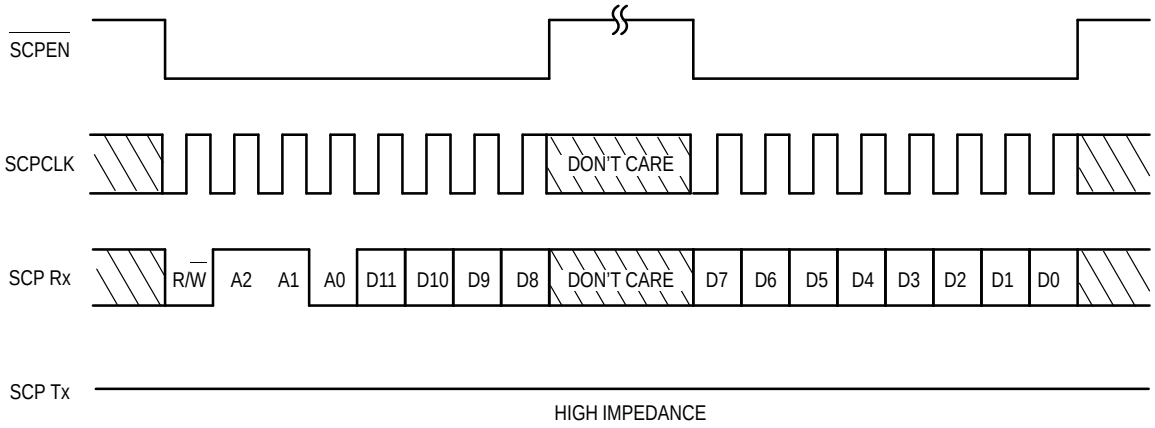


Figure 5–5. SCP eoc Register R6 Write Operation Using Double 8–Bit Transfer

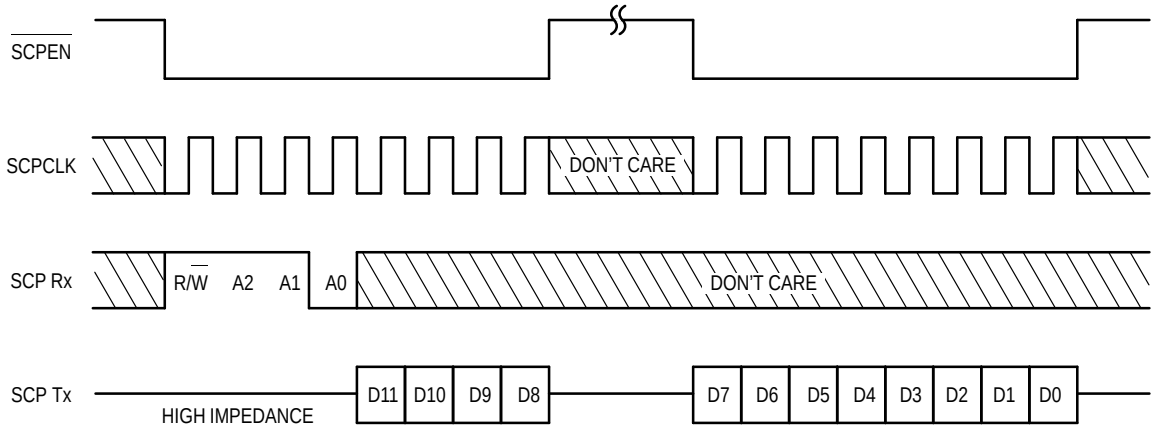


Figure 5–6. SCP eoc Register R6 Read Operation Using Double 8–Bit Transfer

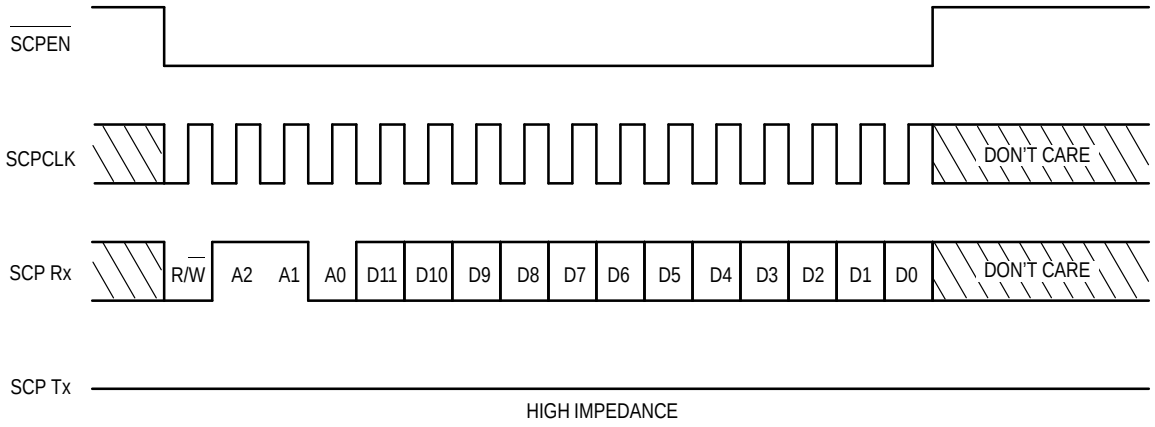


Figure 5–7. SCP eoc Register R6 Write Operation Using Single 16–Bit Transfer

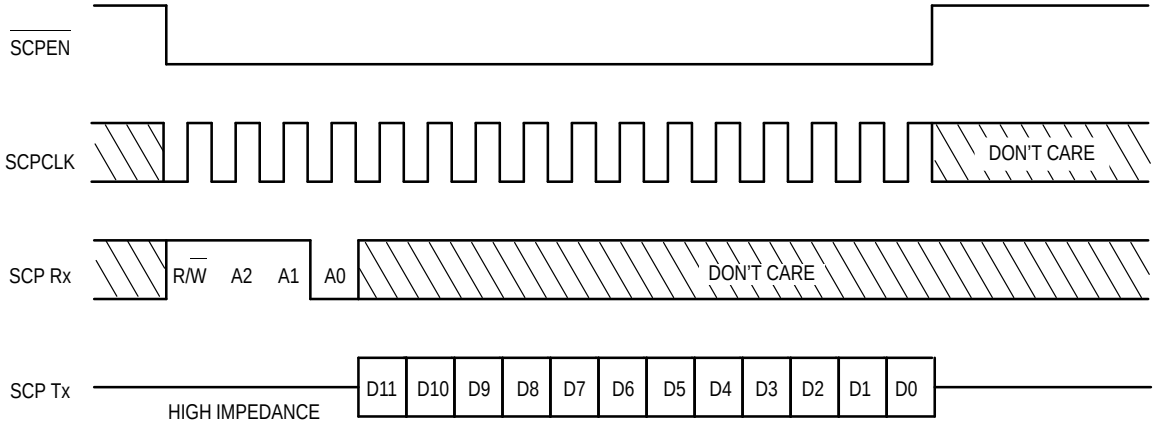


Figure 5–8. SCP eoc Register R6 Read Operation Using Single 16–Bit Transfer

5.3.1.3 BYTE REGISTER OPERATION

The 16 Byte Registers are addressed by addressing nibble address 7 followed by a 4–bit byte register address (A3:A0) as shown in Figures 5–9 and 5–10. A second 8–bit operation transfers the data word (D7:D0). Alternatively, these registers can be accessed with a single 16–bit operation as shown in Figures 5–11 and 5–12.

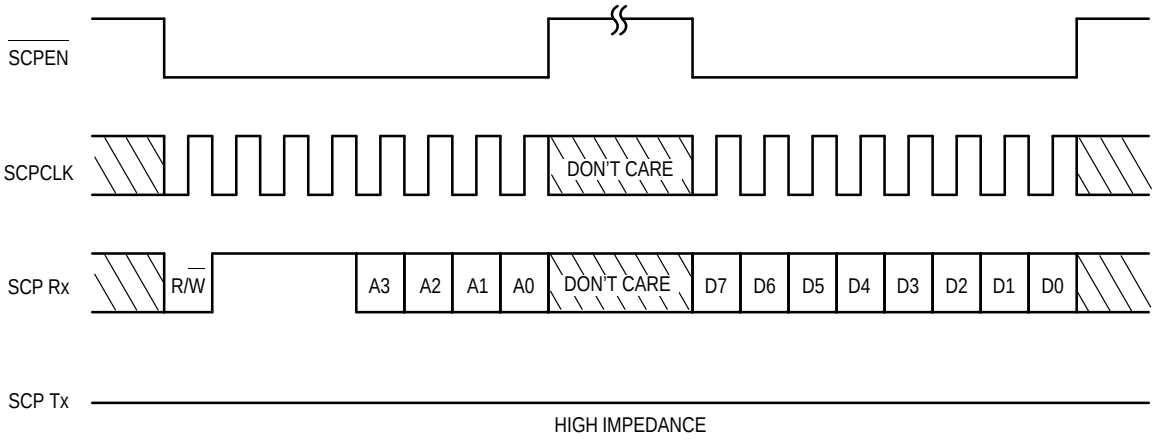


Figure 5–9. SCP Byte Register Write Operation Using Double 8–Bit Transfer

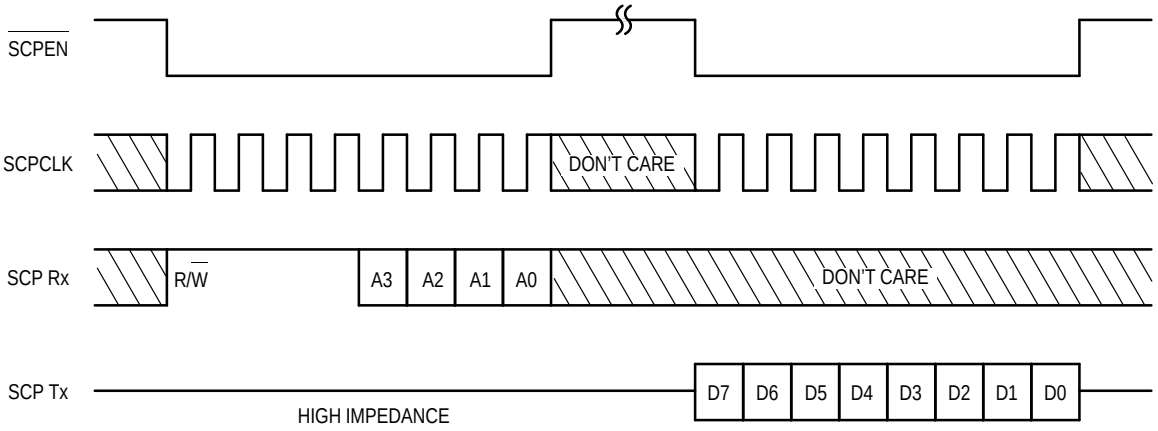


Figure 5–10. SCP Byte Register Read Operation Using Double 8–Bit Transfer

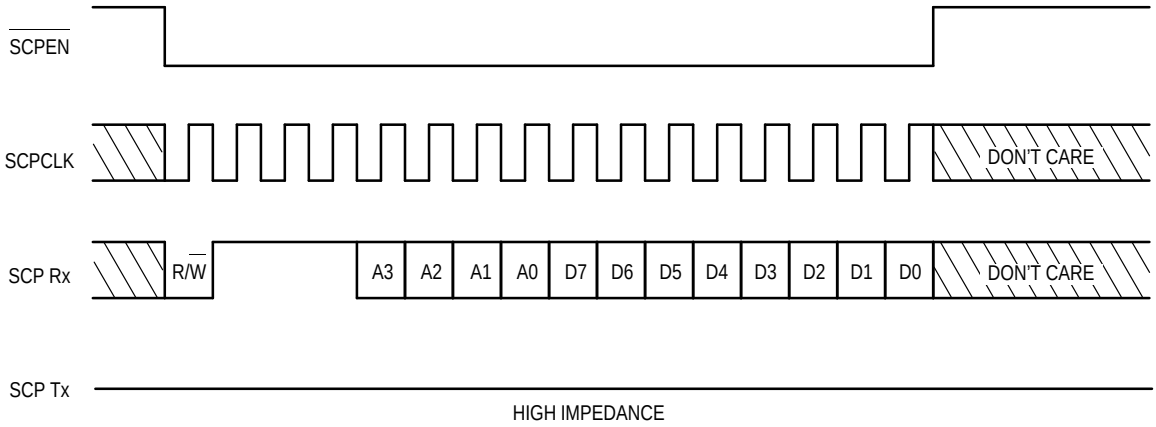


Figure 5–11. SCP Byte Register Write Operation Using Single 16–Bit Transfer

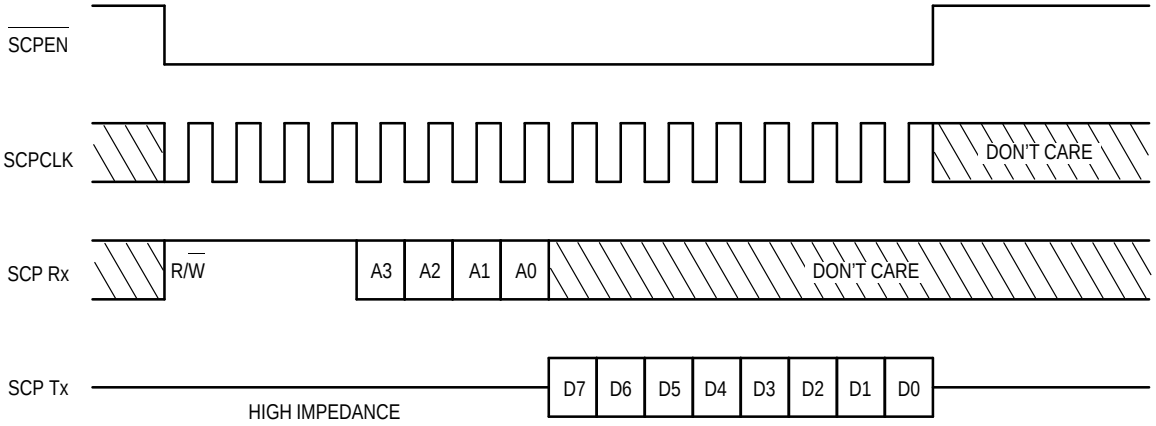
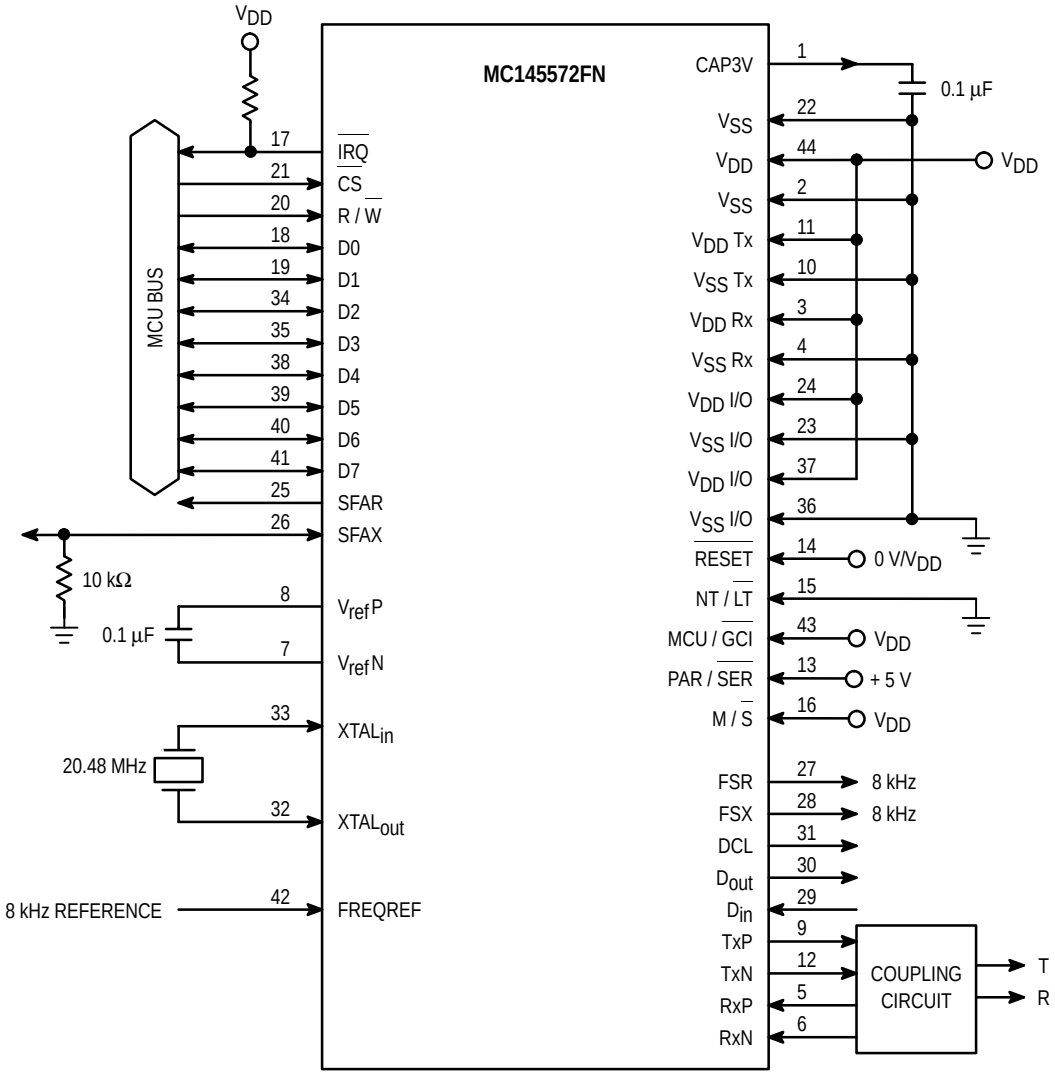


Figure 5–12. SCP Byte Register Read Operation Using Single 16–Bit Transfer

5.3.2 Parallel Control Port Mode

In the Parallel Control Port mode the MC145572 is configured to have a single address byte wide data port for access to the internal register set. A read/write pin (R/W) and chip select pin (CS) are provided to enable read or write accesses to the data port. For an external microcontroller such as the MC68302 to access an individual nibble, byte or overlay register a sequence of write and read operations is required. The first access is always a write cycle that writes a pointer and internal read/write indicator to the MC145572. The pointer byte contains the Nibble or Byte Register address and for the case of Nibble Register writes the data to be written. This initial write may be followed by up to two read accesses or one write access. An open drain IRQ output pin is provided for interrupting an external MCU when a change of status is detected by the MC145572. Figure 5–13 shows pin configurations to operate the MC145572 in MCU mode using the Parallel Control Port for access to the register set.



NOTE: In LT mode the 10 kΩ resistor on SFAX/TxSFS is required when none of these pin functions is enabled.

Figure 5–13. MCU Mode with Parallel Control Port Configuration

5.3.2.1 PARALLEL CONTROL PORT NIBBLE REGISTER OPERATION

Data is written to a Nibble Register using a single Parallel Control Port write operation. The eight bit data word must contain the register address, write bit cleared to ‘0’ and the data to be written as shown in Figure 5–14.

Data is read from a Nibble Register by first writing the nibble register address with the read indicator bit set to a ‘1’ to the parallel data port. Next the parallel data port is read and the data from the register pointed to by the previous write operation appears on bits 0 through 3 of the port. See Figure 5–15. When NR0 through NR5 are read, software should AND the data read with $0F.

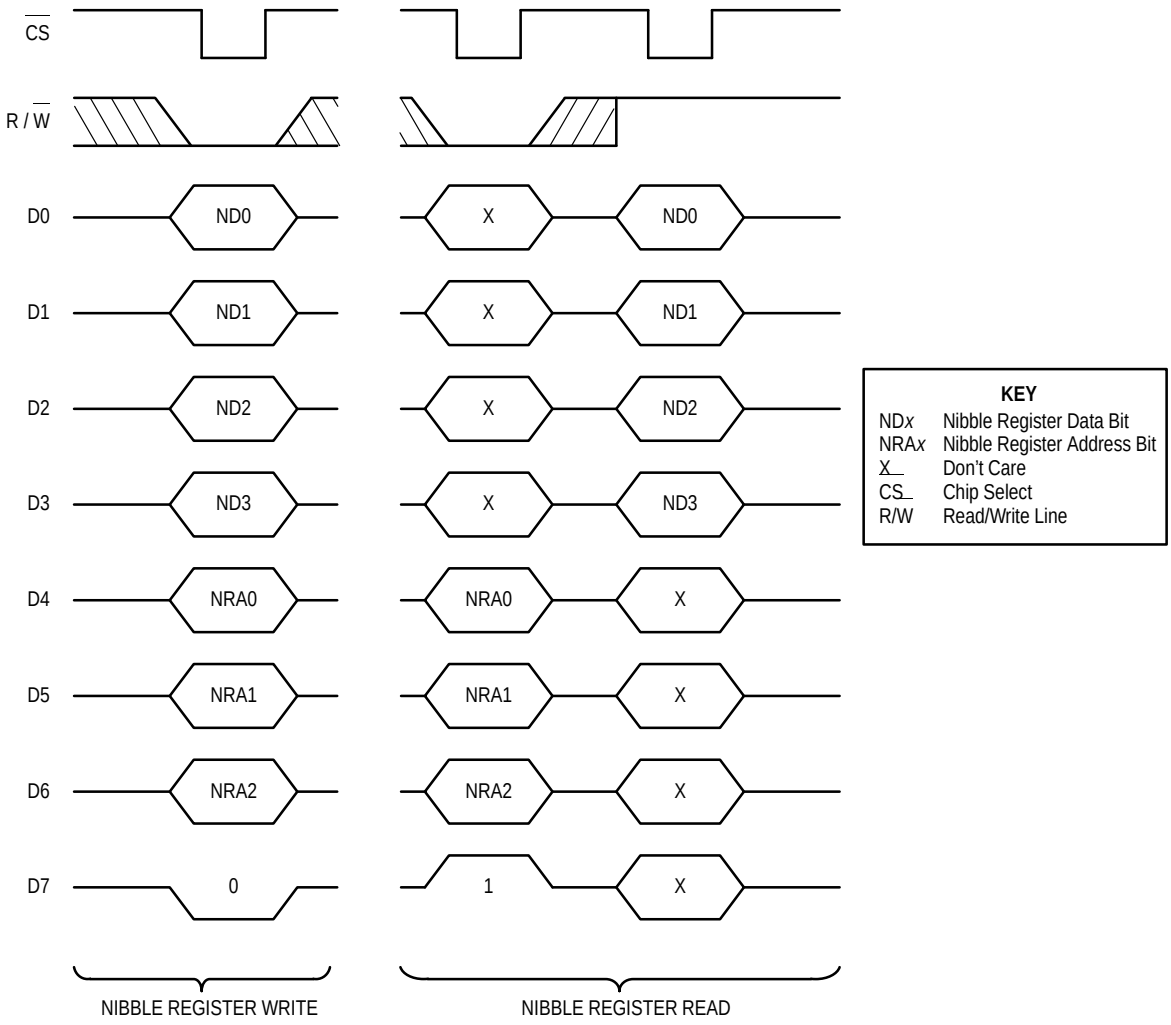


Figure 5–14. Parallel Control Port Mode Nibble Register Write and Read Operations

5.3.2.2 PARALLEL CONTROL PORT REGISTER R6 OPERATION

Data is written to Register R6, the eoc register, by writing two successive bytes to the Parallel Control Port. The first byte must contain the register address, write bit cleared to ‘0’ and the most significant four bits of data to be written as shown in Figure 5–15.

Data is read from Register R6 by first writing a data byte containing the read/write indicator bit set to a ‘1’ and the register address to the Parallel Port. The data is then read from the Parallel Port by reading two bytes. The first byte contains the most significant four bits of data in bits D3:D0. The next byte contains the low order byte of data. See Figure 5–15.

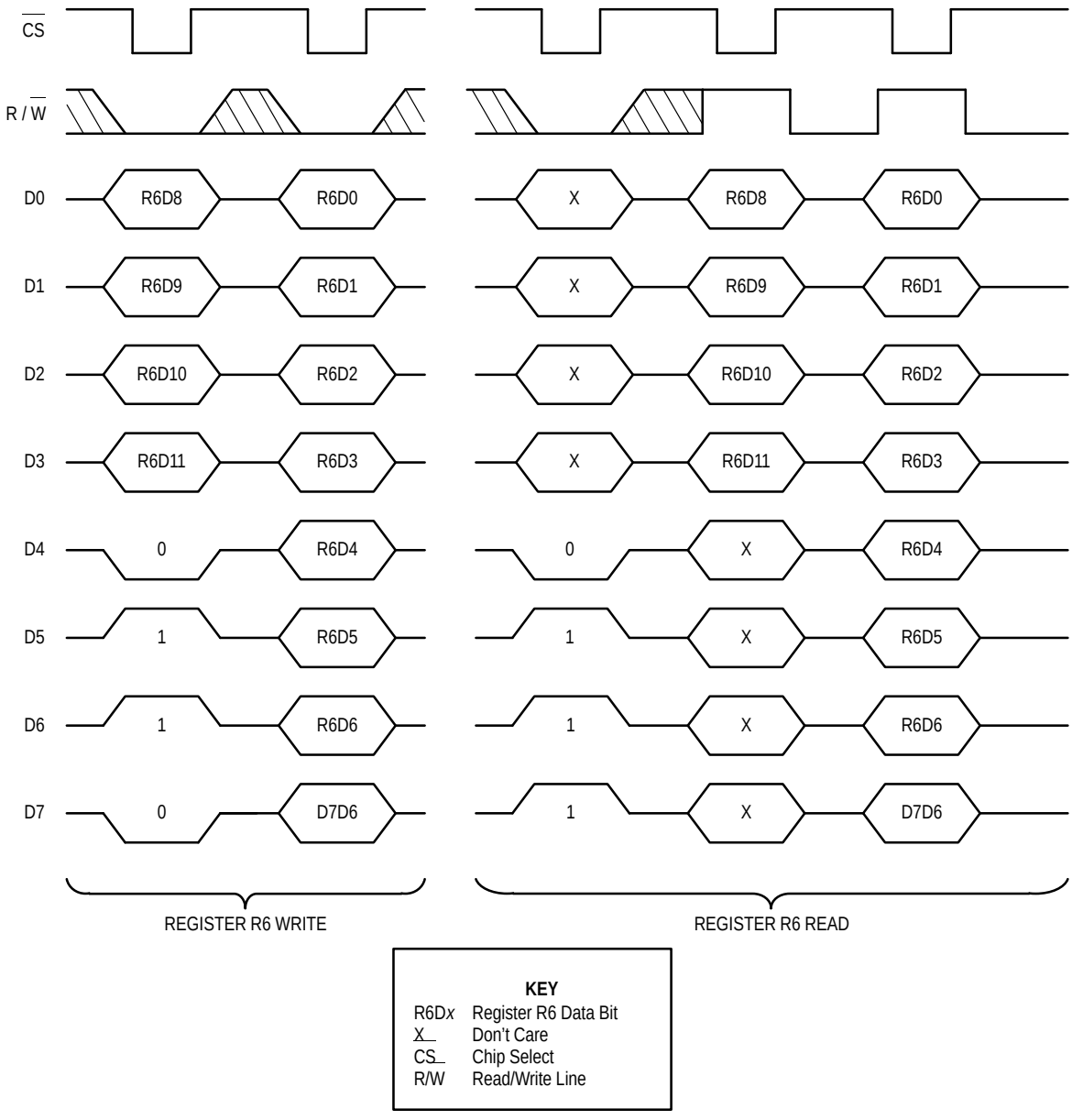
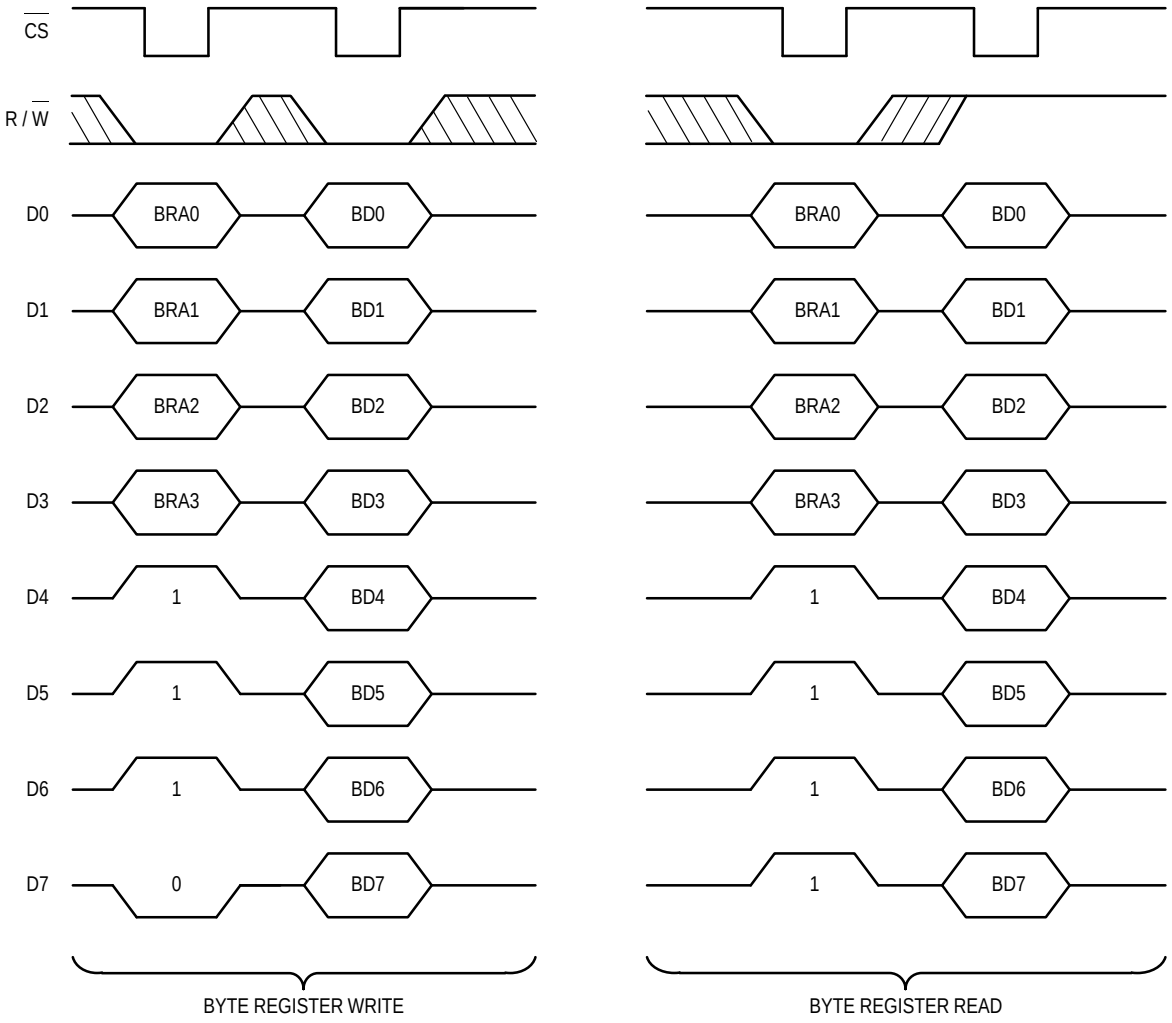


Figure 5–15. Parallel Control Port Register R6 Write and Read Operations

5.3.2.3 PARALLEL CONTROL PORT BYTE REGISTER OPERATION

Data is written to a Byte Register, by writing two successive bytes to the Parallel Control Port. The first byte must contain the register address, write bit cleared to '0', and the address of the Byte Register. The second byte contains the actual data to be written to the selected Byte Register (see Figure 5–16).

Data is read from a Byte Register, by writing the pointer byte to the Parallel Control Port followed by a read of the selected Byte Register from the Parallel Control Port. The first byte must contain the register address, write bit set to '1', and the address of the Byte Register. This is followed by a read cycle to obtain the contents of the selected Byte Register (see Figure 5–16).



KEY	
BD*x*	Byte Register Data Bit
BRA*x*	Byte Register Address Bit
X	Don't Care
CS	Chip Select
R/W	Read/Write Line

Figure 5–16. Parallel Control Port Byte Register Write Operation

5.4 IDL2 TIME DIVISION BUS INTERFACE

The IDL2 Interface consists of six pins: M/$\overline{S}$, FSX, FSR, DCL, D_{in}, and D_{out}. With the M/$\overline{S}$ pin, the IDL2 Interface can be configured as a timing Master (FSR, FSX, and DCL are outputs) or a timing Slave (FSR, FSX, and DCL are inputs). Master or Slave configuration is independent of NT or LT mode selection. The IDL2 Interface receives 2B + D data on the D_{in} pin and buffers it through a FIFO to the U–interface Superframe Framer. Simultaneously, this block accepts 2B + D data from the U–interface Superframe Deframer, buffers it through a FIFO, and transmits it out the D_{out} pin. Refer to Figure 5–1 for a block diagram of the MC145572.

After a hardware or software reset the MC145572 IDL2 interface is configured for short frame operation. Short frame format is compatible with the IDL interface timing used on the MC145472 U–interface transceiver. Table 5–3 details how to configure the MC145572 for the different IDL2 interface data formats. In both short frame and long frame formats two frame sync signals are available, FSX and FSR. In GCI 2B + D data format a single frame sync, FSC, is available.

2B + D Data is transferred over the IDL2 interface at an 8 kHz rate. Each IDL2 2B + D frame contains 8 bits of B1 channel data, 8 bits of B2 channel data, and 2 bits of D channel data. The IDL2 interface supports five different frame formats and a timeslot assigner. The frame formats are long frame and short frame synchronization each with either 8–bit or 10–bit 2B + D data formats. The fifth frame format is the IDL2 GCI Electrical frame format. In this format only the 2B + D data bits of the GCI interface are accessible by the MC145572. Either the Serial Control Port or the Parallel Control Port must be used for access to the internal register set of the MC145572 when IDL2 operation is enabled.

As a master the IDL2 interface of the MC145572 can be configured to output 512 kHz, 2.048 MHz, or 2.56 MHz clock rates at the DCL pin. Table 5–4 is a guide to IDL2 clock rate selection. These data rates apply to all IDL2 frame formats including the GCI 2B + D data format. Please note that when configured for GCI Electrical operation the data rate is one half the DCL clock rate.

As a slave the IDL2 interface of the MC145572 accepts clock rates from 256 kHz to 4.096 MHz at the DCL pin.

A separate D channel port is available when configured for MCU Serial Control Port operation.

Table 5–3. IDL2 Interface Data Format Selection

IDL2 Data Format	OR6 (b3)	OR7 (b3)	BR7 (b0)	Available Frame Syncs	D Channel Port Available	Comments
IDL2 Short Frame Format 10–bit Frame Size (MC145472 Compatible)	0	0	0	FSX, FSR	Yes	Default After hardware or software reset
IDL2 Short Frame Format 8–bit Frame Size (MC145472 Compatible)	0	0	1	FSX, FSR	Yes	
IDL2 Long Frame Format 10–bit Frame Size1	0	1	0	FSX, FSR	No	
IDL2 Long Frame Format 8–bit Frame Size	0	1	1	FSX, FSR	No	
GCI 2B + D Frame Format	1	0	0	FSC	Yes	

NOTE: The timeslot assigner is enabled when one or more of OR6(b7 or b6 or b5) are set to a ‘1’. Enabling the timeslot assigner over rides all other IDL2 frame formats.

Table 5–4. IDL2 Interface Master Mode Clock Rate Selection

Clock Rate	OR7(b4)	BR7(b2)
2.56 MHz	0	0
2.048 MHz	0	1
512 kHz	1	X

5.4.1 Short Frame Operation

Short frame operation is the same as the IDL interface used on the MC145472 and MC14LC5472 U–interface transceivers with one exception. The MC145572 provides for two 8 kHz frame sync pins, FSX and FSR, when operated in IDL2 mode. The FSX pin is used to indicate IDL2 frame synchronization for data input into the D_{in} pin for transmission onto the U–interface. The FSR pin is used to indicate IDL2 frame synchronization for data recovered from the U–interface and output to the D_{out} pin. When configured for master mode, the MC145572 drives FSR and FSX simultaneously. When configured for IDL2 slave operation, the MC145572 FSX and FSR inputs can be driven independently. In slave mode, both FSX and FSR can be connected together so a single synchronization signal can be used to drive both inputs.

Figures 5–17 and 5–18 show typical data formats for short frame operation as a master and configured for 8–bit and 10–bit frame formats respectively. Figures 5–19 and 5–20 show typical data formats for IDL2 operation as a slave and configured for 8–bit and 10–bit frame formats respectively.

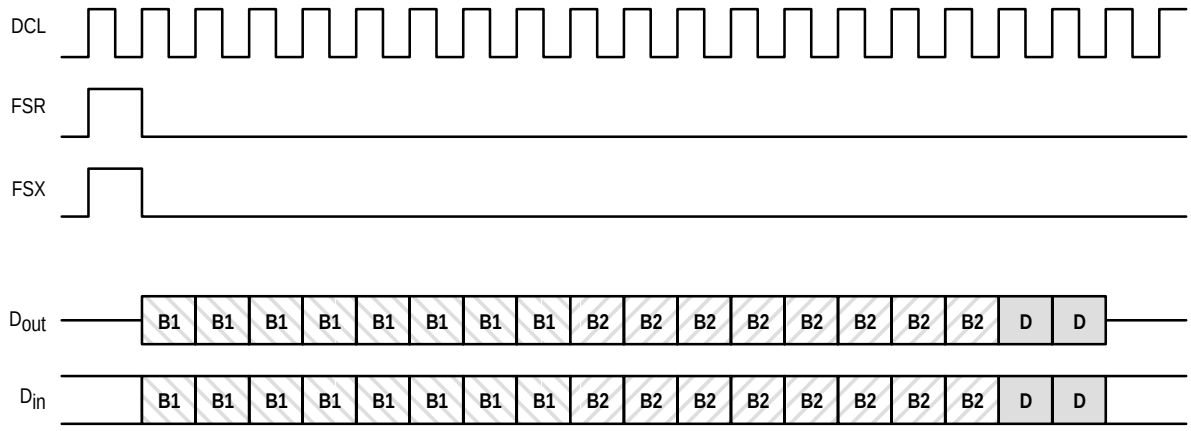


Figure 5–17. IDL2 Interface Timing in Short Frame Master Mode, 8–Bit Frames

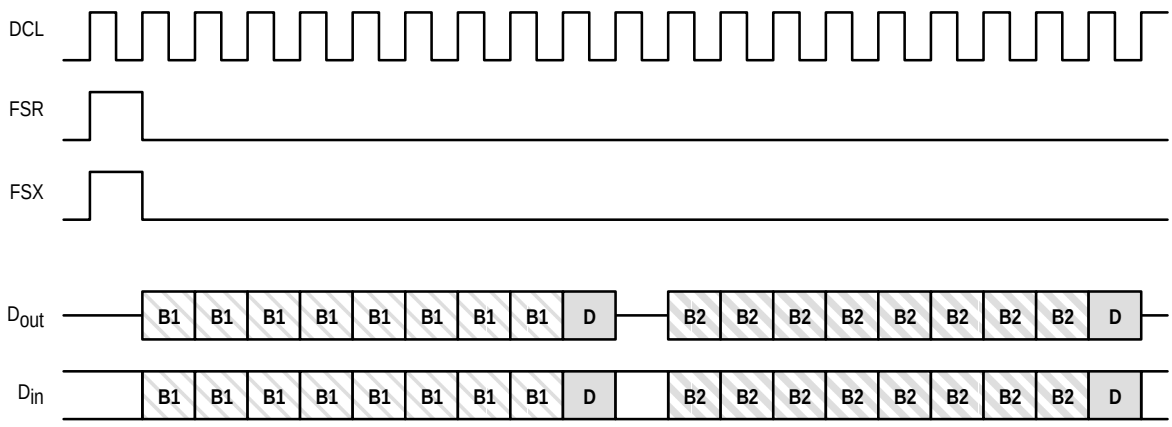


Figure 5–18. IDL2 Interface Timing in Short Frame Master Mode, 10–Bit Frames

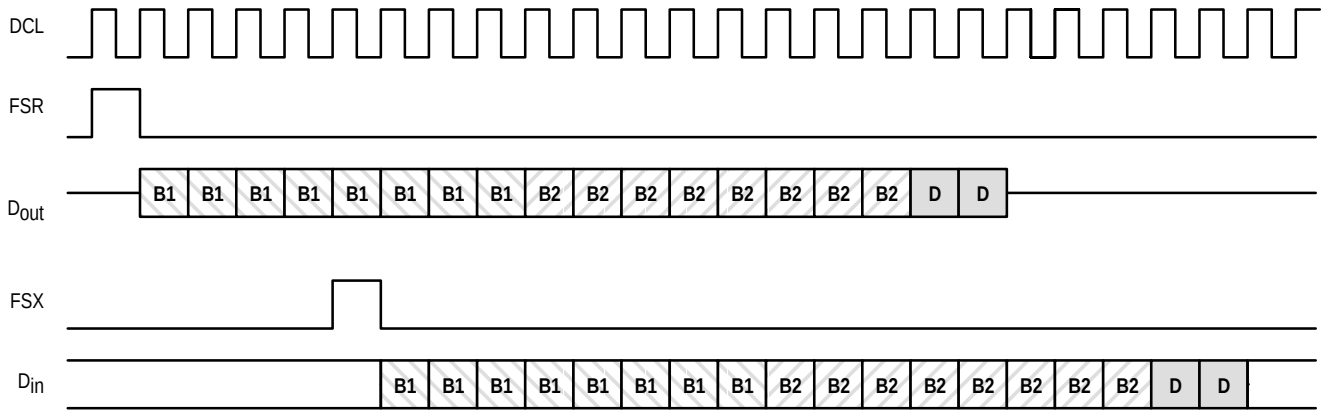


Figure 5–19. IDL2 Interface Timing in Short Frame Slave Mode, 8–Bit Frames

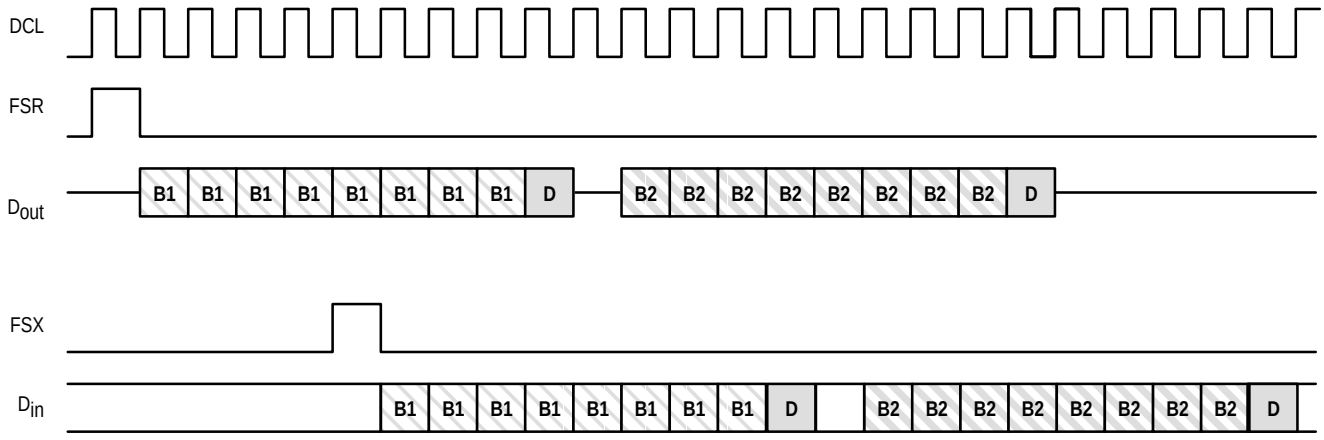


Figure 5–20. IDL2 Interface Timing in Short Frame Slave Mode, 10–Bit Frames

5.4.2 Long Frame Operation

When configured for long frame mode the 8 kHz frame sync is active during the 2B + D data transfer. The FSX pin is used to indicate frame synchronization for data input into the D_{in} pin for transmission onto the U–interface. The FSR pin is used to indicate frame synchronization for data recovered from the U–interface and output to the D_{out} pin. When configured for master mode, the MC145572 drives FSR and FSX simultaneously. When configured for IDL2 slave operation, the MC145572 FSX and FSR inputs can be driven independently. In slave mode, both FSX and FSR can be connected together so a single synchronization signal can be used to drive both inputs.

Figures 5–21a and 5–22a show typical data formats for long frame operation as a master and configured for 8–bit and 10–bit frame formats respectively. Figures 5–21b and 5–22b show typical data formats for long frame operation as a slave and configured for 8–bit and 10–bit frame formats respectively.

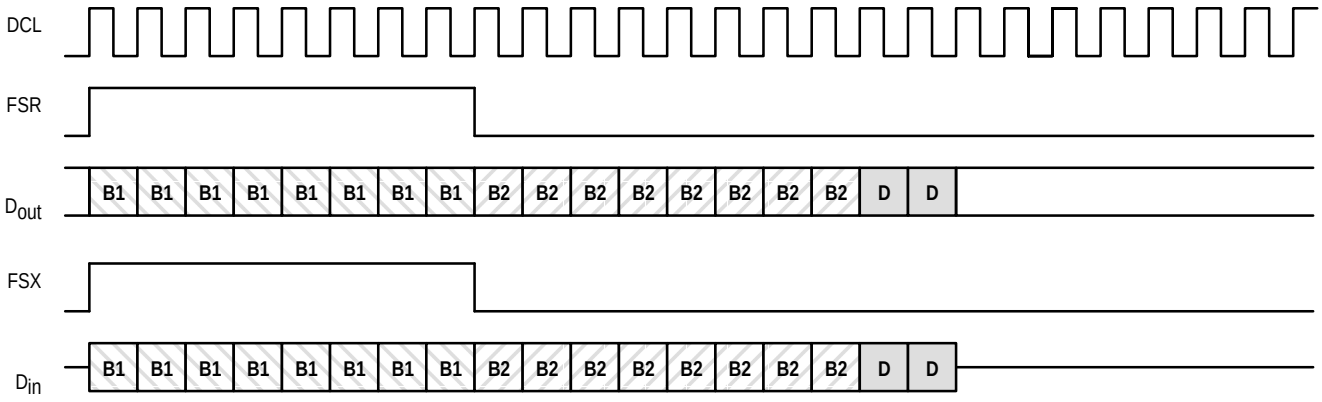


Figure 5–21a. 8–Bit Mode, Master

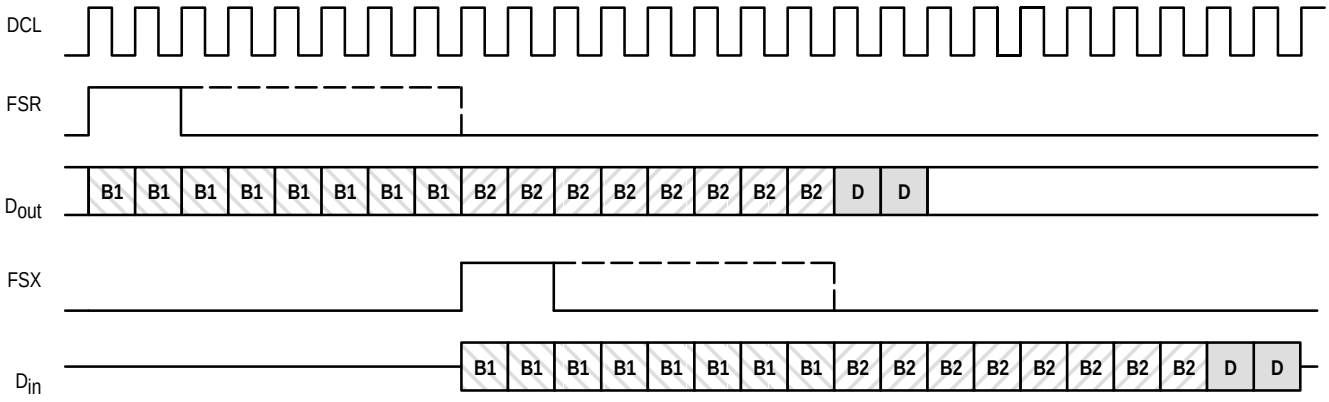


Figure 5–21b. 8–Bit Mode, Slave

Figure 5–21. IDL2 Interface Timing in Long Frame, 8–Bit Frames

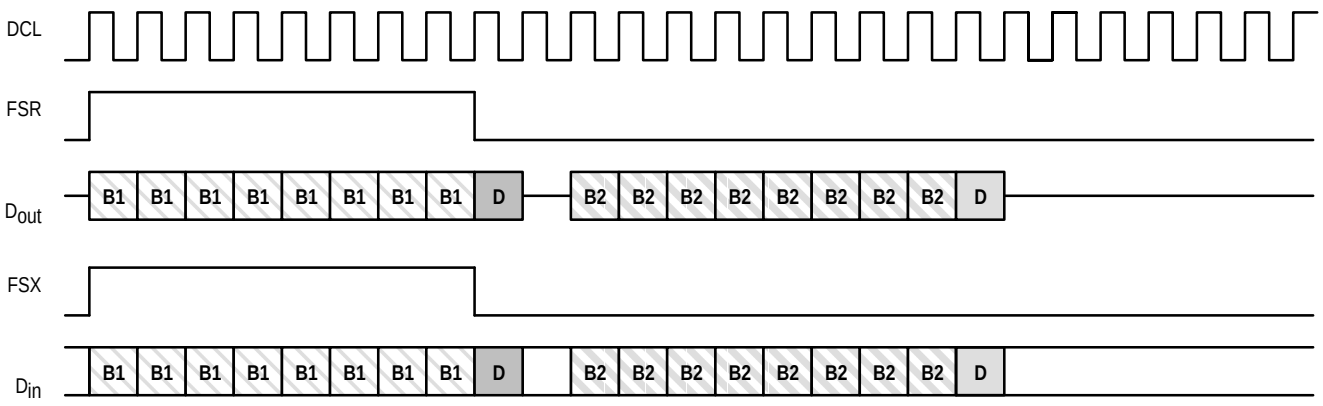


Figure 5–22a. 10–Bit Mode, Master

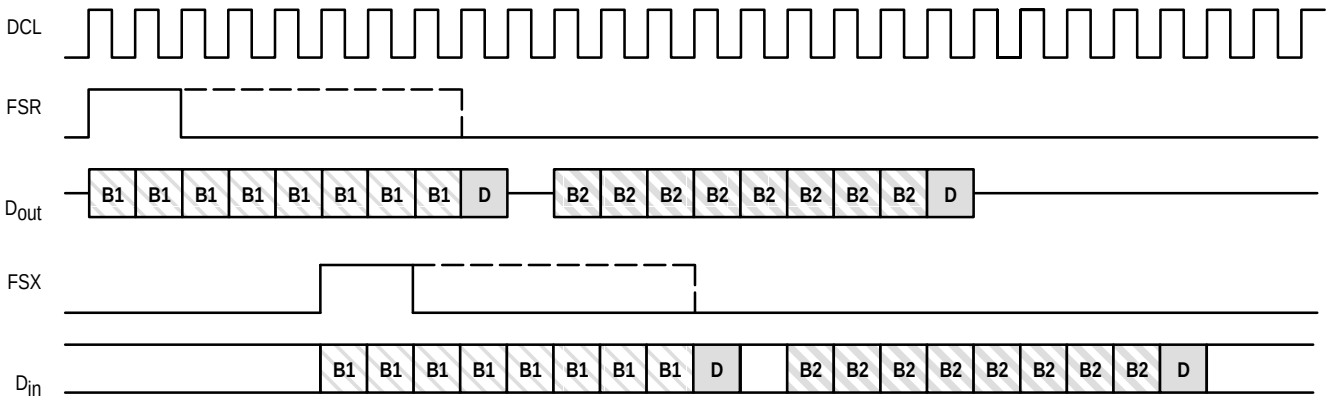


Figure 5–22b. 10–Bit Mode, Slave

Figure 5–22. IDL2 Interface Timing in Long Frame, 10–Bit Frames

5.4.3 GCI 2B + D Operation

By setting OR6(b3), GCI Mode Enable, to a '1' the IDL2 interface is configured to accept GCI interface timing. In this mode only 2B + D data is transferred between the MC145572 and the GCI interface. The other bits in the GCI frame are ignored. Four signal pins are available in this mode: DCL, FSC, D_{in}, and D_{out}. Control and status information for the MC145572 is provided through the Serial Control Port or the Parallel Port. DCL is a 2X bit clock, D_{in} accepts data from the IDL2 interface to be transmitted onto the U–interface, D_{out} transmits data received from the U–interface onto the IDL2 interface, and FSC is the 8 kHz frame synchronization pulse. D_{out} is driven only when 2B + D data is output from the MC145572. During all other bit times of the GCI frame D_{out} is high impedance. For applications having a multiplexed GCI frame structure, overlay register OR5 bits 2:0 are used to program the active GCI channel in the multiplex.

Figure 5–23 shows the GCI data format that is transferred over the IDL2 interface. If an application requires full GCI capability see **Section 8** for more details.

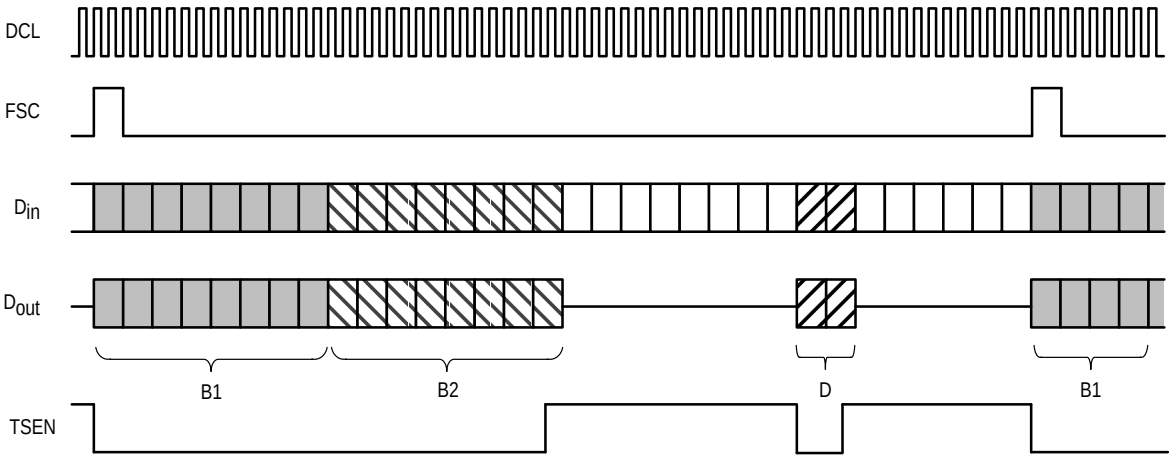


Figure 5–23. IDL2 GCI 2B+D Data Formats

5.4.4 Master and Slave Mode Operation

The MC145572 can be configured for IDL2 master or IDL2 slave operation independently of LT or NT configuration. A logic '1' selects IDL2 master operation and a logic '0' selects IDL2 slave operation.

When configured as an IDL2 slave, FSX and FSR can be independently driven by external circuitry. FSX and FSR must be synchronized to the clock applied to DCL. If there is only a single synchronization source, the FSR and FSX pins can be tied together and driven from a single source. In slave mode the IDL2 interface can accept an input clock at DCL between 512 kHz and 8.192 MHz.

As an IDL2 master the MC145572 drives FSX and FSR simultaneously so that the active high time of each signal coincides with each other. The 2B+D data transfer into D_{in} and out of D_{out} occurs simultaneously. For applications where only one output synchronization pulse is required either FSX or FSR can be used. As an IDL2 master the MC145572 outputs data clocks of 512 kHz, 2.048 MHz, and 2.56 MHz. The DCL clock rate is programmed by BR7(b2) and OR7(b4). See Table 5–4.

5.4.5 D Channel Port

When operated in MCU mode with the Serial Control Port enabled the MC145572 can be configured to have a separate data port for D channel data. The D channel port is available for short frame data format and GCI 2B+D data format. When the Parallel Control Port is used to access the MC145572 register set the D channel port is not available since the pins are assigned to the data bus of the parallel port. The D channel port is enabled by setting OR8(b0), D Channel Port Enable, to a '1'. After a hardware or software reset the D channel port is disabled. Figure 5–2 shows an LT mode configuration with the D channel port enabled.

The D channel port has three signals: DCH_{in} (D channel data input), DCH_{out} (D channel data output), and DCHCLK (D channel clock). When the D channel port is enabled, DCHCLK is always a clock output. The clock is a gated clock, based on whatever is on DCL. The clock occurs whenever the normal D1 and D2 bits would have occurred during the transfer taking place over D_{out} with respect to FSR. Internal buffering of the data received on DCH_{in} aligns the data for transmission onto the U–interface. DCH_{out} does not go high impedance.

When the D channel port is enabled, the D channel bits are diverted to the port, and the D_{out} pin on the IDL2 interface is high impedance during the D bit times. Data bits received at the IDL2 interface D_{in} pin are ignored during the D channel bit times. In timeslot assigner mode, the D channel bits are transferred at the time programmed in register OR2, D_{out} D Channel Timeslot Bits. Figures 5–24 through 5–26 show the D channel port timing.

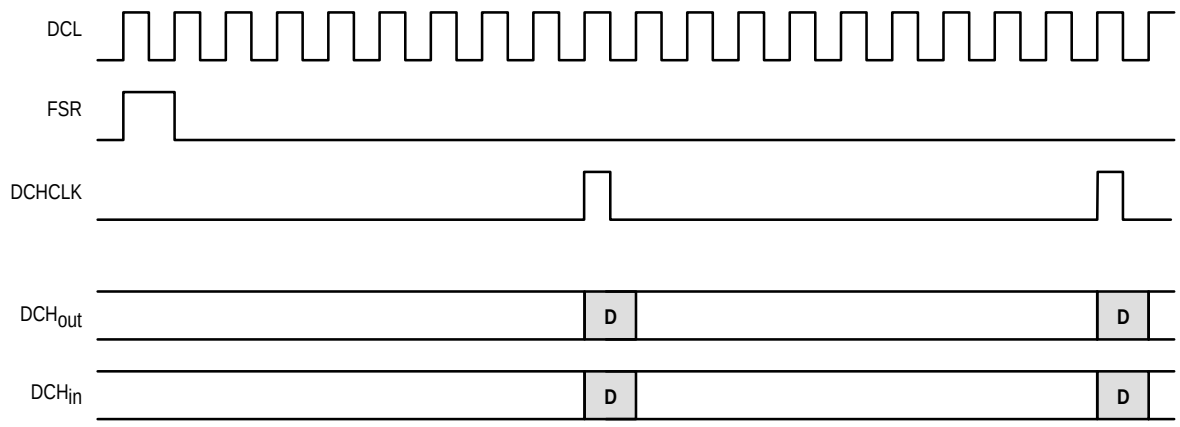


Figure 5–24. D Channel Port Timing, IDL2 10–Bit Frames

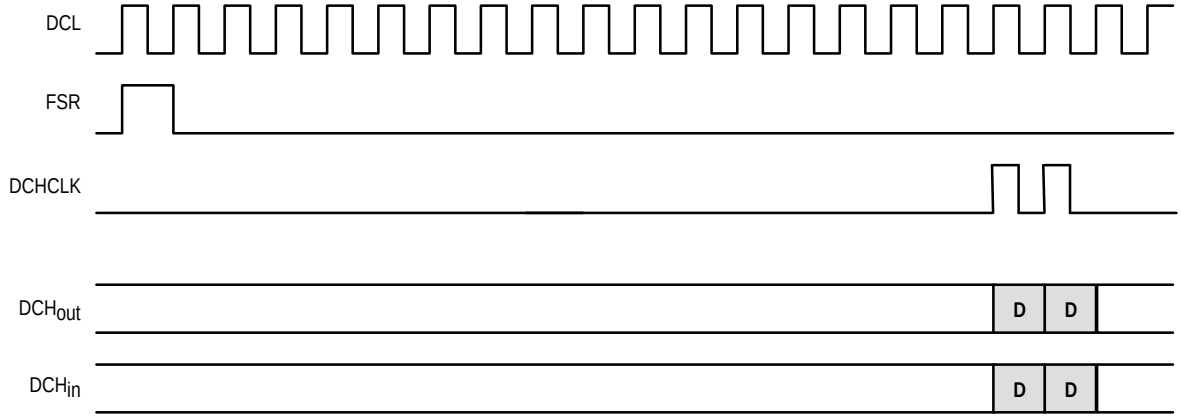


Figure 5–25. D Channel Port Timing, IDL2 8–Bit Frames

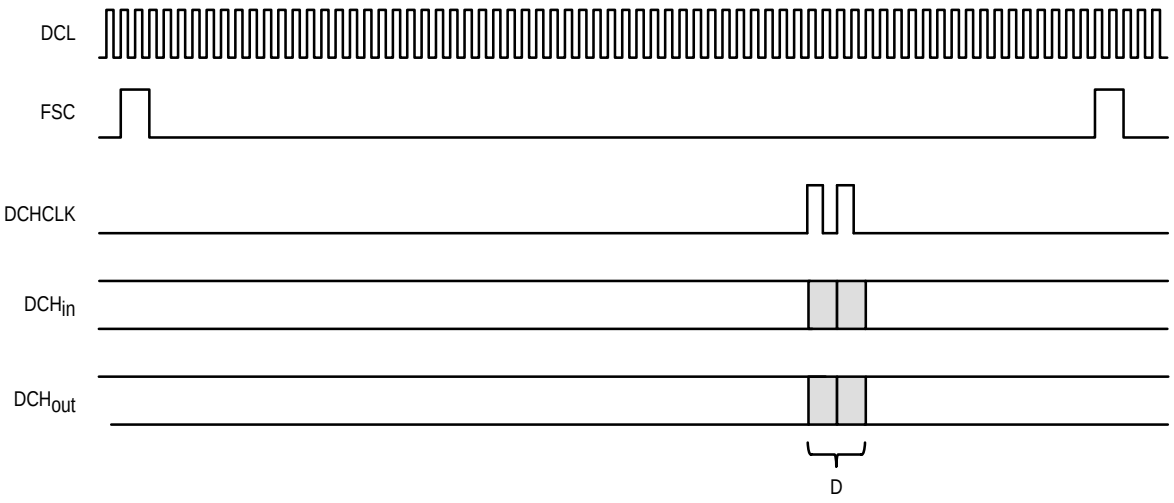


Figure 5–26. D Channel Port Timing, IDL2 GCI 2B+D Frames

5.4.6 Timeslot Assigner

The MC145572 has a timeslot assigner that can be used when configured for MCU mode. The timeslot assigner is enabled when one or more of OR6(b7, b6, or b5) are set to a '1'. The starting timeslot(s) are programmed into overlay registers OR0 – OR5. The B1, B2 and D channels are each independently programmable for both transmit and receive directions.

Timeslots are each 2 DCL clocks wide. Timeslot numbering starts from timeslot 0. Timeslot 0 occurs during the first two DCL clocks following FSX or FSR. DCL clocks are numbered starting from 0. Clock number 0 is the first DCL clock after the frame sync pulse FSX or FSR. Since FSX and FSR can occur at different times DCL clocks are counted referenced to either FSX or FSR depending on which data direction is being configured. The timeslot number is calculated by counting the DCL clocks after the appropriate frame sync where it is desired to place the start of the B or D channel timeslot. This DCL count is divided by two and the resulting value is written to the appropriate timeslot register.

The D channel data is always two contiguous DCL clocks or one timeslot in duration. B channel data is always eight contiguous DCL clocks or four timeslots in duration. B channel timeslots may be programmed to start in any timeslot though in normal applications B channel timeslots are programmed to start on every fourth timeslot or eighth DCL clock. Data is transferred between the MC145572 and the IDL2 interface only during B1, B2, or D channel timeslots that are enabled. When a B or D channel timeslot is disabled, data appearing at the D_{in} pin is ignored and the D_{out} pin is high impedance. Table 5–5 details the timeslot assigner registers in the overlay register set. See Figures 5–27 and 5–28 for timeslot format examples.

The register programming for Figure 5–27 is as follows:

OR0 = $04	OR3 = $00	OR6 = $E0
OR1 = $0B	OR4 = $08	OR7 = $20
OR2 = $01	OR5 = $0D	OR8 = $08

The register programming for Figure 5–28 is as follows:

OR0 = $00	OR6 = $50
OR2 = $0D	OR7 = $20
OR3 = $04	OR8 = $08
OR5 = $01	

The register programming for Figure 5–29 is as follows:

OR0 = $00	OR3 = $00	OR6 = $E0
OR1 = $0B	OR4 = $0B	OR7 = $00
OR2 = $08	OR5 = $08	OR8 = $09

Enabling the timeslot assigner over rides all other IDL2 frame formats with the exception of GCI 2B + D. In GCI 2B + D data format OR5 bits 2:0 are used to select the active GCI channel.

When the D channel port is enabled the corresponding D channel timeslot is not enabled on the IDL2 interface. Instead, the D channel data is transferred over the D channel port referenced to FSR as programmed in overlay registers OR2 or OR5. This is also true when IDL2 GCI 2B + D mode has been enabled. The D_{out} pin of the IDL2 interface is high impedance and data at D_{in} is ignored. Figure 5–29 gives an example of D channel port operation when the timeslot assigner is enabled.

Table 5–5. Timeslot Assigner Registers

OR0	D_{out} B1 Channel Timeslot Bits (7:0)							
OR1	D_{out} B2 Channel Timeslot Bits (7:0)							
OR2	D_{out} D Channel Timeslot Bits (7:0)							
OR3	D_{in} B1 Channel Timeslot Bits (7:0)							
OR4	D_{in} B2 Channel Timeslot Bits (7:0)							
OR5	D_{in} D Channel Timeslot Bits (7:0) and GCI Slot (2:0)							
OR6	TSA B1 Enable	TSA B2 Enable	TSA D Enable	GCI Select M4–BR0	GCI Mode Enable	Reserved	Reserved	Reserved

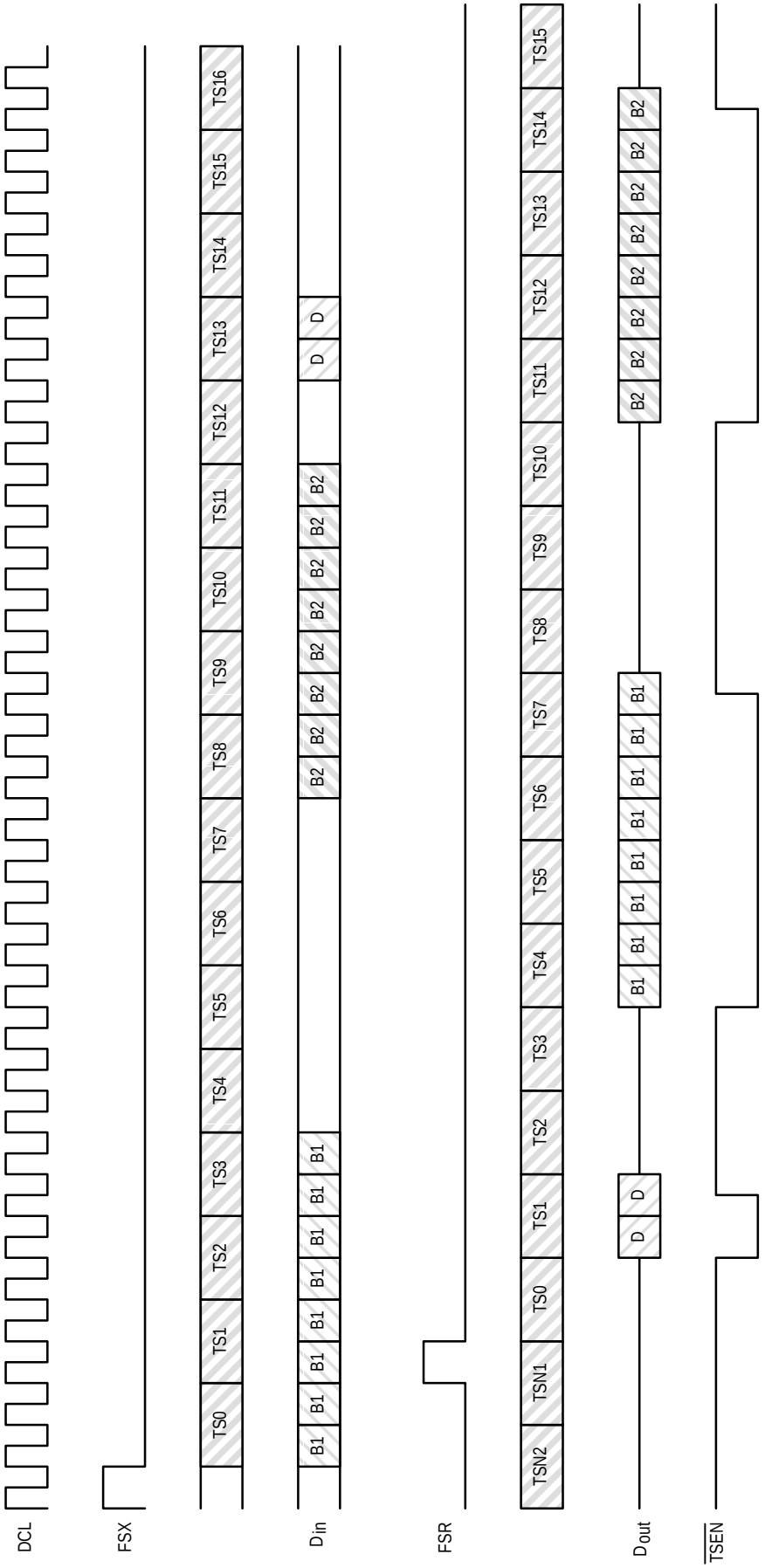


Figure 5–27. Timeslot Assigner Data Format Example

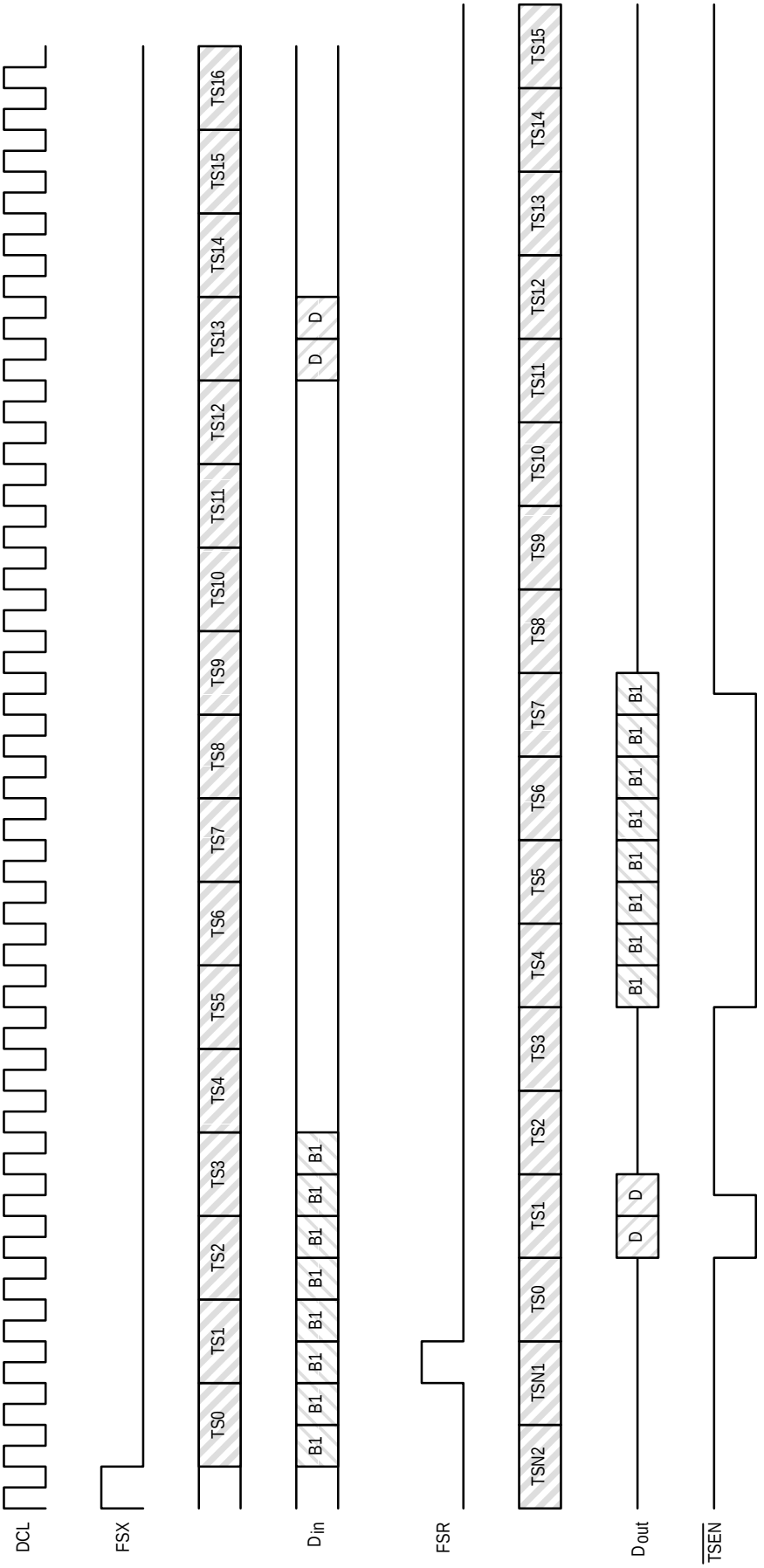


Figure 5–28. Timeslot Assigner Data Format Example, B2 Channel Not Enabled

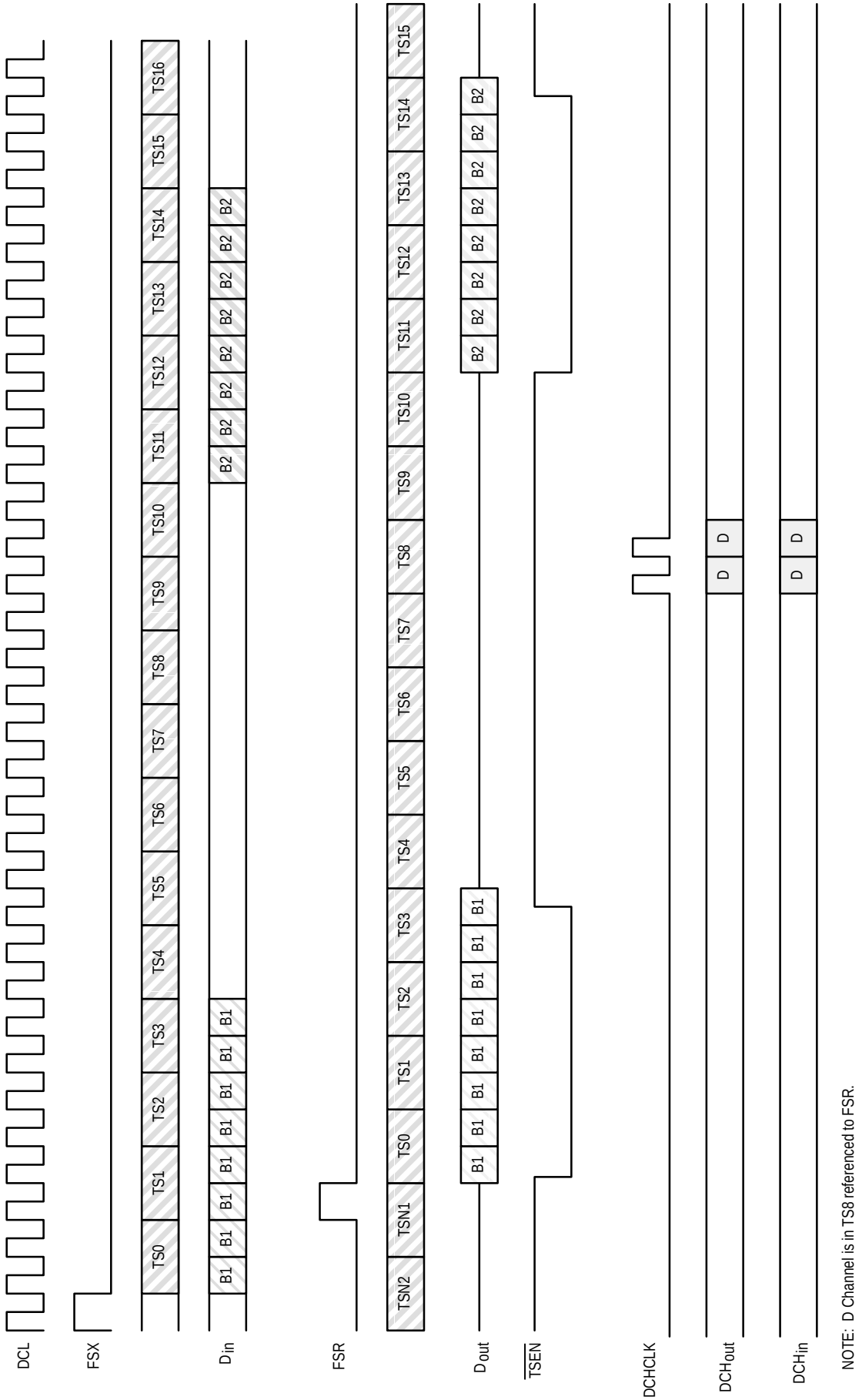


Figure 5–29. Timeslot Assigner Example with D Channel Port Enabled

5.4.7 Timeslot Selection

The MC145572, operating at a DCL clock of 4.096 MHz, allows up to 256 start times for data channels (see Table 5–6). Timeslot 0 starts immediately following the FSX/FSR pulse. Timeslot 1 is two DCL pulses later, counted from the rising edge.

Table 5–6. Maximum Number of Timeslots vs. DCL Frequency

DCL Frequency	Max Timeslot (Hex)	Max Timeslot (Decimal)
4.096 MHz	$FF	255
2.56 MHz	$9F	159
2.048 MHz	$7F	127
512 kHz	$1F	31

Figure 5–30 shows the relationship of the FSR and FSX pulses, DCL, and timeslot locations. Each timeslot is on a 2 clock boundary, and is named TS0 to TS*n* – 1, where *n* is the maximum number of timeslots for the current operating data clock. A B channel occupies four contiguous two bit timeslots. A D channel occupies a single two bit timeslot.

The following formula calculates the maximum number of timeslots for other values of DCL frequency.

$$\frac{f_{DCL}}{16\ kHz} = \text{Maximum Number of Timeslots}$$

B and D channel registers are programmed with the following formula:

B Register Value = TS*x*
D Register Value = TS*x*

Where the *x* of TS*x* is the value programmed into a register. All numbers are programmed in hex. Any B channel must be assigned to a timeslot at or before TS*n* – 4. Where TS*n* – 1 is the maximum timeslot number for the current operating data clock. The three timeslots following any B channel assignment are reserved for that B channel and may not be assigned to any other data channel.

Registers OR0 – OR5 are programmed in the above fashion.

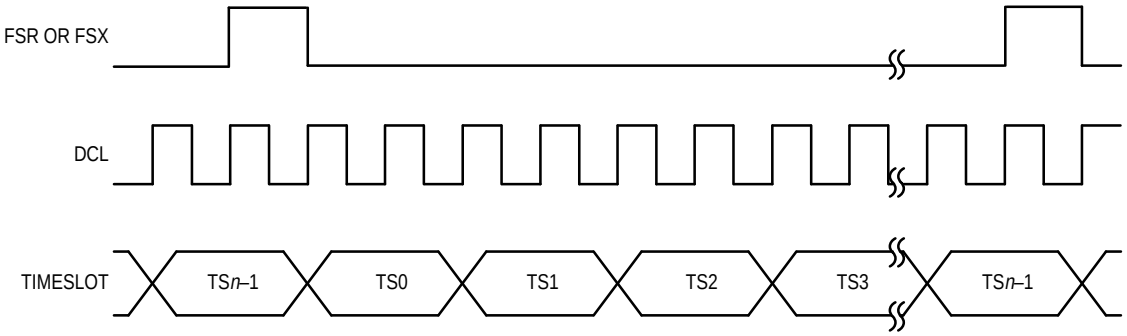


Figure 5–30. Timeslot Numbering

NOTE

If timeslot assignment mode is enabled via OR6 b(7), b(6), or b(5), then the IDL2 8/10 control bit is ignored and B channel and D channel data is placed according to OR0 – OR5. The TSEN function is available when the timeslot assigner is enabled.

5.4.8 IDL2 2B + D Data Alignment to U-Interface Superframe

The MC145572 provides signals that indicate the relationship between the data transferred over the IDL2 interface and where that data is positioned in the U–interface superframe. In IDL2 short frame and long frame operation, the SFAX and SFAR pins are used to indicate the IDL2 2B + D data frame that corresponds to the first 2B + D block in basic frame 1 of the U–interface superframe. This feature is enabled by setting OR8(b1), SFAX/SFAR ENABLE to a '1' when the MC145572 is configured for IDL2 operation.

SFAX provides superframe alignment timing for data transmitted onto the U–interface. It is active during the IDL2 frame that corresponds to the 2B + D data transmitted at the start of basic frame 1 on the U–interface. In NT mode SFAX is always an output. In LT mode SFAX defaults to an input and is used to force alignment of the outgoing superframe as well as indicating transfer of the first 2B + D frame of the U–interface basic frame 1 into D_{in} of the IDL2 interface. When in LT mode setting OR8(b5), SFAX Output Enable, to a '1' configures SFAX as an output and indicates transfer of the first 2B + D frame of the U–interface basic frame 1 into D_{in} of the IDL2 interface. When SFAX is not enabled as an input the MC145572 selects the starting point of the transmitted superframe when in LT mode.

SFAR provides superframe alignment timing for data received form the U–interface. It is active during the IDL2 frame that outputs the 2B + D data from the MC145572 that arrived at the start of basic frame 1 on the U–interface. SFAR is always an output when enabled.

When configured for GCI 2B + D operation the FSC signal is used to indicate superframe alignment.

The superframe alignment signal(s) occur once every 96 IDL2 or GCI frames. Since frames are 125 μs in duration this corresponds to 12 ms (96x125 μs) which is the duration of a U–interface superframe.

5.4.8.1 IDL2 SHORT FRAME MODE SUPERFRAME ALIGNMENT

In IDL2 short frame format, SFAX and SFAR indicate the IDL2 frame corresponding to the first 2B + D block in the U–interface superframe by pulsing high for one DCL clock time. This occurs immediately following the IDL2 frame syncs FSX and FSR (see Figures 5–31a and 5–31a). When configured as an input SFAX must be driven high for the DCL clock period immediately following FSX, and it is sampled on the falling edge of DCL.

5.4.8.2 IDL2 LONG FRAME MODE SUPERFRAME ALIGNMENT

In IDL2 long frame format SFAX and SFAR indicate the IDL2 frame corresponding to the first 2B + D block in the U–interface superframe by pulsing high for the duration of FSX and SFR respectively (see Figures 5–31b and 5–32b).

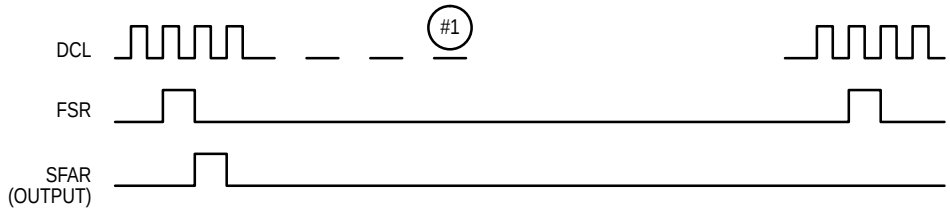


Figure 5–31a. Short Frame Mode

The #1, circled, indicates which 2B+D transfer is the first of the superframe. The clock, DCL, is continuous.

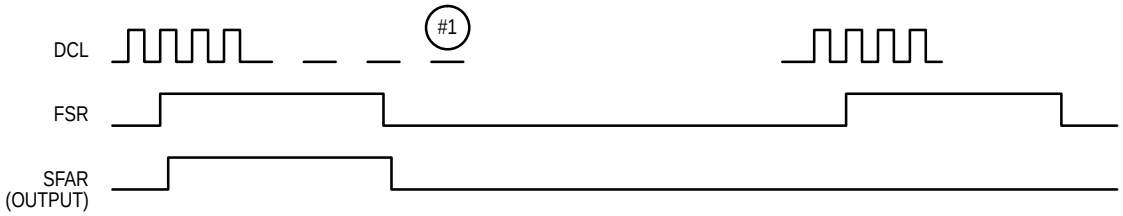


Figure 31b. Long Frame Mode

Figure 5–31. SFAR Timing

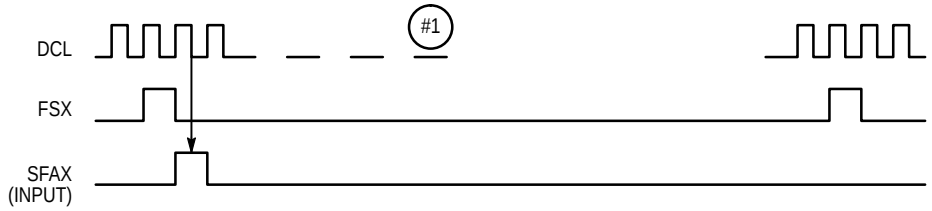


Figure 5–32a. Short Frame Mode

The #1, circled, indicates which 2B+D transfer is the first of the superframe. The clock, DCL, is continuous.

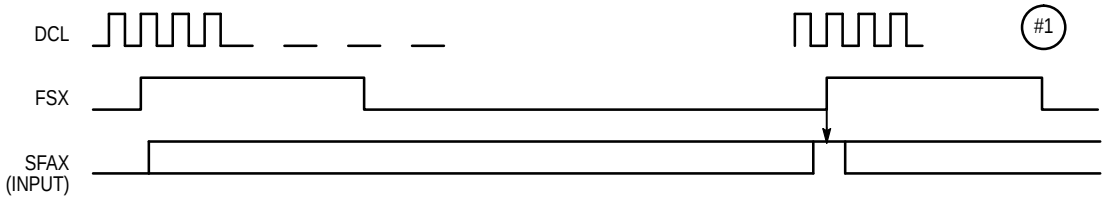


Figure 5–32b. Long Frame Mode

Figure 5–32. SFAX Timing

5.4.8.3 GCI 2B+D Mode Superframe Alignment

When configured for IDL2 GCI 2B + D data format, OR6(b3) = 1, the MC145572 uses the FSC signal to indicate superframe alignment. Inputs on SFAX are ignored.

In LT mode, when the MC145572 is configured as an IDL2 slave the FSC pin is used to force alignment of the transmitted U–interface superframe. Normally, the FSC pulse is two DCL clocks in duration. The transmit superframe alignment is set by driving FSC with a one DCL clock wide pulse once every 96 GCI frames. The 2B + D data read into the D_{in} pin corresponding to the single clock wide FSC is the first 2B + D frame transmitted onto the U–interface. If superframe alignment is not input to FSC the MC145572 aligns the outgoing U–interface superframe alignment (see Figure 5–33).

When configured for master mode and either LT or NT operation reception of the first 2B + D data of the U–interface superframe is indicated by outputting a FSC pulse that is one DCL clock wide. This happens once every 96 GCI frames.

In NT mode, IDL2 slave operation any superframe alignment information that may be present on FSC is ignored. ANSI T1.601 defines a 60 ±2 baud turnaround at the NT. This means that the transmitted superframe sync word in the NT configured MC145572 is delayed 60 bauds or 750 μs from the received superframe sync word. On an 18,000 foot loop the total propagation delay in both directions is approximately 6 bauds or 39 μs. This gives a worse case offset between the transmitted sync word at the LT and the receive sync word at the NT of approximately 790 μs or 6 IDL frames.

5.4.9 Initial State of B1 and B2 Channels

Upon initial activation the MC145572 transmits all 1's in the B and D channels onto the U–interface. Data transparency is enabled by setting Customer Enable (NR2(b0)) when the M4 channel act bit is received as a '1'. If the Verified `act/dea` mode is enabled, see BR9(b5,b4) then data transparency onto the U–interface is automatically enabled when the M4 channel `act` bit is received as a "1".

5.5 FRAME SYNC TO U-INTERFACE PROPAGATION DELAYS

Due to the MC145572 having separate FIFOs for receive and transmit directions, there is a propagation delay between data being input into the IDL2 or GCI interfaces and that same data being transmitted onto the U–interface. Likewise, there is a delay between when data is received at the U–interface and is transmitted onto the IDL2 or GCI interfaces. Table 5–5 gives the minimum and maximum delays for both NT and LT modes of operation. For any given activation the delay remains fixed but the propagation delay through the MC145572 will vary from activation to activation.

Table 5–7. FIFO Delays Through the MC145572

Delay Path	Min	Max	Units
NT Mode FSX to U–Interface transmission delay	196	315	us
NT Mode U–Interface to FSR transmission delay2	281	400	us
LT Mode FSX to U–Interface transmission delay	184	328	us
LT Mode U–Interface to FSR transmission delay	281	400	us

NOTE

The total end–to–end delay is the sum of the transmit FIFO delay in the originating transceiver and the receive FIFO delay at the destination transceiver.

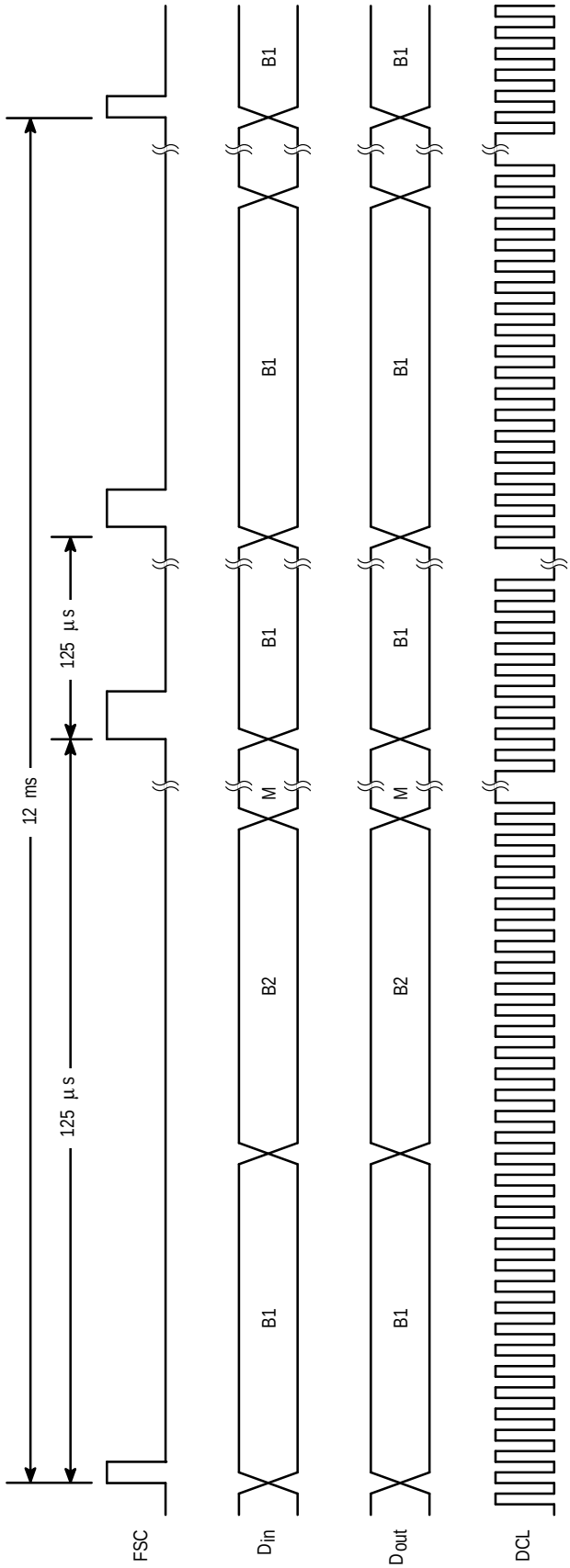


Figure 5–33. IDL2 GCI 2B+D Format Superframe Alignment Signal

5.6 LOOPBACKS

The MC145572 U–interface transceiver supports four different loopback types, each having various modes. The four types are: 1) U–Interface Loopback, 2) IDL2 Interface Loopback, 3) Superframe Framer–to–Deframer Loopback, and 4) External Analog Loopback. Each of these loopback modes is selected by setting bits in the appropriate register(s). Any combination of loopbacks may be invoked, including simultaneous loopbacks toward the U–interface and toward the IDL2 Interface. These loopbacks are available as transparent or non–transparent. “Transparent” means that a loopback passes the data on through to the other side as well as looping it back and “non–transparent” means that the data is blocked from being passed downstream and is replaced with the idle code (all 1s).

5.6.1 U-Interface Loopback

A U–Interface Loopback configuration is shown in Figure 5–34. As the shaded portion of the block diagram shows, this loopback mode exercises virtually the entire U–interface transceiver. 2B1Q symbols are received from the far end transmitter, recovered, passed through the IDL2 Interface block, and transmitted back to the far end receiver.

The four most significant bits of BR6 control the U–Interface Loopback modes. The loopback occurs in the IDL2 Interface section of the MC145572. Data appearing at the D_{in} pin is ignored (i.e., not transmitted onto the U–interface). By setting U–loop Transparent (BR6(b4)), to ‘1’, the loopback is made transparent and the D_{out} pin is enabled permitting transfer of recovered data onto the IDL2 Interface. When U–loop Transparent (BR6(b4)), is reset to ‘0’, the B and D channels at the D_{out} pin are forced to idle 1s when a loopback is enabled. If IDL2 Invert (BR7(b4)) is set to ‘1’, then the B and D channels at the D_{out} pin idle at all 0s.

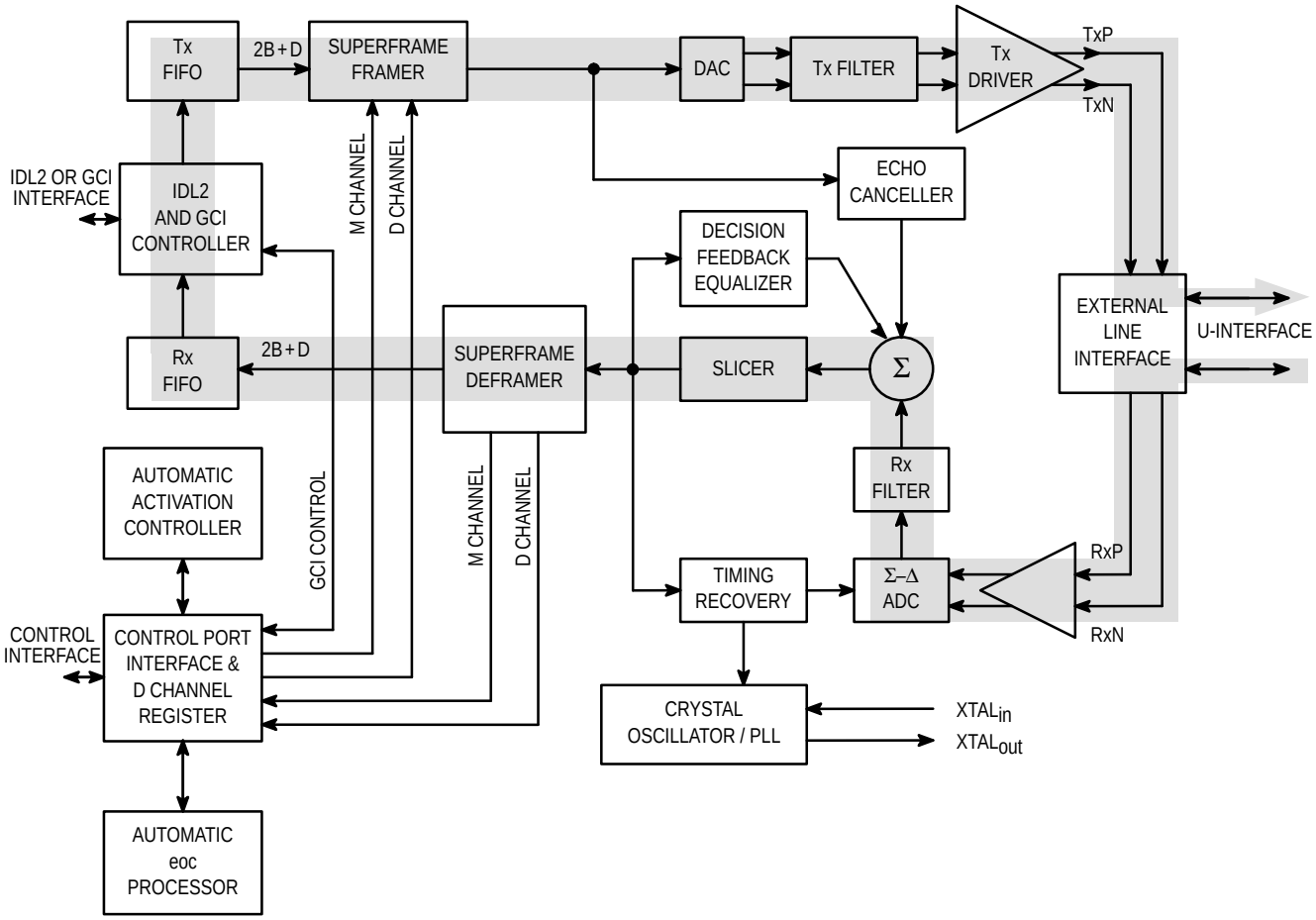


Figure 5–34. U–Interface Loopback Block Diagram

The U–Interface Loopback is selected by setting one or more of U–loop B1, U–loop B2, or U–loop 2B+D (BR6(b7:b5)) to ‘1’. To enable loopback of B1 channel data to the U–interface, U–loop B1 (BR6(b7)) is set to ‘1’. To enable loopback of B2 channel data to the U–interface, U–loop B2 (BR6(b6)) is set to ‘1’. To enable loopback of 2B+D data to the U–interface, U–loop 2B+D (BR6(b5)) is set to ‘1’. The 2B+D loopback overrides any B1 or B2 channel loopback that has been enabled. When the Automatic eoc Processor in the MC145572 is enabled, the logical OR of loopback modes enabled by the Automatic eoc Processor and loopback modes selected in BR6 are enabled. As a result, the external microcontroller can always enable a loopback whether the U–interface transceiver is operated with the Automatic eoc Processor or not.

When the U–interface transceiver is operating without the Automatic eoc Processor, loopback modes can be disabled by setting to 1 and then resetting to 0 the Return to Normal bit, NR0(b0). This clears all bits in BR6 and clears the `crc` Corrupt control bit, BR8(b3). The loopback modes can also be cleared by resetting the appropriate bits in BR6 to 0.

5.6.2 IDL2 Interface Loopback

IDL2 Interface Loopback is shown in Figure 5–35. As the shaded portion of the block diagram shows, this loopback mode takes B and D channel data in at the IDL Rx pin and sends the same data back out the IDL2 Tx pin.

The four least significant bits of BR6 control the IDL2 Interface loopback modes. The loopback occurs in the IDL2 Interface block of the MC145572. By setting IDL2–loop Transparent (BR6(b0)) to ‘1’, the loopback is made transparent and the data input on the D_{in} pin is transmitted onto the U–interface. When IDL2–Loop Transparent (BR6(b0)) is reset to ‘0’, the data transmitted on the U–interface is forced to idle 1s when an IDL2 Interface loopback mode is enabled.

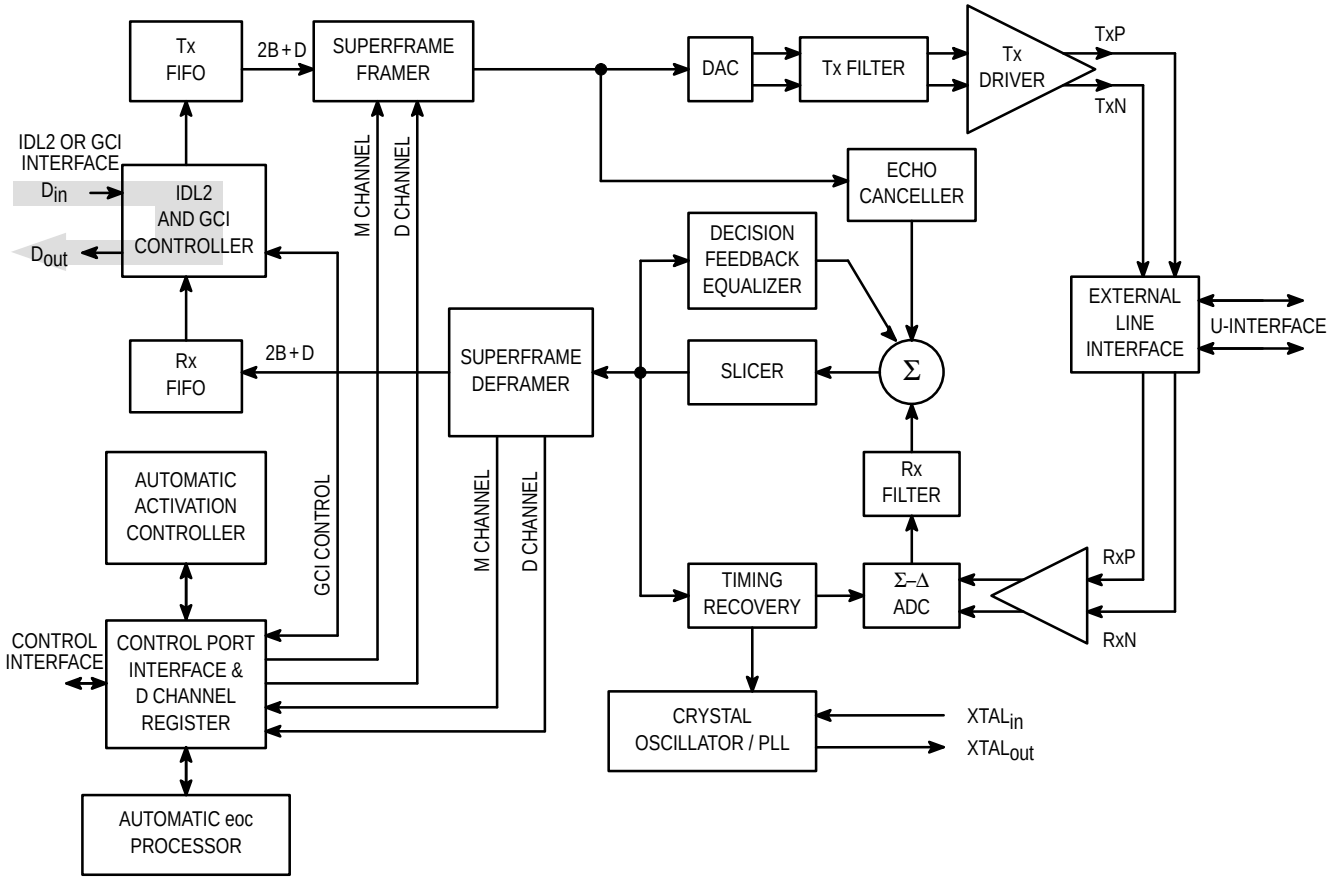


Figure 5–35. IDL2 Interface Loopback Block Diagram

An IDL2 Interface Loopback is selected by setting one or more of the registers IDL2–loop B1, IDL2–loop B2, or IDL2–loop 2B+D (BR6(b3:b1)) to ‘1’. To enable loop–back of B1 channel data to the IDL2 Interface, IDL2–loop B1 (BR6(b3)) is set to ‘1’. To enable loopback of B2 channel data to the IDL2 Interface, IDL2–loop B2 (BR6(b2)) is set to ‘1’. To enable loopback of 2B+D data to the IDL2 Interface, IDL2–loop 2B+D (BR6(b1)) is set to ‘1’. The 2B+D loopback mode overrides any B1 or B2 channel loopback that has been enabled. IDL2 Interface Loopback modes are independent of U–Interface Loopback modes and, as a result, these loopback modes can be operational simultaneously.

IDL2 Interface Loopback modes can be disabled by setting to ‘1’ and then resetting to ‘0’ the Return to Normal bit (NR0(b0)). This clears all bits in BR6 and the `crc` Corrupt control bit (BR8(b3)). The IDL2 Interface loopback modes can also be cleared by resetting the appropriate bits in BR6 to 0.

5.6.3 Superframe Framer-to-Deframer Loopback

Superframe Framer–to–Deframer Loopback is shown in Figure 5–36. As the shaded portion of the block diagram shows, this loopback mode takes B and D channel data in at the D_{in} pin and M channel data via the SCP, performs all of the superframe framing and subsequent deframing functions, and sends the same data back out the D_{out} pin and SCP. This loopback mode is intended primarily for diagnostic purposes.

Register BR14(b4) controls the Superframe Framer–to–Deframer Loopback mode. The loopback of B, D, and M channel data occurs between the output of the Superframe Framer block of the MC145572 and the Superframe Deframer input. In this loopback mode, the Tx Driver is disabled. A ‘1’ written to BR14(b4) enables the mode and a ‘0’ disables the mode. In addition, Match Scrambler (BR8(b2)) and Receive Window Disable (BR8(b1)) should be set to ‘1’.

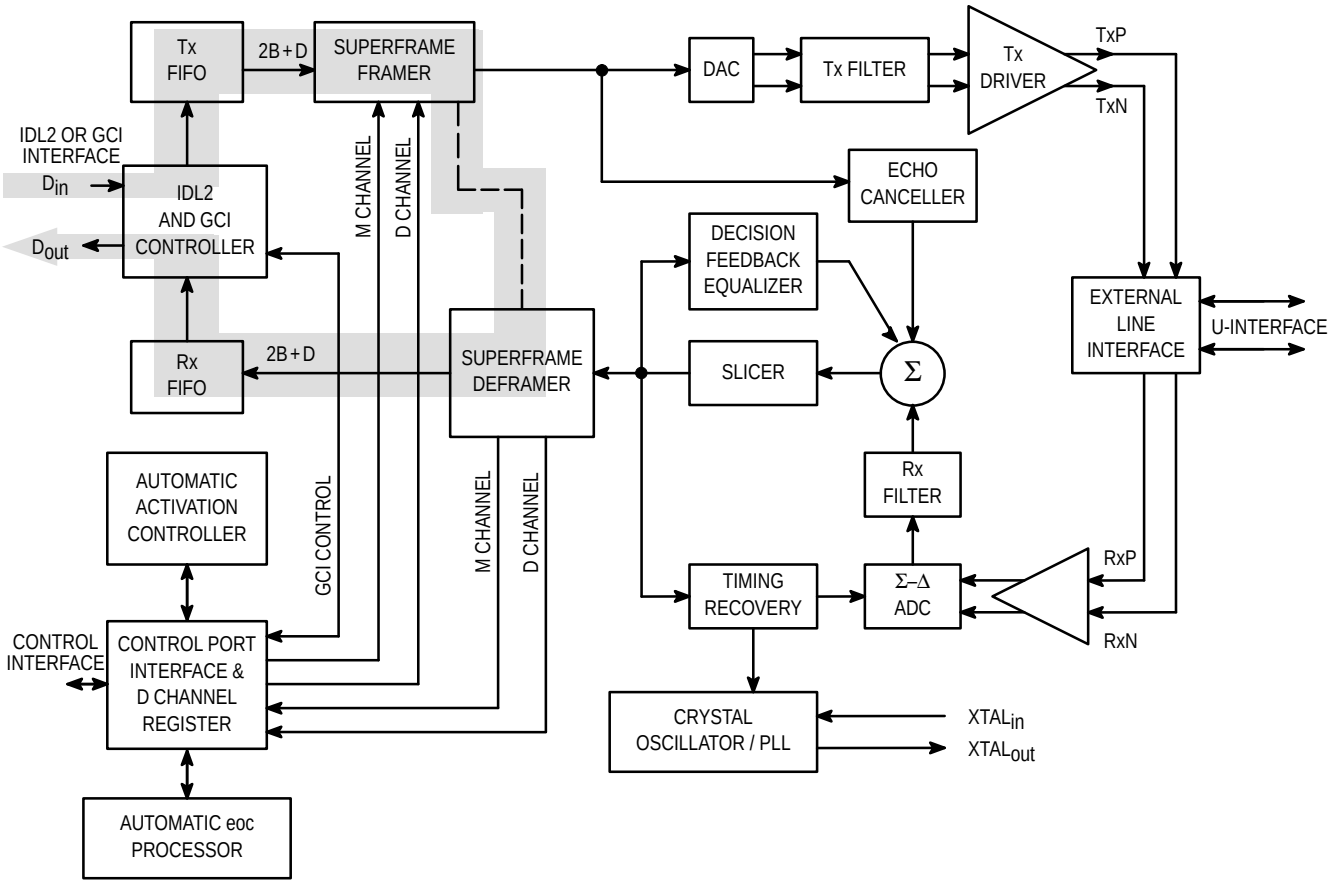


Figure 5–36. Superframe Framer–to–Deframer Loopback Block Diagram

The procedure to enable the Superframe Framer–to–Deframer Loopback for an NT configured U–interface transceiver follows with all numbers given in hexadecimal:

```
NR0 = 8       Assert reset, not required.
NR0 = 0       Deassert reset, not required.
BR14 = 10     Enable Framer–to–Deframer Loopback, Enable CLKs. Enable
              CLKs is optional and enables SYSCLK to display an eye pattern.
BR8 = B7      Match Polynomials, Receive Window Disable, set NT/LT Invert,
              transmit Frame Control state SN3.
BR12 = 89     Control Steer, Hold Activation State, Force Linkup.
BR13 = 0C     Accumulate DFE Output and Enable DFE Updates. Disable echo
              cancellers.
NR2 = 1       Set Customer Enable.
```

The procedure to enable the Superframe Framer–to–Deframer Loopback for an LT configured U–interface transceiver follows with all numbers given in hexadecimal:

```
NR0 = 8       Assert reset, not required.
NR0 = 0       Deassert reset, not required.
BR14 = 10     Enable Framer–to–Deframer Loopback, Enable CLKs. Enable CLKs is
              optional and enables SYSCLK to display an eye pattern.
BR8 = B6      Match Polynomials, Receive Window Disable, do not set NT/LT In
              vert, transmit Frame Control state SL3.
BR12 = 89     Control Steer, Hold Activation State, Force Linkup.
BR13 = 0C     Accumulate DFE Output and Enable DFE Updates. Disable echo
              cancellers.
NR2 = 1       Set Customer Enable.
```

5.6.4 External Analog Loopback

External Analog Loopback is shown in Figure 5–37. As the shaded portion of the block diagram shows, this loopback mode takes B and D channel data in at the D_{in} pin and transmits the data out the Tx Driver pins. The 2B1Q signal passes through the external line interface circuitry and back into the receiver input pins. The signal is then recovered and sent out the D_{out} pin. It is recommended that TIP and RING be physically disconnected from the U–interface twisted wire pair. This is perhaps the easiest way to assure that the transmitted signal is not properly terminated, resulting in very little trans–hybrid loss. Do not use a 135 ohm termination resistor.

OR7 bits 6 and 7 can be used to modify operation of the analog loopback. In order to use them, they must be set prior to setting OR9 (b5). These bits must be cleared after the analog loopback is turned off. These bits are cleared after any reset. See OR7 description for more details.

Since the entire 2B1Q superframe is being looped back, loopback data includes the 2B+D channels and all of the M channels. For instance, data written by an external microcontroller to the eoc, M4, and M5/M6 registers (R6, BR0, and BR2), is looped back and can be read from the eoc, M4, and M5/M6 registers (R6, BR1, and BR3).

The procedure to enable the External Analog Loopback follows with all numbers given in hexadecimal. Analog loopback is released by clearing OR9 (b5).

```
NR0 = 8       Assert reset.
NR0 = 0       Deassert reset.
BR10 = 01     Select Init Group Register Set.
OR9 = 20      Enable Analog Loopback.
BR10 = 00     Deselect INIT Group Register Set.
```

When activation is indicated by NR1 reading as 0B then:

```
NR2 = 1       Set Customer Enable.
```

Once activation occurs the following information should be available from the MC145572:

BR12+BR13 should stabilize, preferably with BR12 = 00 and BR13 typically less than hexadecimal C0.

BR3(b0) should be set to 1.

BR11 should be 46 or 47.

5.6.5 Releasing Analog Loopback

To release the MC145572 from analog loopback:

BR10 = 01

OR9 = 00

BR10 = 00

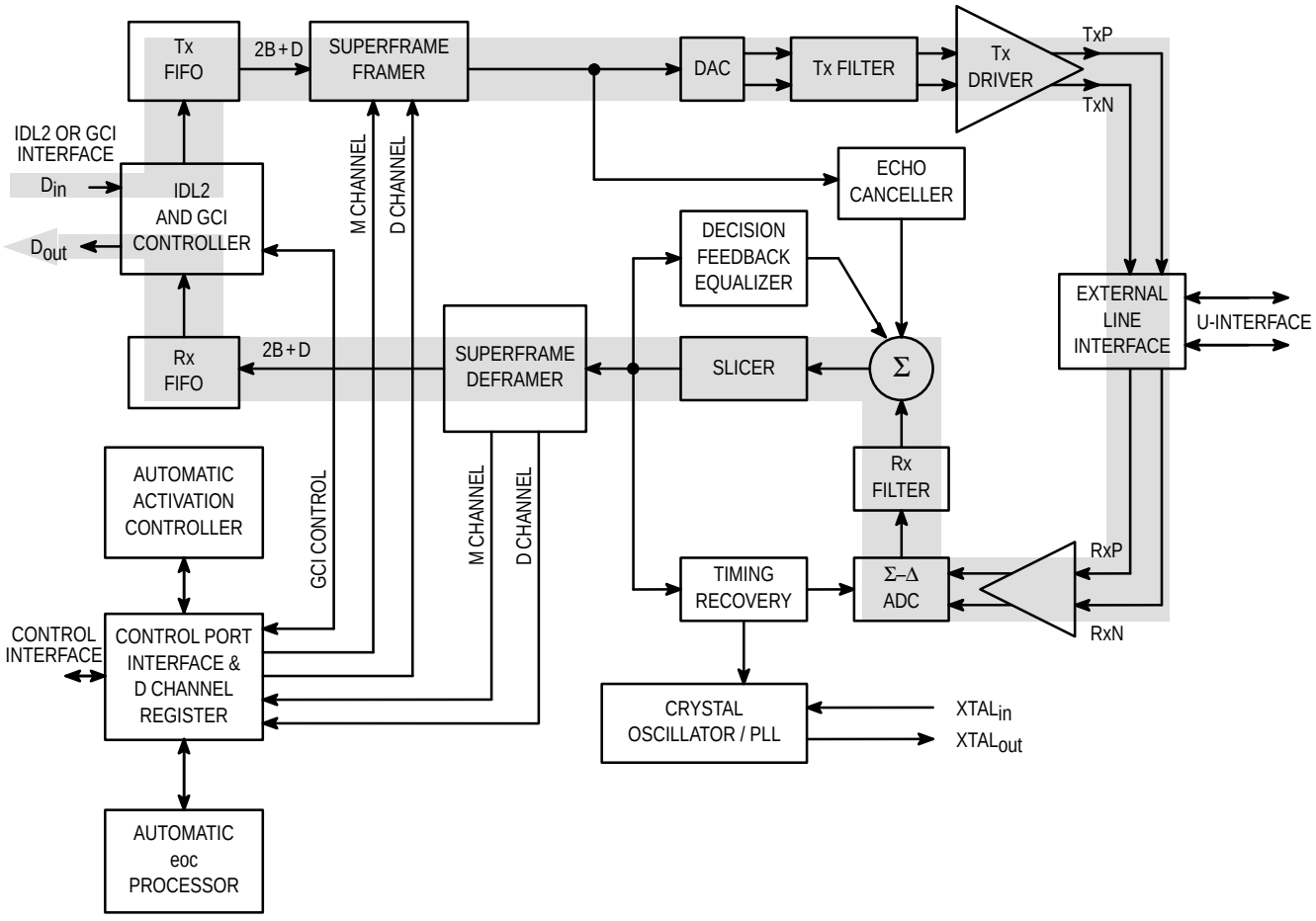


Figure 5–37. External Analog Loopback Block Diagram

Table 5–8. 2B1Q Line Interface Component Values

Component	Description (Figure 5–38a)	Description (Figure 5–38b)
C1	0.012 μF, 16 V, 10%, ceramic NPO, polystyrene, or polypropylene capacitor. See **Appendix E** for how to calculate this value.	0.012 μF, 16 V, 10%, ceramic NPO, polystyrene, or polypropylene capacitor. See **Appendix E** for how to calculate this value.
C2	1.0 μF, 200 V, 10%, low distortion capacitor	1.0 μF, 200 V, 10%, low distortion capacitor
R1, R2	35 Ω, 1%, metal film or other high quality low distortion resistor. See **Appendix E** for how to calculate this value.	32 Ω, 1%, metal film or other high quality low distortion resistor. See **Appendix E** for how to calculate this value.
R3, R4	Not Used	7.5 Ω, positive temperature coefficient resistor, polyswitch TR600–150.
D1, D2	MMBD7000 LT1	MMBD7000 LT1
D3, D4	IN5232B 5.6 V Zener	IN5232B 5.6 V Zener
D5	Transient voltage suppressor, TECCOR P1300EA70.	Transient voltage suppressor, TECCOR P1300EA70.
T1	Pulse engineering PE68628.	Pulse engineering PE68628.

NOTES:
1. Pulse transformer, 1:1.25 turns ratio. See **Appendix B** for sourcing and specification information. Dielectric isolation must accept highest power cross voltage and highest lightning surge test voltage to be applied to Tip and Ring.
2. Pulse transformers are available from several manufacturers.
3. Diodes D1, D2, D3, and D4 can be MMBD7000 LT1. It is not required that D3, D4 be zener diodes.
4. 22 Ω 5% resistors can be connected at RxN and RxP for additional surge protection, if desired.

5.7 2B1Q LINE INTERFACE

Figure 5–38 shows the suggested 2B1Q interface networks for connection to the U–interface and component specifications are shown in Table 5–8. Sources and specifications for the 2B1Q line interface transformer can be found in Appendix B.

There are two basic topologies for the 2B1Q line interface. The first topology does not have resistors between the transformer and Tip and the transformer and Ring. The second topology does have these resistors. By using positive temperature coefficient resistors on the line side of the transformer electrical safety design requirements may be more easily implemented. A positive temperature coefficient resistor greatly increases its resistance value when it heats up due to the application of external voltages across Tip and Ring. Effectively, the positive temperature coefficient resistor creates a high impedance thereby limiting current flow between Tip and Ring when the protection diodes turn on.

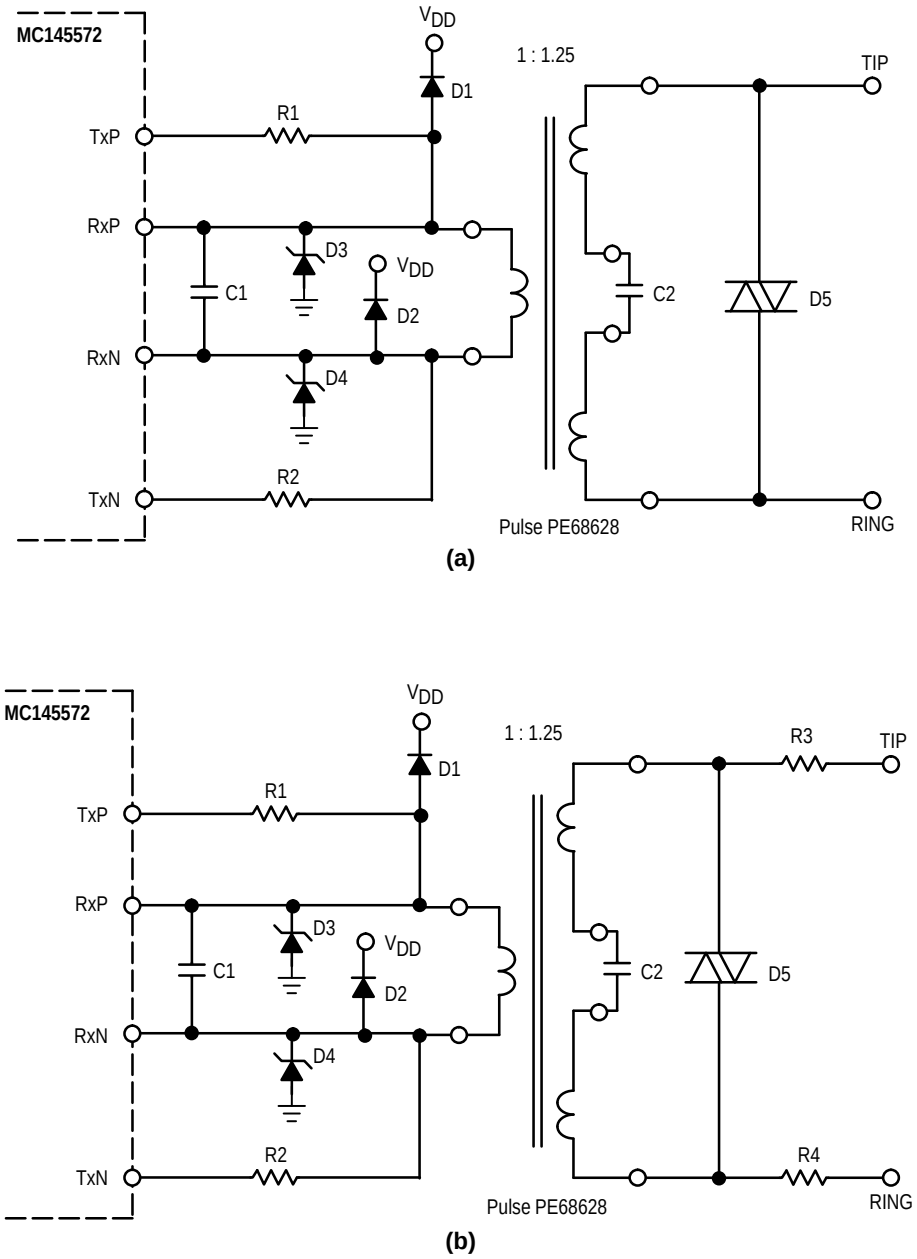


Figure 5–38. Typical 2B1Q Line Interface Schematic

NOTE

Motorola continues to qualify several third party sources for the 2B1Q line interface transformer. Contact your local Motorola representative or the Motorola factory applications staff for the latest information regarding component sourcing.

5.8 CRYSTAL OSCILLATOR

In the LT mode an internal PLL synchronizes a voltage controlled 20.48 MHz crystal oscillator to an 8 kHz reference frequency supplied by the switching equipment. This phase–locked clock assures that the transmitted 2B1Q signal is synchronized to the frequency reference supplied at the FREQREF pin. In addition, the very low frequency response (1 Hz) of the internal PLL loop filter limits jitter present in the frequency reference.

In the NT mode, the MC145572 synchronizes its DCL clock output pin to the recovered timing from the U–interface. This clock is available at 512 kHz, 2.048 MHz and 2.56 MHz. Frequency adjustments are also made to the 20.48 MHz oscillator but it is not precisely locked to the recovered 2B1Q signal at all times. This means that the BUFXTAL OUT pin cannot be used as a master clock source in applications that require a synchronized clock. In NT mode, the U–interface transceiver can lock to 80 kbaud ± 32 ppm receive signals.

A single 20.48 MHz pullable crystal must be connected between $XTAL_{in}$ and $XTAL_{out}$ pins of the MC145572. Please refer to **Appendix B** for crystal specifications and sourcing information. The crystal specified for NT mode operation will operate in LT applications. The crystal specified for LT applications ***will not*** operate in NT applications. The reason is that the NT mode crystal has a tighter overall frequency tolerance than the LT mode crystal.

NOTE

Motorola continues to qualify several third party sources for the 20.48 MHz crystal. Contact your local Motorola representative or the Motorola factory applications staff for the latest information regarding component sourcing.