10
ELECTRICAL SPECIFICATIONS

10.1 ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to 7.0	V
Voltage, Any Pin to V_{SS}	V_{in}	−0.3 to V_{DD} +0.3	V
DC Current, Any Pin (Note 1)	I_{in}	± 10	mA
Operating Temperature	T_A	– 40 to + 85	°C
Storage Temperature	T_{stg}	– 85 to + 150	°C

NOTE:
1. Except for V_{DD}, V_{SS}, TxP, and TxN.

10.2 RECOMMENDED OPERATING CONDITIONS

(Voltages referenced to V_{SS}, T_A = –40 to +85°C)

Parameter	Pins	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Current Sourced from CAP 3V pin @ 2.7 V				5	mA

10.3 POWER CONSUMPTION

(Voltages referenced to V_{SS}, T_A = – 40 to + 85°C)

Parameter	Pins	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Power Consumption, Activated		—	225	275	mW
Power Consumption, Absolute Power Down		—	—	5	mW
Power Consumption, Deactivated			135		mW

10.4 PERFORMANCE

(V_{DD} = 5.0 V ± 5%, T_A = – 40 to + 85°C)

Parameter	Min	Typ	Max	Unit
Cold Start Time, LT Mode	—	9	—	s
Cold Start Time, NT Mode	—	4	—	s
Warm Start Time, LT and NT Modes	—	75	—	ms
Transmit Linearity	45	—	—	dB
Bit Error Rate, 16,500k ft of 26 AWG, 1500 ft of 24AWG, +1 dB NEXT Margin, ANSI T1.601–1992 (see Note)	—	—	10^{-7}	
Differential Receiver Sensitivity		15	20	mV

NOTE: Bit error rate performance depends significantly on the characteristics of the line interface circuit used to couple the MC145572 to the transmission line. This parameter is provided for informational purposes only.

10.5 DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5.0 V + 5%, T_A = – 40 to + 85°C)

Parameter	Test Conditions	Symbol	Min	Max	Unit
High–Level Input Voltage, except FREQREF and RESET		V_{IH}	2.0	—	V
Low–Level Input Voltage, except FREQREF and RESET		V_{IL}	– 0.3	0.8	V
High–Level Input Voltage, FREQREF and RESET		V_{IH}	3.75	—	V
Low–Level Input Voltage, FREQREF and RESET		V_{IL}	—	1.25	V
High–Level Output Voltage (I_{OH}=–400 uA)		V_{OH}	2.4	—	V
Low–Level Output Voltage (I_{OL}= 5 mA)		V_{OL}		.5	V
High–Level Input Current		I_{IH}	– 1	1	µA
Low–Level Input Current		I_{IL}	– 1	1	µA
High–Level Output Current	$V_{OH} = V_{DD} – 0.5$ V	I_{OH}	– 4	—	mA
Low–Level Output Current	V_{OL} = 0.4 V	I_{OL}	—	2.5	mA
$\overline{IRQ}$ Output Current	V_{OL} = 0.4 V	I_{IRQ}	—	2	mA
$\overline{IRQ}$ High Impedance		$R_{IRQ\ off}$	100	—	kΩ
Input Capacitance, Digital Pins		C_{in}	—	10	pF
$XTAL_{in}$ High–Level Input			3.5	—	V
$XTAL_{in}$ Low–Level Input			—	1.5	V
$XTAL_{out}$ Output Current	V_{OH} ,V_{OL} = 2.5 V		– 6.5	6.5	mA

NOTE: All digital outputs except $XTAL_{out}$ are three–stateable regardless of their normal operating condition.

10.6 2B1Q INTERFACE ELECTRICAL CHARACTERISTICS

10.6.1 Pins TxP and TxN (V_{DD} = 5 V + 5%, T_A = – 40 to + 85°C, R_L = 60 Ω from TxP to TxN)

Parameter	Min	Typ	Max	Unit
Output Resistance — Full Power Mode	—	—	0.05	Ω
Output Resistance — Power Down Mode	—	10	30	Ω
Output Resistance — Absolute Power Down Mode	—	10	30	Ω
Output Peak Voltage from TxP to TxN	—	± 4.0	—	V_{pk} $-V_{pk}$
Output Load Capacitance	—	—	47	nF
Power Supply Rejection	—	60	—	dB
Peak Current	—	75	—	mA

10.6.2 Pins RxP and RxN (V_{DD} = 5 V + 5%, T_A = – 40 to + 85°C)

Parameter	Min	Max	Unit
Input Resistance — Full Power Mode	1	—	MΩ
Input Resistance — Power Down Mode	1	—	MΩ
Input Resistance — Absolute Power Down Mode	1	—	MΩ
Input Capacitance	—	10	pF
Input Voltage Range for RxP or RxN	$((V_{DD} – V_{SS})/2) – 0.5$	$((V_{DD} – V_{SS})/2) + 0.5$	V

10.7 IDL2 TIMING

10.7.1 IDL2 Master Short Frame Sync Timing, 8/10-Bit and TSAC Formats

Ref. No.	Parameter		Min	Typ	Max	Unit	Note
1	FSR or FSX Period		125	125	—	µs	1
2	Delay From the Rising Edge of DCL to the Rising Edge of FSX or FSR		—		30	ns	
3	Delay From the Rising Edge of DCL to the Falling Edge of FSX or FSR		—		30	ns	
4	DCL Clock Period		391		1953	ns	2
5	DCL Pulse Width High, Nominal	512 kHz	878		1074	ns	3
		2.048 MHz	210		265		
		2.56 MHz	170		215		
	DCL Clock 249 Pulse Width High	2.048 MHz	160		315		
		2.56 MHz	120		265		
	DCL Clock 59 Pulse Width High	512 kHz	825		1120		
6	DCL Pulse Width Low		45		55	% of DCL Period	4
7	Delay From Rising Edge of DCL to Low–Z and Valid Data on D_{out}		—		30	ns	
8	Delay From Rising Edge of DCL to Data Valid on D_{out}		5		30	ns	
9	Delay From Rising Edge of DCL to Hi–Z on D_{out}		—		30	ns	
10	Data Valid on D_{in} Before Falling Edge of DCL (D_{in} Setup Time)		25		—	ns	
11	Data Valid on D_{in} After Falling Edge of DCL (D_{in} Hold Time)		25		—	ns	
12	Delay From Rising Edge of DCL to TSEN Low		—		30	ns	5
13	Delay From Falling Edge of DCL to TSEN High		—		30	ns	

NOTES:

1. FSR or FSX occurs on average every 125 µs.
2. The DCL Frequency may be 512 kHz, 2.048 MHz, or 2.56 MHz.
3. The duty cycle of DCL is between 45% and 55% when operated in master timing mode. This duty cycle is guaranteed for all DCL clocks except the clock that is used for making timing adjustments in order to maintain synchronization with the received signal when operating in NT mode.
   In NT master mode the MC145572 conveys timing adjustments over the DCL clock of the device. This is done by adding or subtracting a single 20.48 MHz clock period of 48 ns to the high phase of DCL clock on two successive IDL frames once per U–Interface basic frame. The total adjustment is 96 ns distributed over the two IDL frames. When DCL is configured for 2.048 MHz or 2.56 MHz the adjustment occurs during clock pulse number 249 after FSX/FSR. The count starts at clock pulse 0 for the DCL clock immediately following FSX/FSR. When DCL is configured for 512 kHz the adjustment occurs during DCL pulse number 59. It is important to remember this when using the timeslot assigner since it is possible to program it to transfer 2B or D data during the clock period where the timing adjustment is being made and this may effect setup and hold times for other components in a system.
4. The pulse width during the low phase of the clock varies between 45% and 55% of the nominal frequency. Timing adjustments are not made during the low phase of DCL.
5. In IDL 8 and 10 bit formats, TSEN can be valid during the B1, B2 and D channel timeslots.

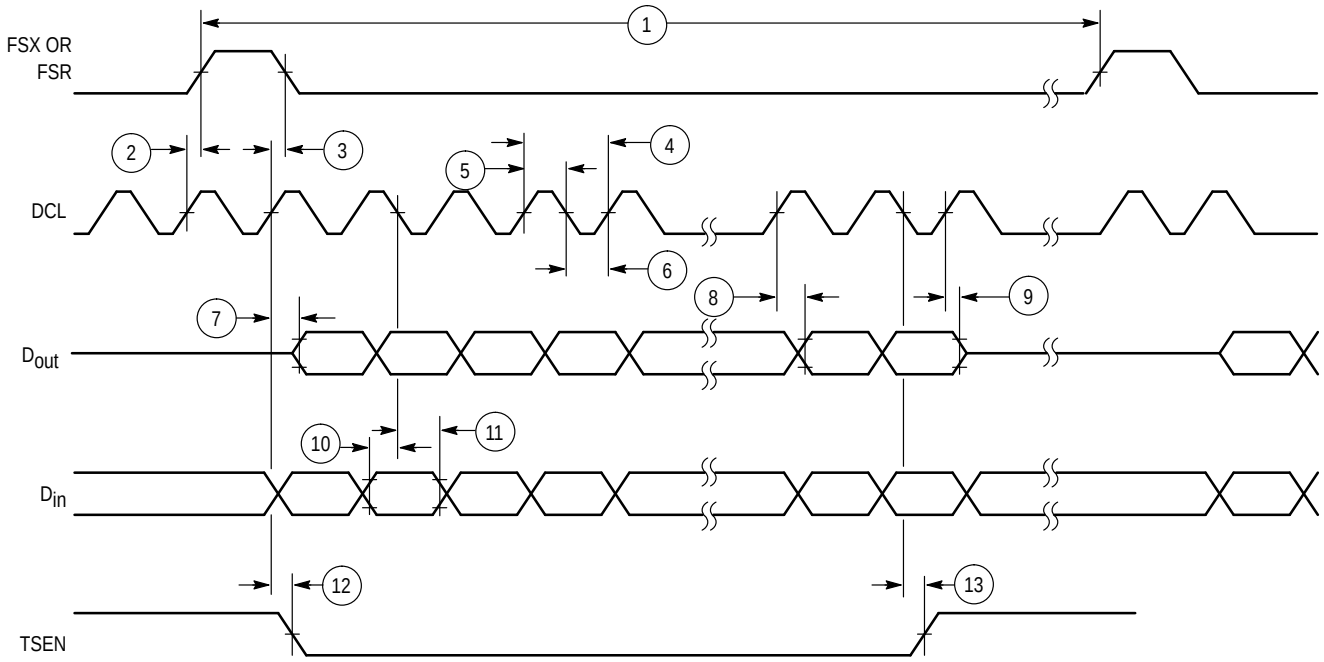

Figure 10–1. IDL Short Frame Sync Master Timing, 8/10–Bit Formats and TSAC Formats

10.7.2 IDL2 Slave Short Frame Sync Timing, 8- and 10-Bit Formats

Ref. No.	Parameter	Min	Max	Unit	Note
14	FSR or FSX Period	125	—	µs	1
15	FSR or FSX High Before the Falling Edge of DCL (FSR or FSX Setup Time)	25	—	ns	
16	FSR or FSX High After the Falling Edge of DCL (FSR or FSX Hold Time)	25	—	ns	
17	Delay From Rising Edge of DCL to Low–Z and Valid Data on D_{out}	—	30	ns	
18	Delay From Rising Edge of DCL to Data Valid on D_{out}	—	30	ns	
19	Delay From Rising Edge of DCL to Hi–Z on D_{out}	5	30	ns	
20	Delay From Rising Edge of DCL to TSEN Low	—	30	ns	2
21	Delay From Rising Edge of DCL to TSEN High	—	30	ns	
22	DCL Clock Period	244	1953	ns	3
23	DCL Pulse Width High	45	55	% of DCL Period	
24	DCL Pulse Width Low	45	55	% of DCL Period	
25	Data Valid on D_{in} Before Falling Edge of DCL (D_{in} Setup Time)	25	—	ns	
26	Data Valid on D_{in} After Falling Edge of DCL (D_{in} Hold Time)	25	—	ns	

NOTES:

1. FSR or FSX occurs on average every 125 µs. FSX and FSR/FSC must occur every 125 µs with a maximum instantaneous phase titter of ± 30 µs.
2. In IDL2 8 and 10 bit formats, TSEN is valid during the B1, B2, and D–Channel timeslots. TSEN will be aligned with data on the D_{out} pin.
3. In IDL2 slave mode, DCL may be any frequency multiple of 8 kHz between 256 kHz and 4.096 MHz inclusive.

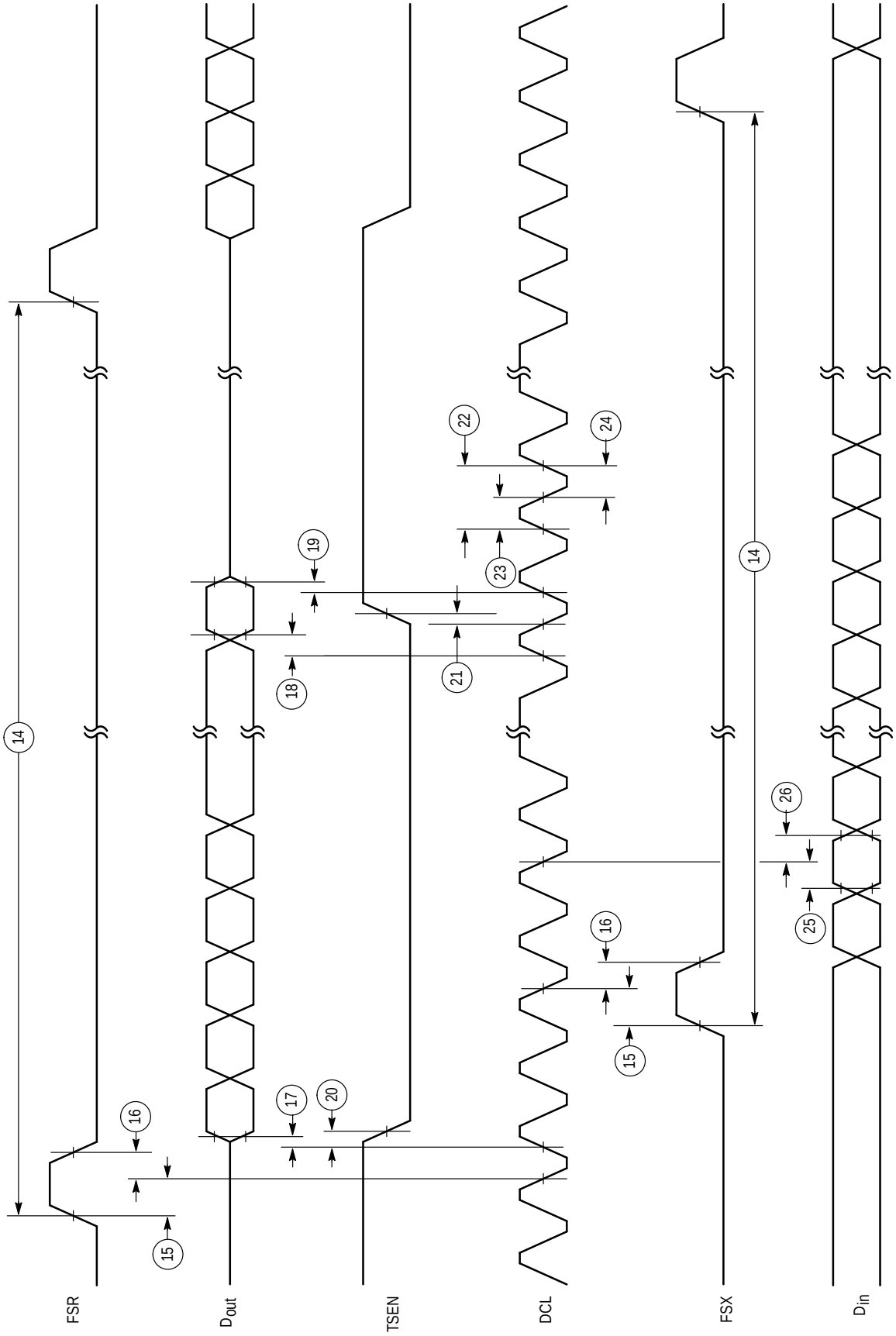

Figure 10–2. IDL Short Frame Sync Slave Timing, 8/10–Bit Formats

10.7.3 IDL2 Master Long Frame Sync, 8- and 10-Bit Formats

Ref. No.	Parameter	Min	Max	Unit	Note
27	FSR or FSX Period	125	—	µs	1
28	Delay From Rising Edge of DCL to Rising Edge of FSR or FSX	—	30	ns	
29	Delay From Rising Edge of DCL to Falling Edge of FSR or FSX	—	30	ns	2
30	Delay From Rising Edge of FSR to Low–Z and Valid Data on D_{out}	—	30	ns	
31	Delay From Rising Edge of DCL to Data Valid on D_{out}	—	30	ns	
32	Delay From Rising Edge of DCL to Hi–Z on D_{out}	5	30	ns	
33	DCL Clock Period	391	1953	ns	3
34	DCL Pulse Width High	45	55	% of DCL Period	
35	DCL Pulse Width Low	45	55	% of DCL Period	
36	Data Valid on D_{in} Before Falling Edge of DCL (D_{in} Setup Time)	25	—	ns	
37	Data Valid on D_{in} After Falling Edge of DCL (D_{in} Hold Time)	25	—	ns	
38	Delay From Rising Edge of FSR to TSEN Low	—	30	ns	4
39	Delay From Falling Edge of DCL to TSEN High	—	30	ns	

NOTES:
1. FSR or FSX occurs on average every 125 µs.
2. The duty cycle of DCL is between 45% and 55% when operated in master timing mode. This duty cycle is guaranteed for all DCL clocks except the clock that is used for making timing adjustments in order to maintain synchronization with the received signal when operating in NT mode. This timing adjustment does not occur during the 2B+D data transfer. The timing adjustment is done by adding or subtracting a single 20.48 MHz clock period of 48 ns to the high phase of DCL clock on two successive IDL frames once per U–Interface basic frame. The total adjustment is 96 ns distributed over the two IDL frames.
3. In IDL master long frame sync mode, the FSR or FSX pulse is 8 DCL clock periods long.
4. The DCL frequency may be 512 kHz, 2.048 MHz, or 2.56 MHz.
5. In IDL 8 and 10 bit formats, TSEN can be valid during the B1, B2, and D–Channel timeslots.

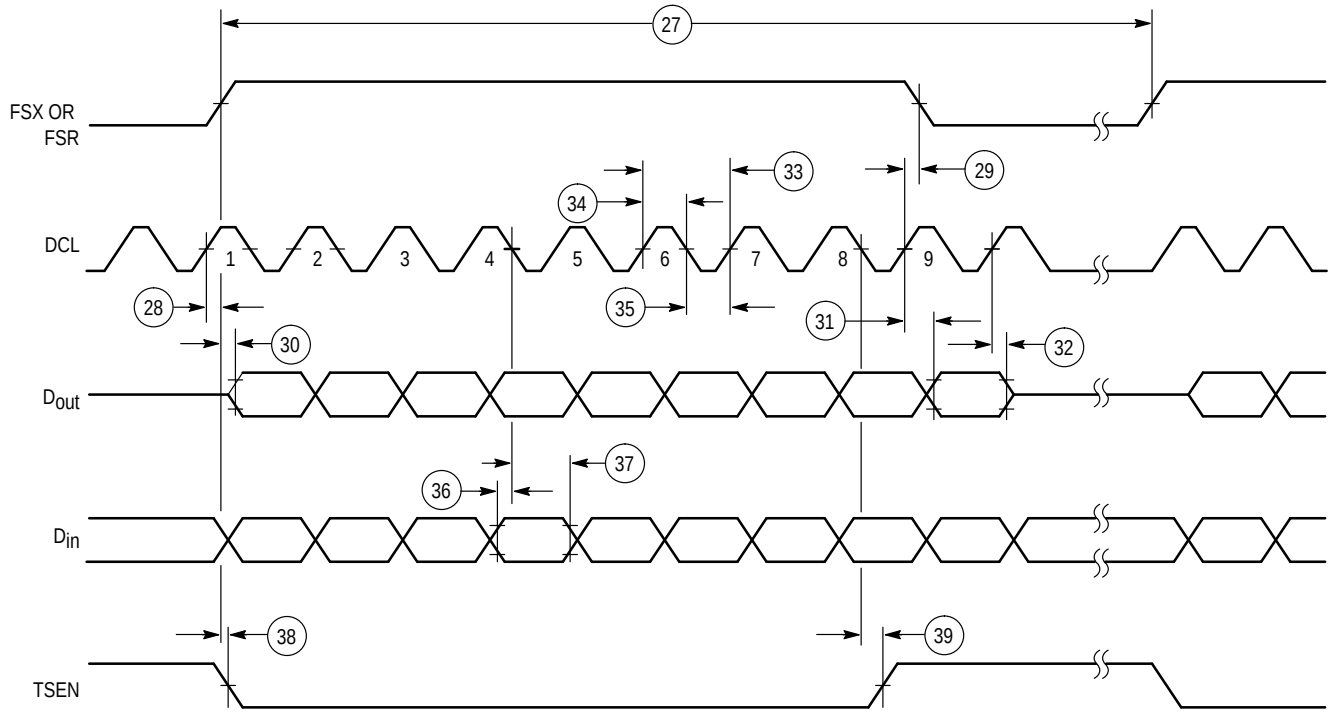

Figure 10–3. Long Frame Sync Master Timing, 8/10–Bit Formats

10.7.4 IDL2 Slave Long Frame Sync, 8- and 10-Bit Formats

Ref. No.	Parameter	Min	Max	Unit	Note
40	FSR or FSX Period	125	—	µs	1
41	FSR or FSX High Before the Falling Edge of DCL (FSR or FSX Setup Time)	25	—	ns	2
42	FSR or FSX High After the Falling Edge of DCL (FSR or FSX Hold Time)	25	—	ns	2
43	FSR or FSX Low Before the Falling Edge of DCL	25	—	ns	2
44	Delay From Rising Edge of FSR to Low–Z and Valid Data on D_{out}	—	30	ns	
45	Delay From Rising Edge of DCL to Data Valid on D_{out}	—	30	ns	
46	Delay From Rising Edge of DCL to Hi–Z on D_{out}	5	30	ns	
47	Delay From Rising Edge of FSR to TSEN Low	—	30	ns	3
48	Delay From Falling Edge of DCL to TSEN High	—	30	ns	
49	DCL Clock Period	244	1953	ns	4
50	DCL Pulse Width High	45	55	% of DCL Period	
51	DCL Pulse Width Low	45	55	% of DCL Period	
52	Data Valid on D_{in} Before Falling Edge of DCL (D_{in} Setup Time)	25	—	ns	
53	Data Valid on D_{in} After Falling Edge of DCL (D_{in} Hold Time)	25	—	ns	

NOTES:

1. FSR or FSX occurs on average every 125 µs. FSX and FSR/FSC must occur every 125 µs with a maximum instantaneous phase titter of ± 30 µs.
2. FSR or FSX should be asserted for at least two DCL clock cycles and at most 8 DCL clock cycles.
3. In IDL 8 and 10 bit formats, TSEN is valid during the B1, B2, and D–Channel timeslots TSEN will be aligned with data on the D_{out} pin.
4. In IDL slave mode, DCL may be any frequency that is a multiple of 8 kHz and is between 256 kHz and 4.096 MHz inclusive.

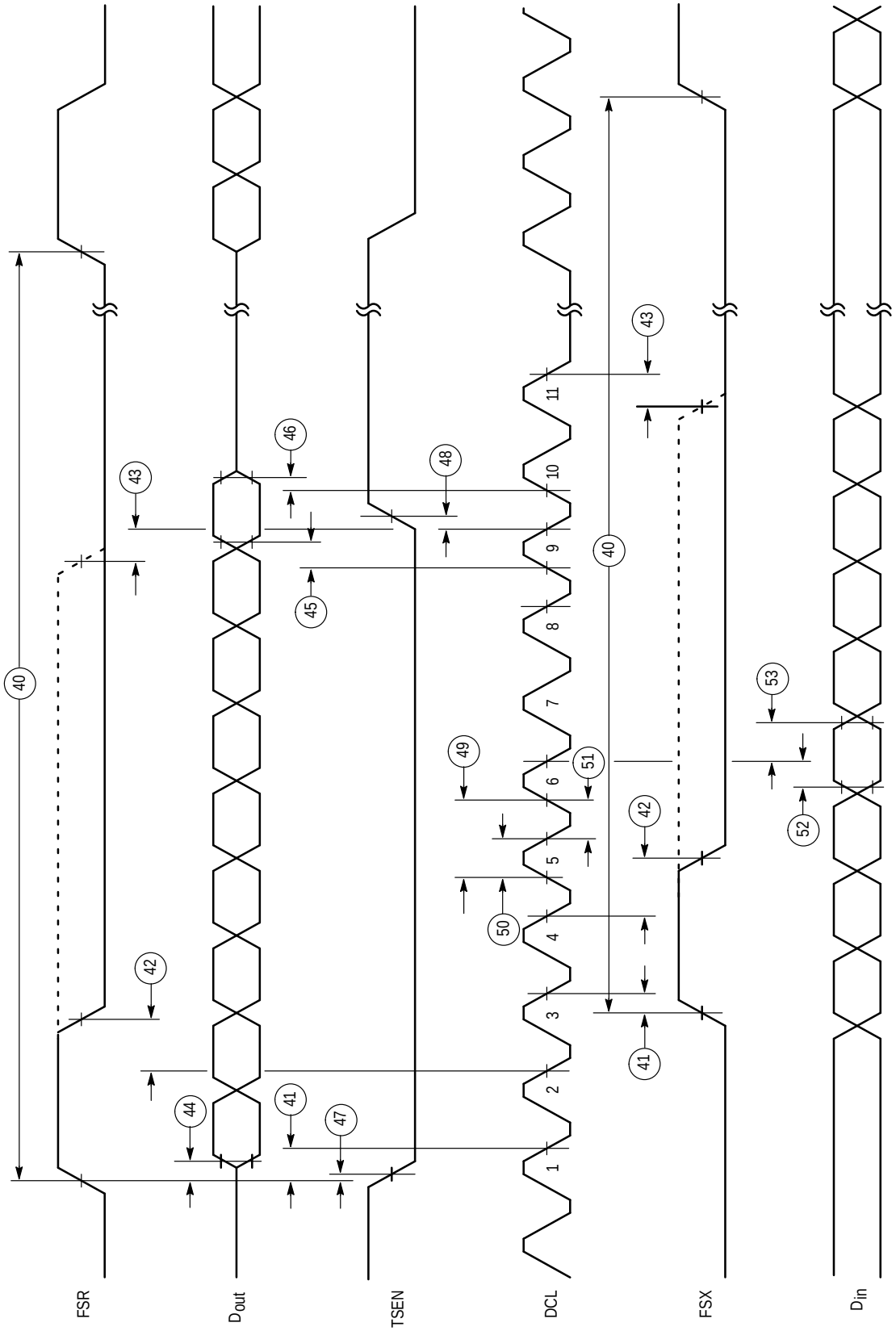

Figure 10–4. Long Frame Sync Slave Timing, 8/10–Bit Formats

10.8 GCI TIMING

Ref. No.	Parameter	Min	Typ	Max	Unit	Note
53	Delay From Rising Edge of DCL to FSC Output High	—		30	ns	
54	Delay From Rising Edge of DCL to FSC Output Low (Normal Frame)	—		30	ns	1
55	Delay From Rising Edge of DCL to FSC Output Low (Super-frame Marker)	—		30	ns	2
56	FSC Input High Before the Falling Edge of DCL (FSC Setup Time)	25		—	ns	
57	FSC Input High After the Falling Edge of DCL (FSC Hold Time — Superframe Marker)	25		—	ns	1
58	FSC Input High After the Falling Edge of FSC (FSC Hold Time — Normal Frame)	25		—	ns	3
59a	DCL Clock Period Master Mode	488		1953	ns	4
59b	DCL Clock Period Slave Mode	122		1953	ns	5
60	DCL Pulse Width High 512 kHz 2.048 kHz DCL Clock 249 Pulse Width High 2.048 MHz DCL Clock 59 Pulse Width High 512 kHz	878 210 160 825		1074 265 315 1120	ns	6
61	DCL Pulse Width Low	45		55	% of DCL Period	
62	DCL Fall Time	5		15	ns	
63	DCL Rise Time	5		15	ns	
64	Delay From Rising Edge of FSC to Low–Z and Valid Data on D_{out}	—		30	ns	
65	Delay From Rising Edge of DCL to Data Valid on D_{out}	—		30	ns	
66	Delay From Rising Edge of DCL Hi–Z on D_{out}	5		30	ns	
67	Data Valid on D_{in} Before Rising Edge of DCL	25		—	ns	
68	Data Valid on D_{in} After Rising Edge of DCL	25		—	ns	
69	Delay From Rising Edge of FSC to TSEN Low	—		30	ns	
70	Delay From Rising Edge of DCL to TSEN High	—		30	ns	

NOTES:

1. The FSC pulse is normally 2 DCL clock periods wide.
2. The FSC pulse is only one DCL clock period wide at the start of a superframe. Every 96th FSC pulse marks the start of a superframe.
3. To mark the beginning of a superframe (i.e., to flag the 2B+D data of the current frame as the first data in the transmitted superframe) the FSC pulse should be only one DCL clock period wide. If the FSC pulse is not modulated as such the MC145572 will randomly chose an FSC frame as the first to be transmitted.
4. In GCI master mode the MC145572 will output a 512 kHz or 2.048 MHz clock as selected by CLKSEL.
5. In GCI slave mode, DCL may be any frequency that is a multiple of 512 kHz and is between 512 kHz and 8.192 MHz.
6. The duty cycle of DCL is between 45% and 55% when operated in master timing mode. This duty cycle is guaranteed for all DCL clocks except the clock that is used for making timing adjustments in order to maintain synchronization with the received signal when operating in NT mode.
   In NT master mode the MC145572 conveys timing adjustments over the DCL clock of the device. This is done by adding or subtracting a single 20.48 MHz clock period of 48 ns to the high phase of DCL clock on two successive GCI frames once per U–Interface basic frame. The total adjustment is 96 ns distributed over the two frames. When DCL is configured for 2.048 MHz the adjustment occurs during clock pulse number 249 after FSC. The count starts at clock pulse 0 for the DCL clock immediately coincident with FSC being driven high. When DCL is configured for 512 kHz the adjustment occurs during DCL pulse number 59. It is important to remember this when programming the GCI timeslot since it is possible for data to be transferred during the clock period where the timing adjustment is being made and this may effect setup and hold times for other components in a system.

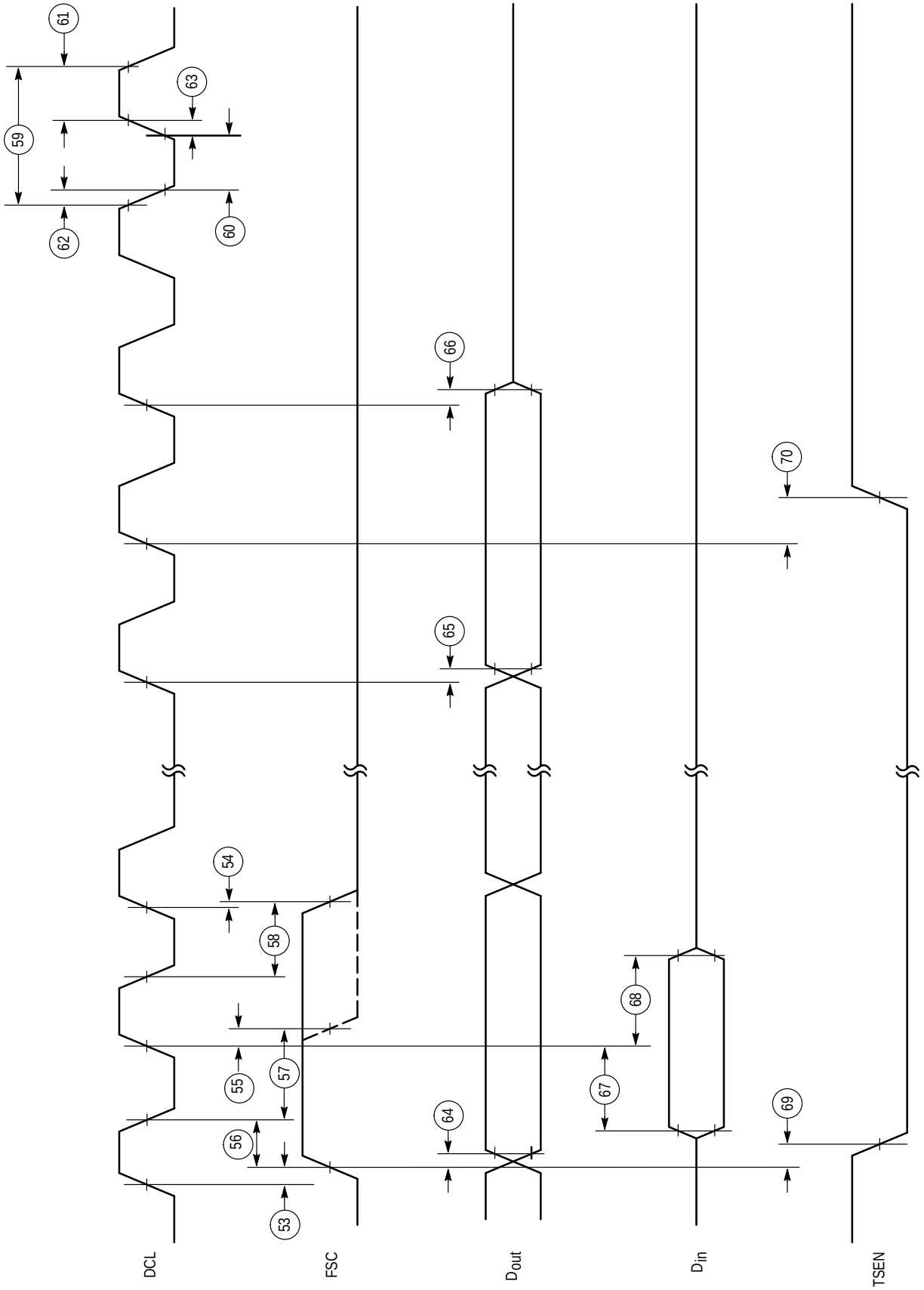

Figure 10–5. GCI Timing

10.9 D-CHANNEL PORT TIMING

10.9.1 IDL2 (Master or Slave) Short Frame Sync 8-Bit Format, D Channel Port Timing

Ref. No.	Parameter	Min	Max	Unit	Note
71	Delay From DCL Rising Edge to DCHCLK Rising Edge	—	30	ns	
72	Delay From DCHCLK Rising Edge to Data Valid on DCHOUT	—	30	ns	
73	Data Valid on DCHIN Before Falling Edge of DCHCLK (DCHIN Setup Time)	25	—	ns	
74	Data Valid on DCHIN After Falling Edge of DCHCLK (DCHIN Hold Time)	25	—	ns	

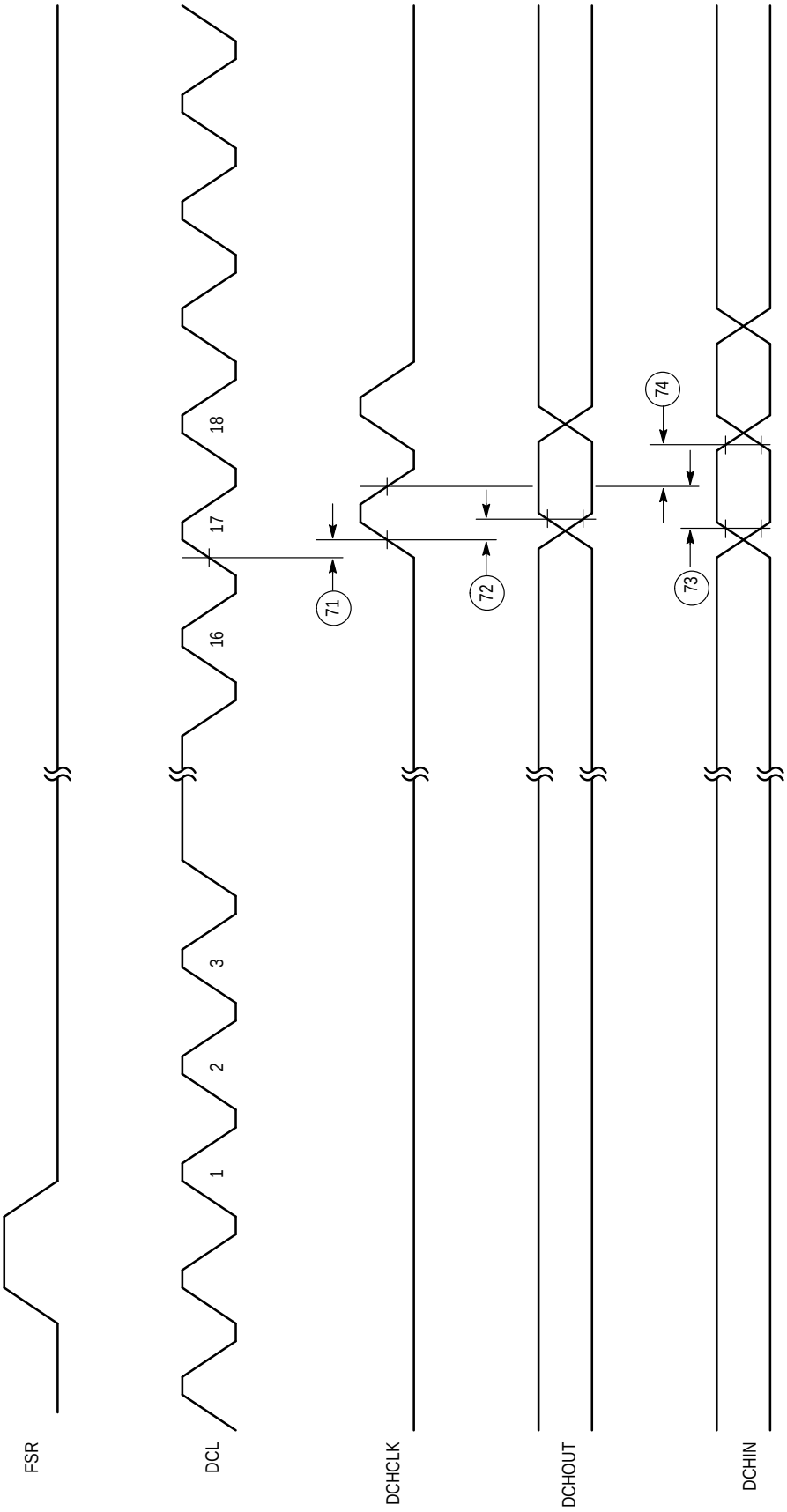

Figure 10–6. IDL2 (Master or Slave) Short Frame Sync 8–Bit Format, D Channel Port Timing

10.9.2 IDL2 (Master or Slave) Short Frame Sync 10-Bit Format, D Channel Port Timing

Ref. No.	Parameter	Min	Max	Unit	Note
75	Delay From DCL Rising Edge to DCHCLK Rising Edge	—	30	ns	
76	Delay From DCHCLK Rising Edge to Data Valid on DCHOUT	—	30	ns	
77	Data Valid on DCHIN Before Falling Edge of DCHCLK (DCHIN Setup Time)	25	—	ns	
78	Data Valid on DCHIN After Falling Edge of DCHCLK (DCHIN Hold Time)	25	—	ns	

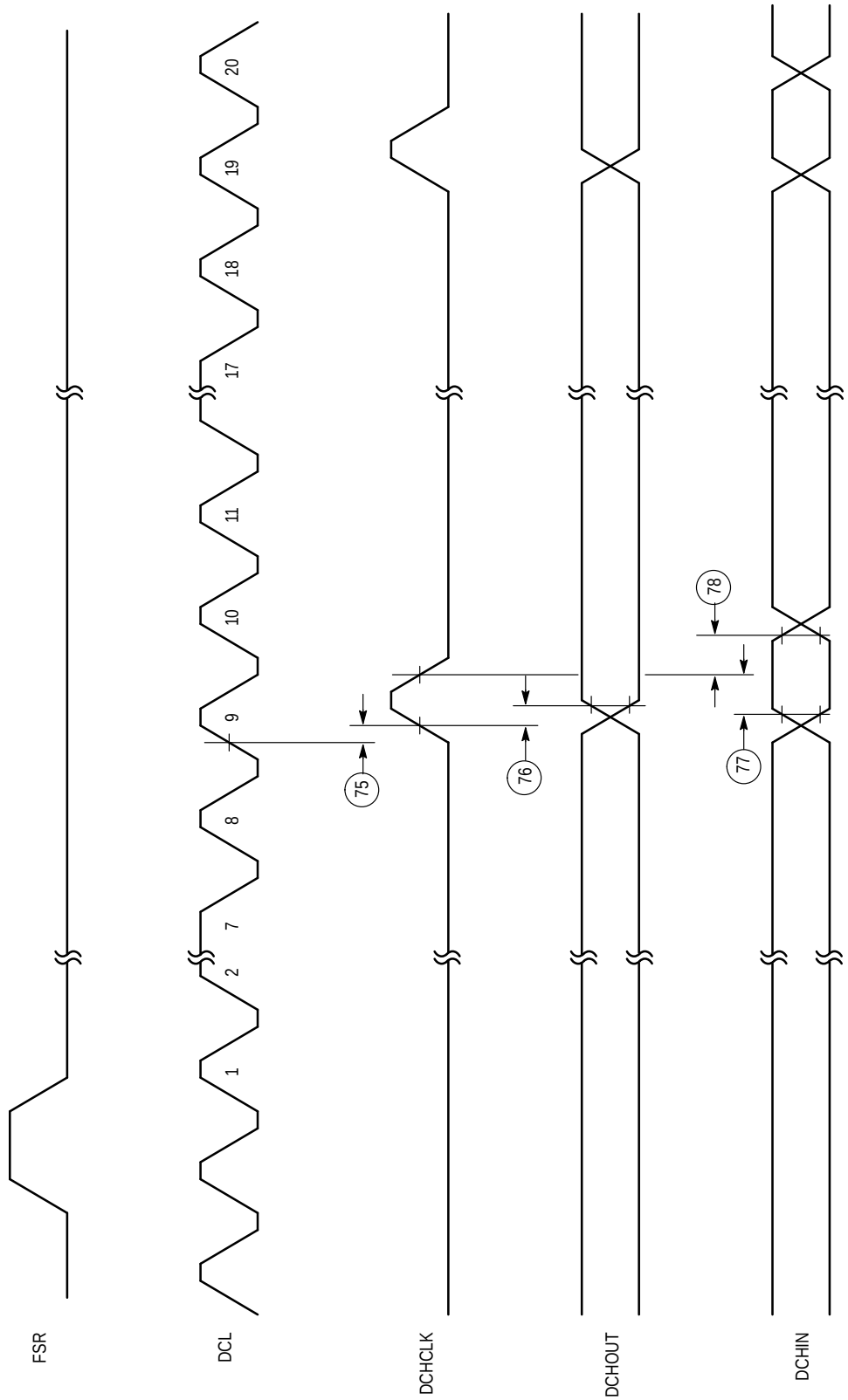

Figure 10–7. IDL2 (Master or Slave) Short Frame Sync 10–Bit Format, D Channel Port Timing

10.9.3 IDL2 (Master or Slave) Long Frame Sync 8-Bit Format, D Channel Port Timing

Ref. No.	Parameter	Min	Max	Unit	Note
79	Delay From DCL Rising Edge to DCHCLK Rising Edge	—	30	ns	
80	Delay From DCHCLK Rising Edge to Data Valid on DCHOUT	—	30	ns	
81	Data Valid on DCHIN Before Falling Edge of DCHCLK (DCHIN Setup Time)	25	—	ns	
82	Data Valid on DCHIN After Falling Edge of DCHCLK (DCHIN Hold Time)	25	—	ns	

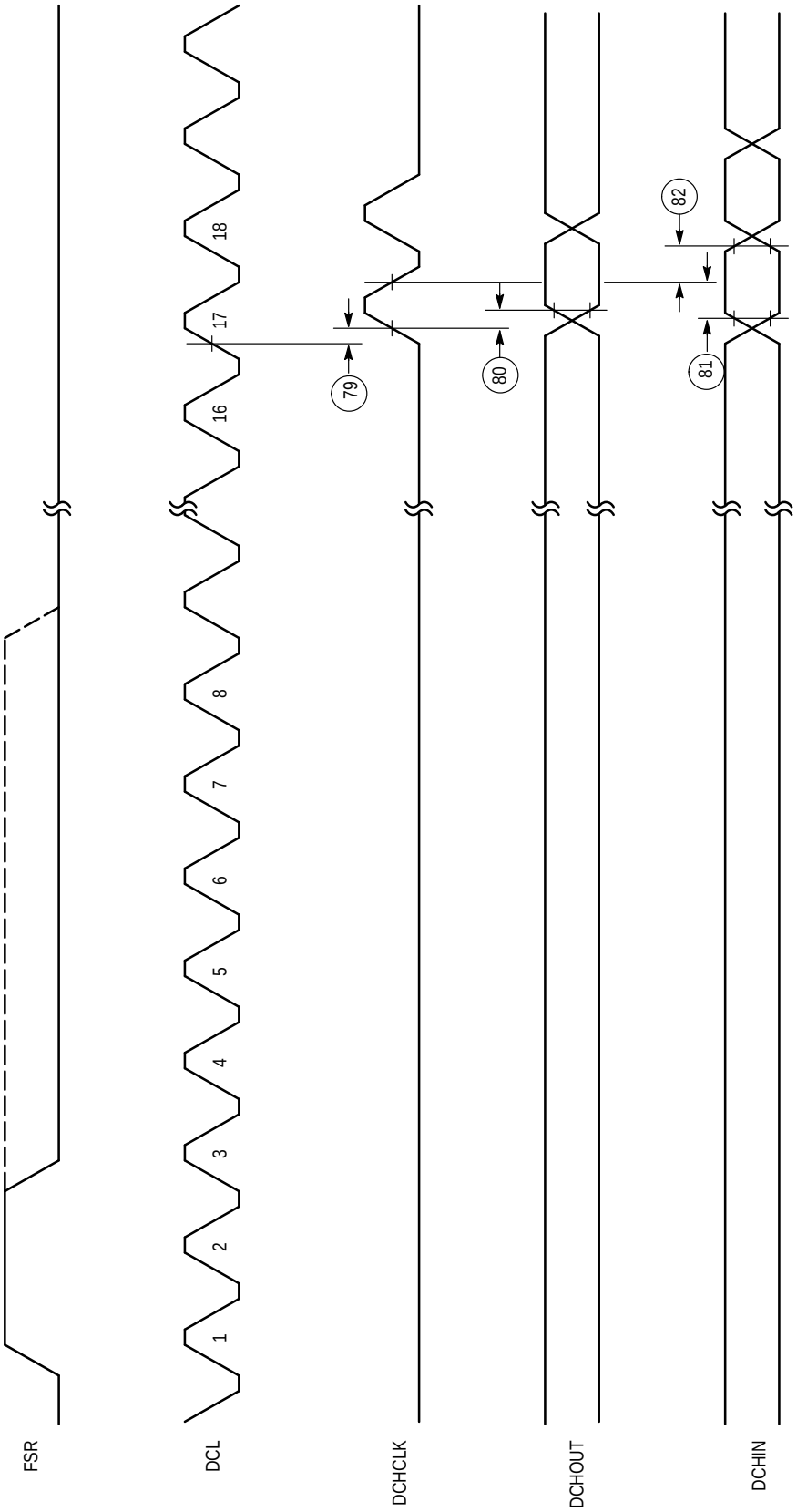

Figure 10–8. IDL2 (Master or Slave) Long Frame Sync 8–Bit Format, D Channel Port Timing

10.9.4 IDL2 (Master or Slave) Long Frame Sync 10-Bit Format, D Channel Port Timing

Ref. No.	Parameter	Min	Max	Unit	Note
83	Delay From DCL Rising Edge to DCHCLK Rising Edge	—	30	ns	
84	Delay From DCHCLK Rising Edge to Data Valid on DCHOUT	—	30	ns	
85	Data Valid on DCHIN Before Falling Edge of DCHCLK (DCHIN Setup Time)	25	—	ns	
86	Data Valid on DCHIN After Falling Edge of DCHCLK (DCHIN Hold Time)	25	—	ns	

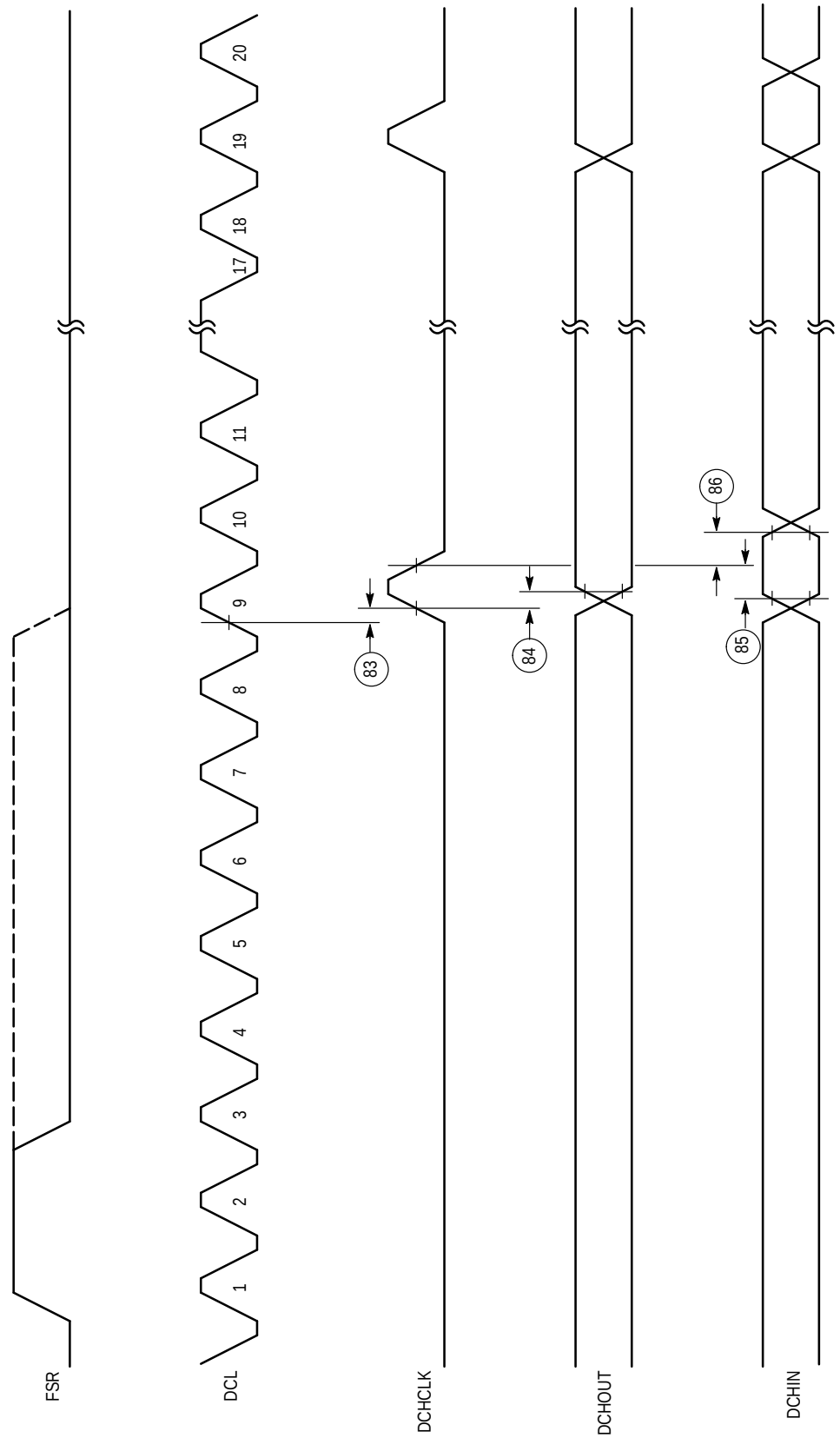

Figure 10–9. IDL2 (Master or Slave) Long Frame Sync 10–Bit Format, D Channel Port Timing

10.10 SUPERFRAME TRANSMIT AND RECEIVE (SFAX/SFAR) TIMING

10.10.1 SFAX Input Timing in IDL2 (Master or Slave) Short Frame Mode

Ref. No.	Parameter	Min	Max	Unit	Note
91	FSX Period	125	—	µs	1
92	SFAX Period	12.0	—	ms	2
93	SFAX Input High Before Falling Edge of DCL (SFAX Setup Time)	25	—	ns	3
94	SFAX Input High After Falling Edge of DCL (SFAX Hold Time)	25	—	ns	

NOTES:
1. See Section 10.7 for FSX jitter requirements and specifications.
2. SFAX must occur every 96 FSX 8 kHz frames.
3. SFAX is sampled on the next DCL falling edge after FSX is asserted.

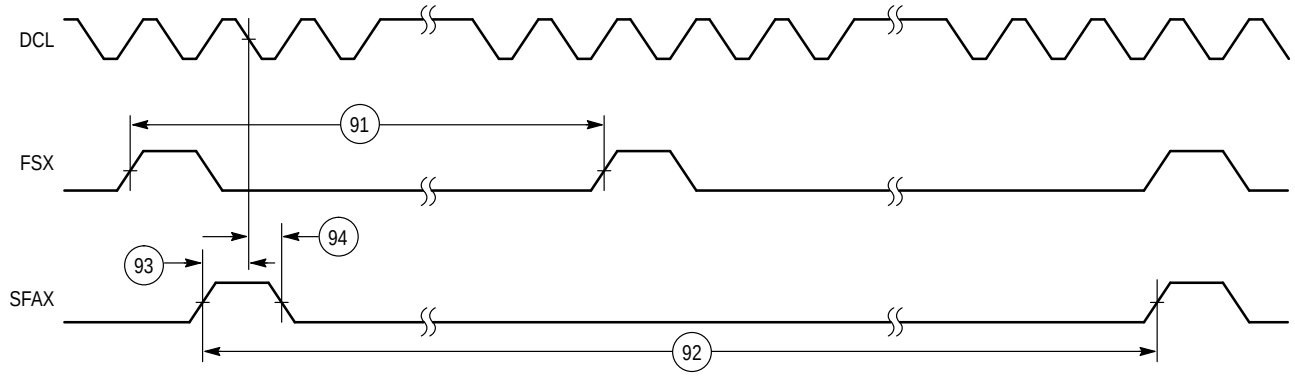

Figure 10–10. SFAX Input Timing in IDL2 (Master or Slave) Short Frame Mode

10.10.2 SFAX Input Timing in IDL2 (Master or Slave) Long Frame Mode

Ref. No.	Parameter	Min	Max	Unit	Note
95	Delay From Rising Edge of DCL to Rising Edge of FSR or FSX	—	30	ns	
96	FSR or FSX High Before the Falling Edge of DCL (FSR or FSX Setup Time)	25	—	ns	
97	FSR or FSX High After the Falling Edge of DCL (FSR or FSX Hold Time)	25	—	ns	
98	FSX Period	125	—	µs	1
99	SFAX Period	12.0	—	ms	2
100	SFAX Input High Before Rising Edge of FSX (SFAX Setup Time)	25	—	ns	3
101	SFAX Input High After Rising Edge of FSX (SFAX Hold Time)	25	—	ns	

NOTES:
1. See Section 10.7 for FSX jitter requirements and specifications.
2. SFAX must occur every 96 FSX 8 kHz frames.
3. SFAX is sampled on the rising edge of FSX.

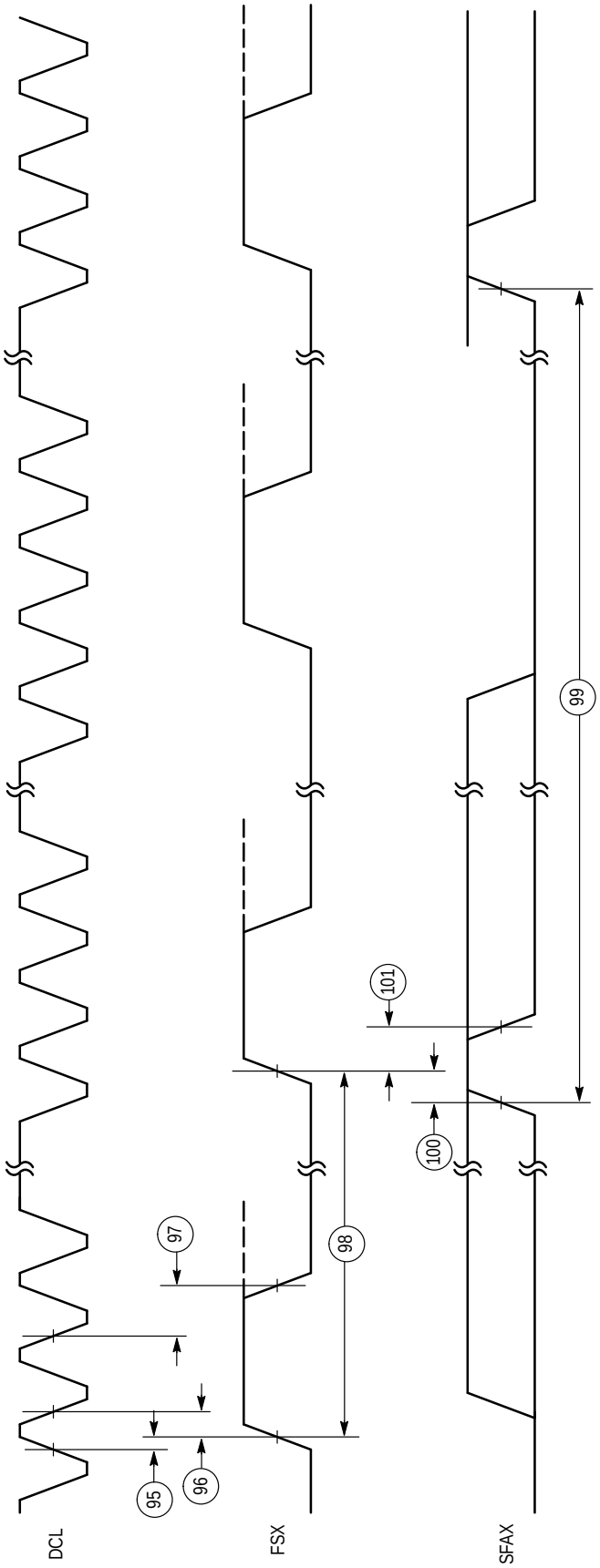

Figure 10–11. SFAX Input Timing in IDL2 (Master or Slave) Long Frame Mode

10.10.3 SFAX/SFAR Output Timing in IDL2 (Master or Slave) Short Frame Mode

Ref. No.	Parameter	Min	Max	Unit	Note
102	FSX Period	125	—	µs	1
103	SFAX Period	12.0	—	ms	2
104	Delay From the Rising Edge of DCL to the Rising Edge of FSAR or FSAX	—	30	ns	3
105	Delay From the Rising Edge of DCL to the Rising Edge of FSAR or FSAX	—	30	ns	

NOTES:
1. See Section 10.7 for FSX jitter requirements and specifications.
2. SFAX and SFAR must occur every 96 FSX 8 kHz frames.
3. SFAX and SFAR are one DCL clock pulse wide and occur on the next DCL clock pulse after FSX or FSR is asserted.

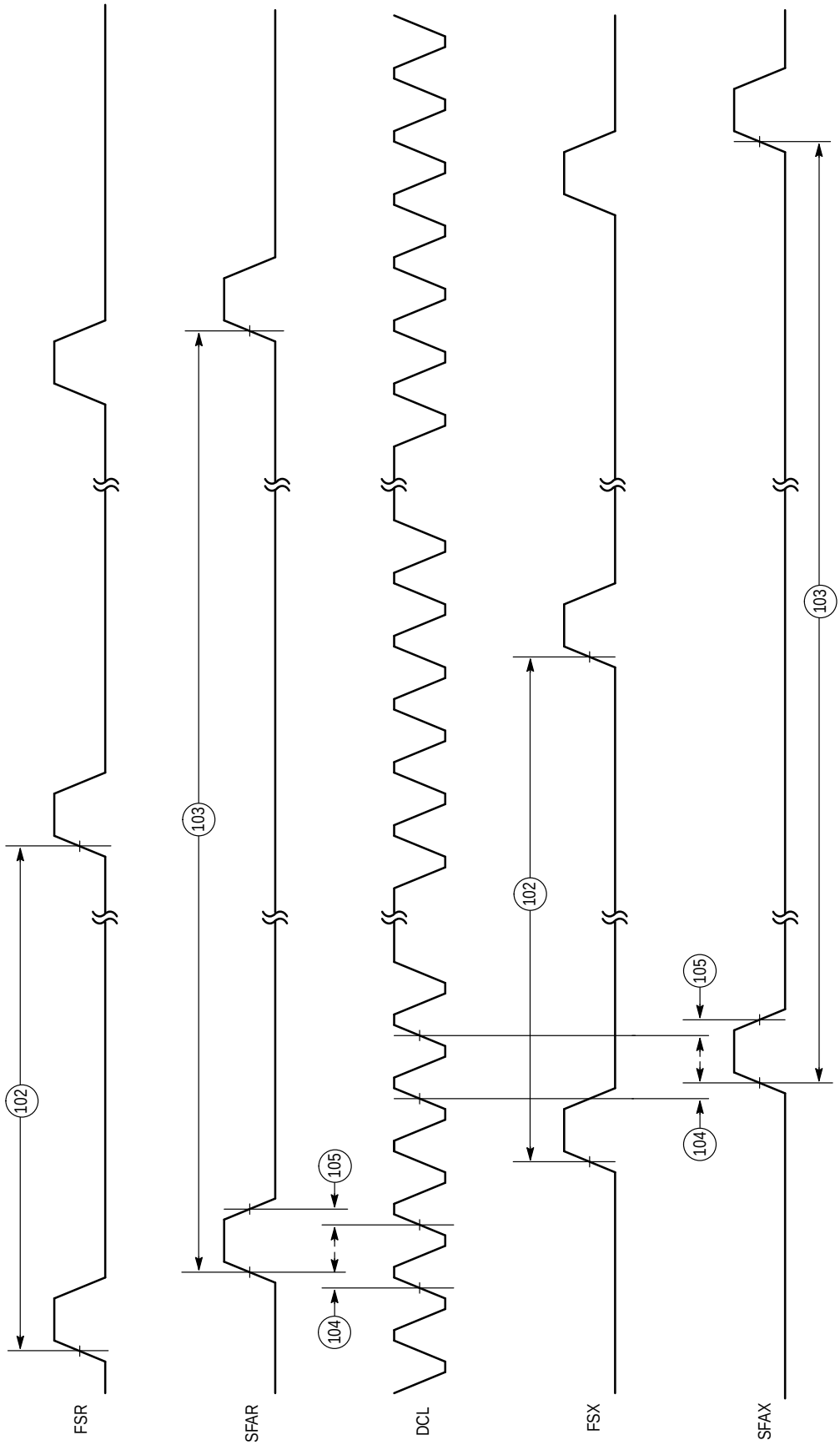

Figure 10–12. SFAX/SFAR Output Timing in IDL2 Short Frame Mode (Master or Slave)

10.10.4 SFAX/SFAR Output Timing in IDL2 (Master or Slave) Long Frame Mode

Ref. No.	Parameter	Min	Max	Unit	Note
106	FSX or FSR Period	125	—	µs	1
107	SFAX or SFAR Period	12.0	—	ms	2
108	Delay From the Rising Edge of FSR or FSX to the Rising Edge of SFAR or SFAX	—	30	ns	3

NOTES:
1. See Section 10.7 for FSX jitter requirements and specifications.
2. SFAX and SFAR must occur every 96 FSX 8 kHz frames.
3. SFAX and SFAR occur coincident with FSX and FSR respectively.

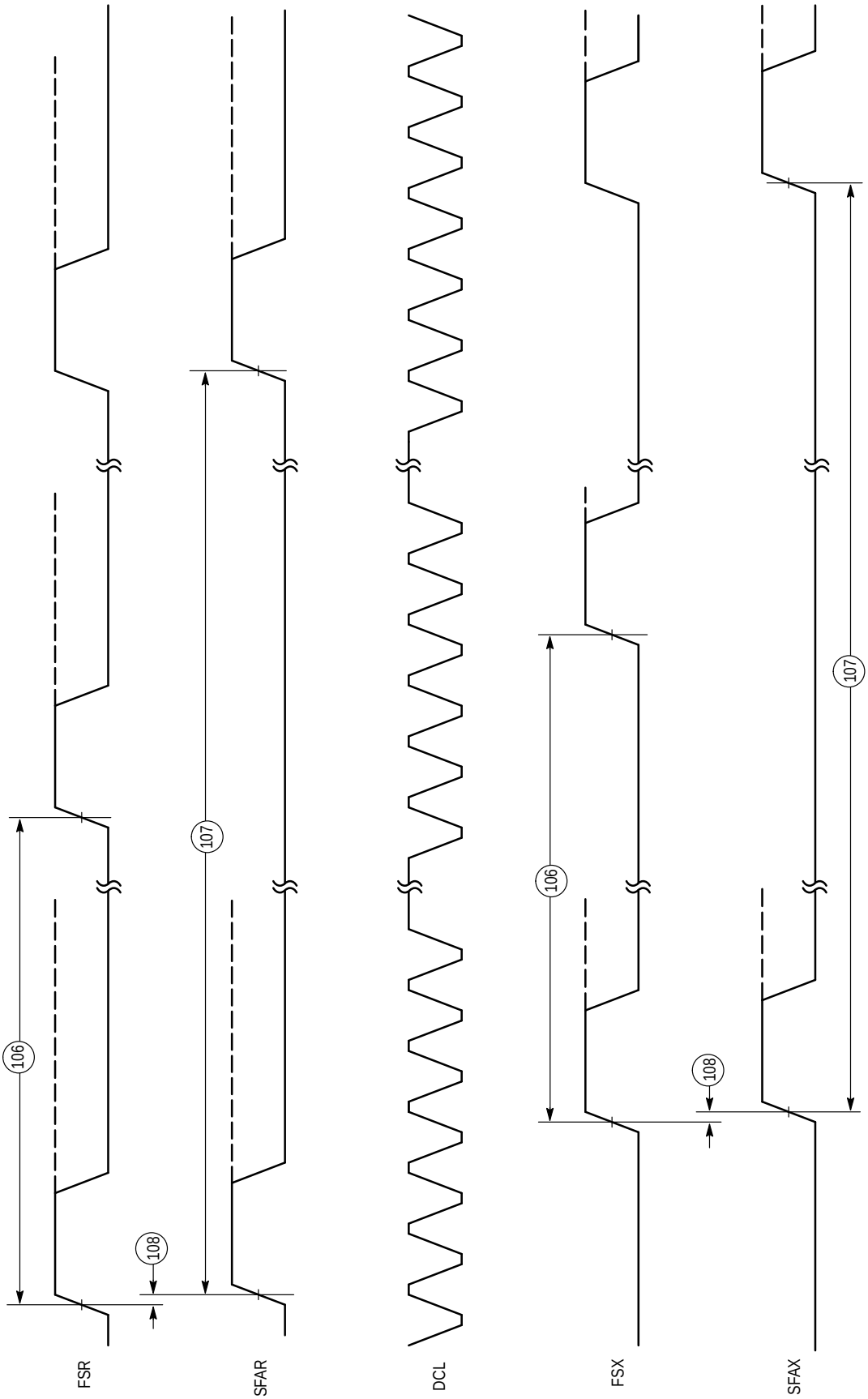

Figure 10–13. SFAX/SFAR Output Timing in IDL2 Long Frame Mode (Master or Slave)

10.11 PARALLEL CONTROL PORT TIMING

10.11.1 Parallel Control Port Write Timing

Ref. No.	Parameter	Min	Max	Unit	Note
109	CS Low	110	—	ns	
110	CS High	440	—	ns	
111	R/W Low Before CS Rising Edge (R/W Setup Time)	50	—	ns	
112	R/W Low After CS Rising Edge (R/W Hold Time)	30	—	ns	
113	D0 – D7 Valid Before the Rising Edge of CS (Data Setup Time)	20	—	ns	
114	D0 – D7 Valid After the Rising Edge of CS (Data Hold Time)	20	—	ns	

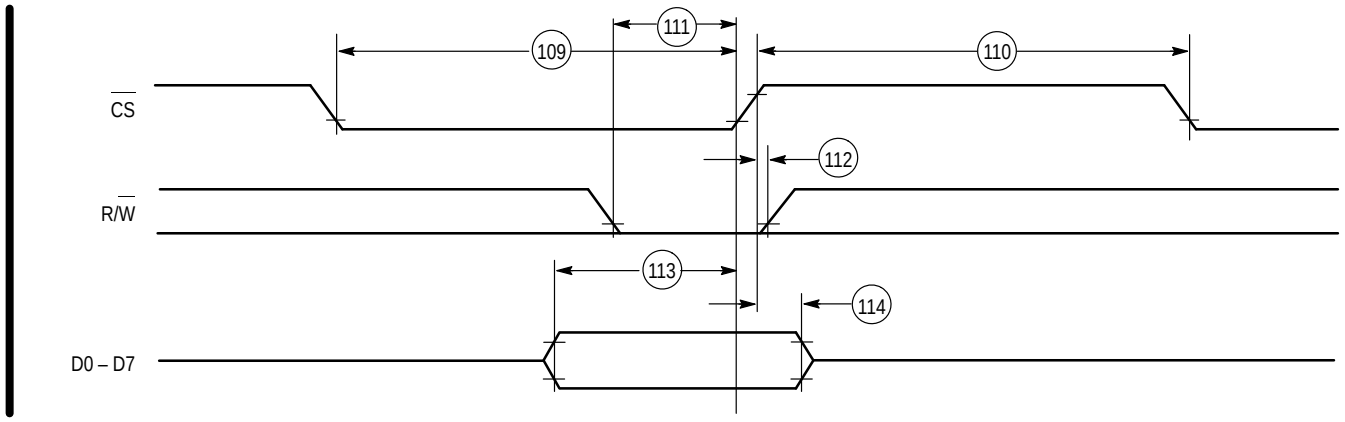

Figure 10–14. Parallel Control Port Write Timing

10.11.2 Parallel Control Port Read Timing

Ref. No.	Parameter	Min	Max	Unit	Note
115	CS Low	110	—	ns	
116	CS High	440	—	ns	
117	R/W High Before CS Falling Edge (R/W Setup Time)	0	—	ns	
118	R/W High After CS Rising Edge (R/W Hold Time)	20	—	ns	
119	D0 – D7 Valid After the Falling Edge of CS (Read Access Time)	—	30	ns	
120	D0 – D7 Valid After the Rising Edge of CS (Data Hold Time)	20	50	ns	

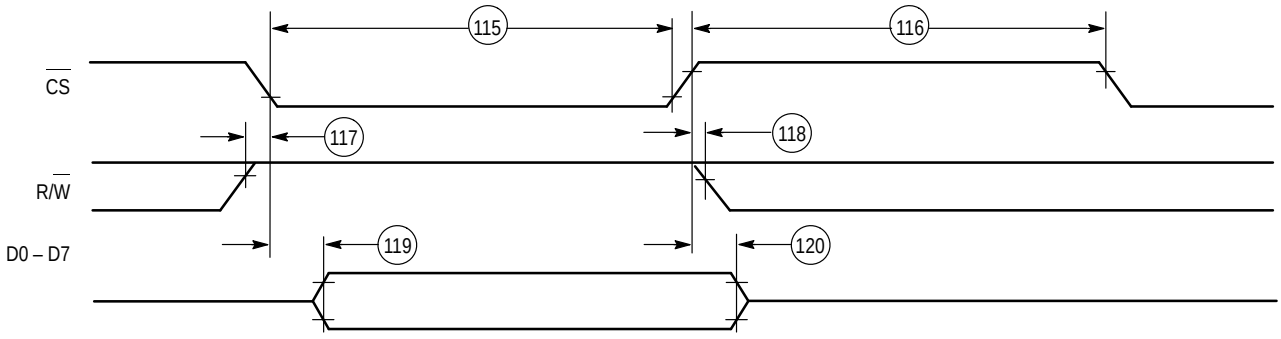

Figure 10–15. Parallel Control Port Read Timing

10.12 SWITCHING CHARACTERISTICS FOR SCP INTERFACE

(V_{DD} = 5.0 V ± 5%, T_A = – 40 to + 85°C, C_L = 50 pF; See Figure 10–2)

Ref. No.	Parameter	Min	Max	Unit
121	SCPCLK Rising Edge Before SCPEN(L) Falling Edge	40	—	ns
122	SCPEN Falling Edge Before SCPCLK Rising Edge	40	—	ns
123	SCP Rx Data Valid Before SCPCLK Rising Edge (Setup Time)	20	—	ns
124	SCP Rx Data Valid After Rising Edge of SCPCLK (Hold Time)	20	—	ns
125	SCPCLK Frequency	—	4.1	MHz
126	SCPCLK Width Low	50	—	ns
127	SCPCLK Width High	50	—	ns
128	SCPCLK Rising Edge Before SCPEN(L) Rising Edge (See Note 2)	40	—	ns
129	SCPEN Rising Before SCP CLK Rising Edge (See Note 2)	40	—	ns
130	SCPCLK Falling Edge to SCP Tx Low–Z	—	40	ns
131	SCPCLK Falling Edge (While SCP EN(L) is Low) to SCP Tx Data Valid	—	40	ns
132	SCPEN Rising Edge to SCP Tx High–Z	—	30	ns
133	SCPEN Falling Edge to SCP Tx Active (Byte Mode)	0	40	ns

NOTES:

1. Measurements are made from the point at which they achieve their guaranteed minimum or maximum logic levels.
2. SCPEN must rise between the rising edge of the eighth SCPCLK and the rising edge of the ninth SCPCLK for an 8–bit access or the access will be ignored. For a 16–bit access, SCPEN must rise between the rising edge of the sixteenth SCPCLK and the rising edge of the seventeenth SCPCLK or the access will be ignored.

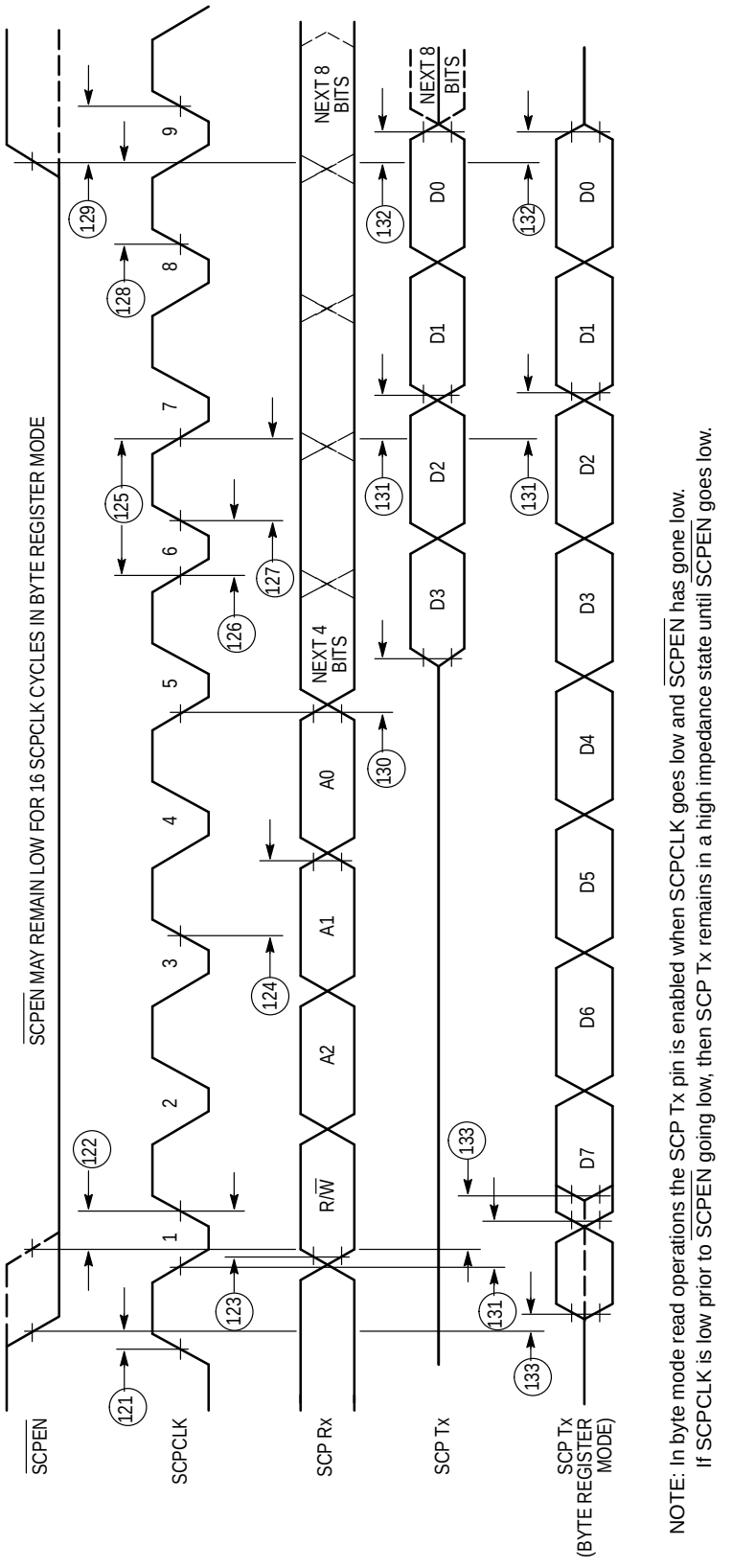

Figure 10–16. Serial Control Port (SCP) Interface Timing

10.13 SWITCHING CHARACTERISTICS FOR SYSCLK AND EYE DATA

(V_{DD} = 5.0 V ± 5%, T_A = – 40 to + 85°C, C_L = 50 pF; See Figure 10–13)

Ref. No.	Parameter	Min	Max	Unit
134	SYSCLK Rising Edge to EYE DATA Valid	–35	35	ns

NOTE: Measurements are made from the point at which they achieve their guaranteed minimum or maximum logic levels.

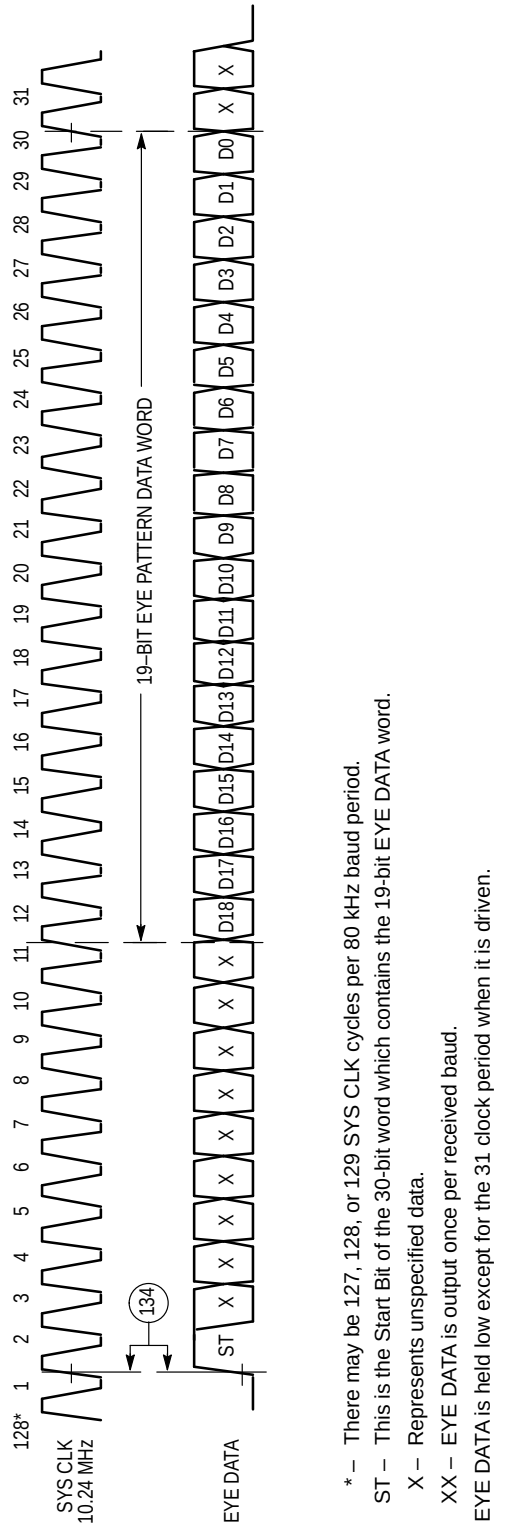

Figure 10–17. SYSCLK and EYE DATA Timing

10.14 SWITCHING CHARACTERISTICS FOR CRYSTAL INPUT, CLKOUT, BUF XTAL, AND FREQREF

(V_{DD} = 5.0 V ± 5%, T_A = – 40 to + 85°C, C_L = 50 pF; See Figure 10–14)

Ref. No.	Parameter	Min	Typ	Max	Unit
135a	FREQREF Minimum Pulse Width Low (LT Mode Only)	20	—	—	ns
135b	FREQREF Minimum Pulse Width High (LT Mode Only)	20	—	—	ns
136	BUF XTAL Duty Cycle at 20.48 MHz	45	50	55	%
137	BUF XTAL Output High to IDL Clock Output High (IDL Master Mode)	—	—	35	ns
138	BUF XTAL Output High to IDL Clock Output Low (IDL Master Mode)	—	—	35	ns
139	BUF XTAL Output Low to 4096 kHz Clock Output Low	—	—	35	ns
140	$XTAL_{in}$ Duty Cycle, for External Clock Source	45	—	55	%
141	LT Mode $XTAL_{in}$ to $XTAL_{out}$ Input Capacitance, FREQREF Connected to Either V_{DD} or V_{SS}			45	pF
142	LT Mode $XTAL_{in}$ to $XTAL_{out}$ Input Capacitance, FREQREF Much Greater Than 8 kHz.	15			pF
143	NT Mode $XTAL_{in}$ to $XTAL_{out}$ Input Capacitance.	15		45	pF
144	NT Mode Deactivated Condition $XTAL_{in}$ to $XTAL_{out}$ Input Capacitance.		24 pF		
145	$XTAL_{out}$ Drive Level		1		mW

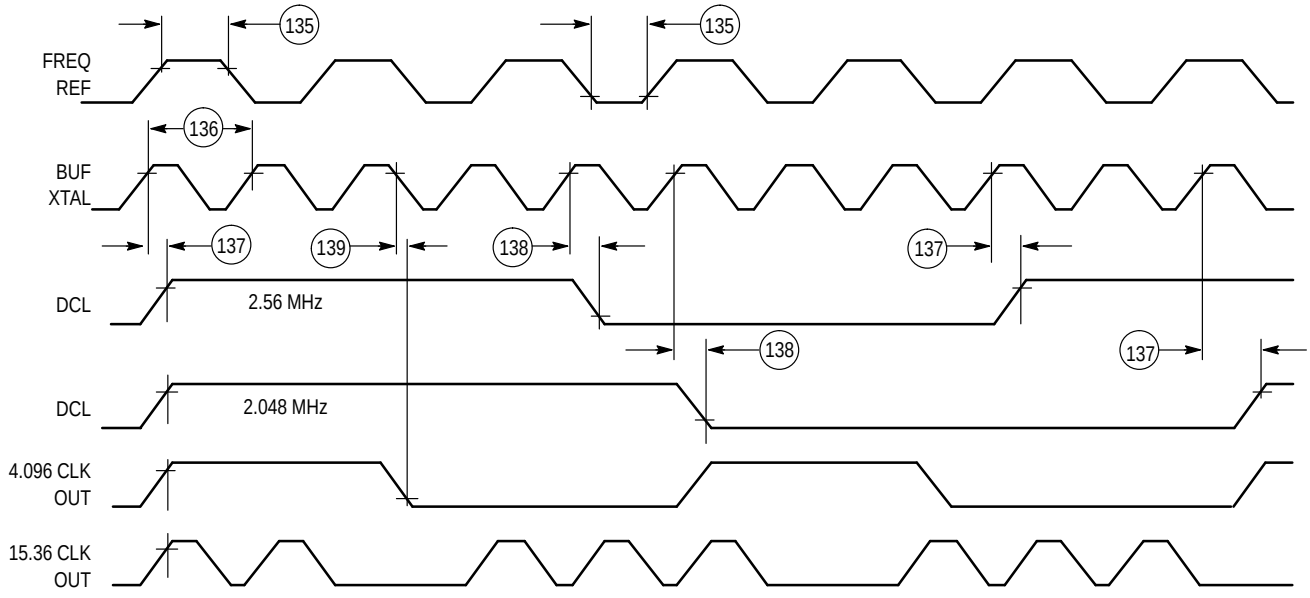

Figure 10–18. Clock Timing

10.15 SWITCHING CHARACTERISTICS FOR BAUD CLOCKS

(V_{DD} = 5.0 V ± 5%, T_A = – 40 to + 85°C, C_L = 50 pF; See Figure 10–15)

Ref. No.	Parameter	Min	Typ	Max	Unit
147	2B1Q Baud Period	—	12.5	—	µs
148	Start of 2B1Q Baud to Tx Baud Clock Rising Edge	—	9	—	µs
149	Tx Baud Clock Width High, Rx Baud Clock TxS_{FS}	75	90	100	ns
150	Superframe Period	—	12	—	ms

NOTE: Measurements are made from the point at which they achieve their guaranteed minimum or maximum logic levels.

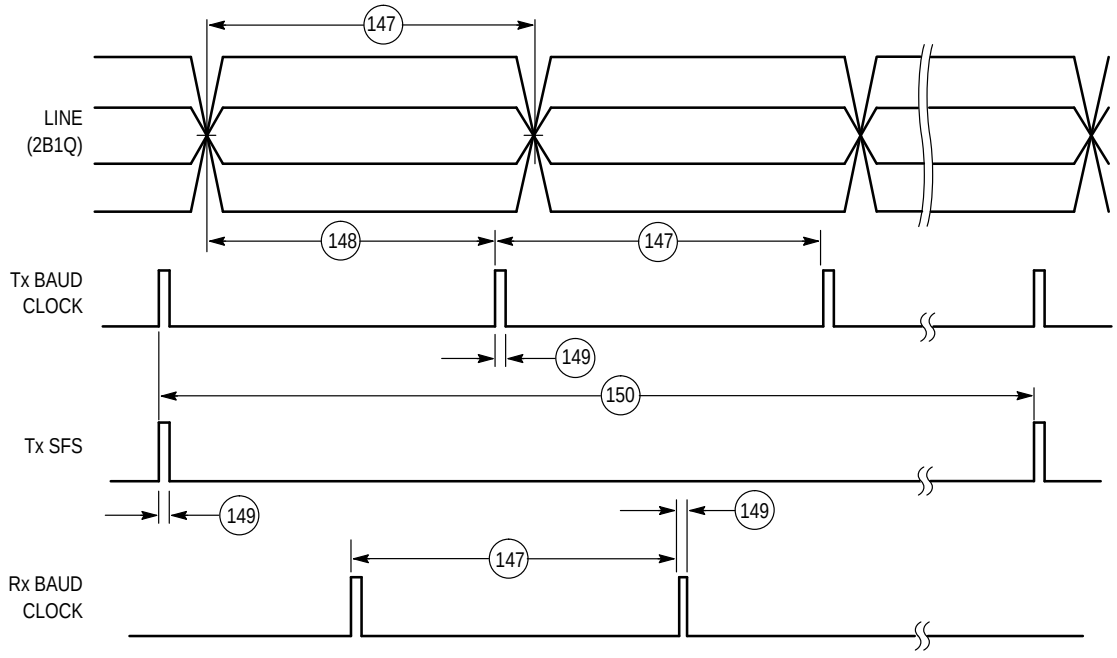

Figure 10–19. Baud Clock Timing

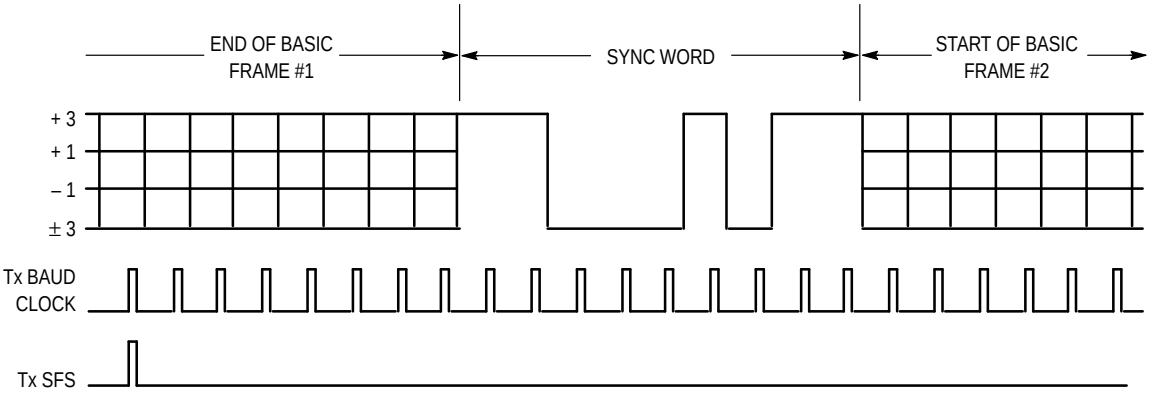

Figure 10–20. Tx Superframe Sync Pulse Alignment