Serial Input PLL Frequency Synthesizer

MC12206

MECL PLL COMPONENTS

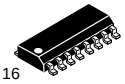
Serial Input PLL Frequency Synthesizer

The MC12206 is a 2.0GHz Bipolar monolithic serial input phase locked loop (PLL) synthesizer with pulse–swallow function. It is designed to provide the high frequency local oscillator signal of an RF transceiver in handheld communication applications.

Motorola's advanced Bipolar MOSAIC™ V technology is utilized for low power operation at a minimum supply voltage of 2.7V. The device is designed for operation over 2.7 to 5.5V supply range for input frequencies up to 2.0GHz with a typical current drain of 7.4mA. The low power consumption makes the MC12206 ideal for handheld battery operated applications such as cellular or cordless telephones, wireless LAN or personal communication services. A dual modulus prescaler is integrated to provide either a 64/65 or 128/129 divide ratio.

For additional applications information, two *InterActiveApNote*™ documents containing software (based on a Microsoft Excel spreadsheet) and an Application Note are available. Please order DK305/D and DK306/D from the Motorola Literature Distribution Center.

- Low Power Supply Current of 6.7mA Typical for I_{CC} and 0.7mA Typical for I_P
- Supply Voltage of 2.7 to 5.5V
- Dual Modulus Prescaler With Selectable Divide Ratios of 64/65 or 128/129
- On–Chip Reference Oscillator/Buffer
- Programmable Reference Divider Consisting of a Binary 14–Bit Programmable Reference Counter
- Programmable Divider Consisting of a Binary 7–Bit Swallow Counter and an 11–Bit Programmable Counter
- Phase/Frequency Detector With Phase Conversion Function
- Balanced Charge Pump Outputs
- Dual Internal Charge Pumps for Bypassing the First Stage of the Loop Filter to Decrease Lock Time
- Outputs for External Charge Pump
- Operating Temperature Range of –40°C to +85°C
- Space Efficient Plastic Surface Mount SOIC or TSSOP Packages



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E–03

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	Power Supply Voltage, Pin 4 (Pin 5 in 20–lead package)	–0.5 to +6.0	VDC
V_P	Power Supply Voltage, Pin 3 (Pin 4 in 20–lead package)	V_{CC} to +6.0	VDC
T_{stg}	Storage Temperature Range	–65 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

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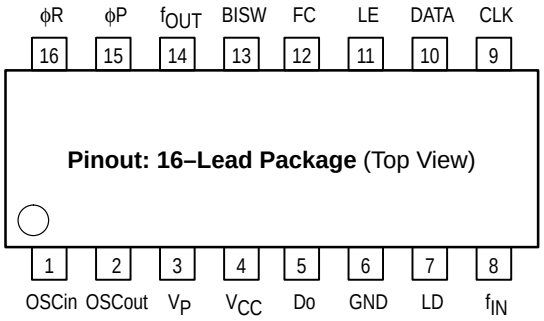
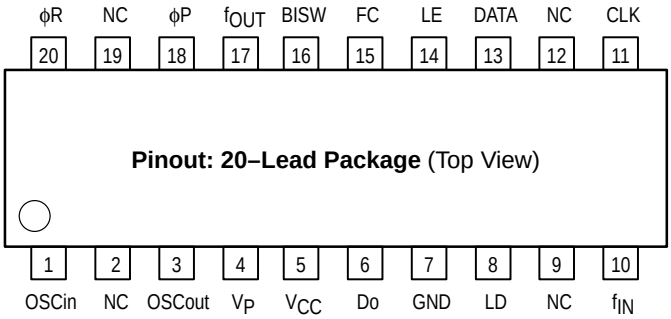


CASE 751B
ACTUAL SIZE



CASE 948E
ACTUAL SIZE

PIN NAMES

Pin	I/O	Function	16–Lead Pkg Pin No.	20–Lead Pkg Pin No.
OSCin	I	Oscillator input. A crystal is connected between OSCin and OSCout. An external source can be AC coupled into this input	1	1
OSCout	O	Oscillator output. Pin should be left open if external source is used	2	3
V_P	—	Power supply for charge pumps (V_P should be greater than or equal to V_{CC}) V_P provides power to the Do, BISW and ϕP outputs	3	4
V_{CC}	—	Power supply voltage input. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.	4	5
Do	O	Internal charge pump output. Do remains on at all times	5	6
GND	—	Ground	6	7
LD	O	Lock detect, phase comparator output	7	8
f_{IN}	I	Prescaler input. The VCO signal is AC–coupled into this pin	8	10
CLK	I	Clock input. Rising edge of the clock shifts data into the shift registers	9	11
DATA	I	Binary serial data input	10	13
LE	I	Load enable input (with internal pull up resistor). When LE is HIGH or OPEN, data stored in the shift register is transferred into the appropriate latch (depending on the level of control bit). Also, when LE is HIGH or OPEN, the output of the second internal charge pump is connected to the BISW pin	11	14
FC	I	Phase control select (with internal pull up resistor). When FC is LOW, the characteristics of the phase comparator and charge pump are reversed. FC also selects fp or fr on the f_{OUT} pin	12	15
BISW	O	Analog switch output. When LE is HIGH or OPEN (“analog switch is ON”) the output of the second charge pump is connected to the BISW pin. When LE is LOW, BISW is high impedance	13	16
f_{OUT}	O	Phase comparator input signal. When FC is HIGH, f_{OUT}=fr, programmable reference divider output; when FC is LOW, f_{OUT}=fp, programmable divider output	14	17
ϕP	O	Output for external charge pump. Standard CMOS output level	15	18
ϕR	O	Output for external charge pump. Standard CMOS output level	16	20
NC	—	No connect	—	2, 9, 12, 19

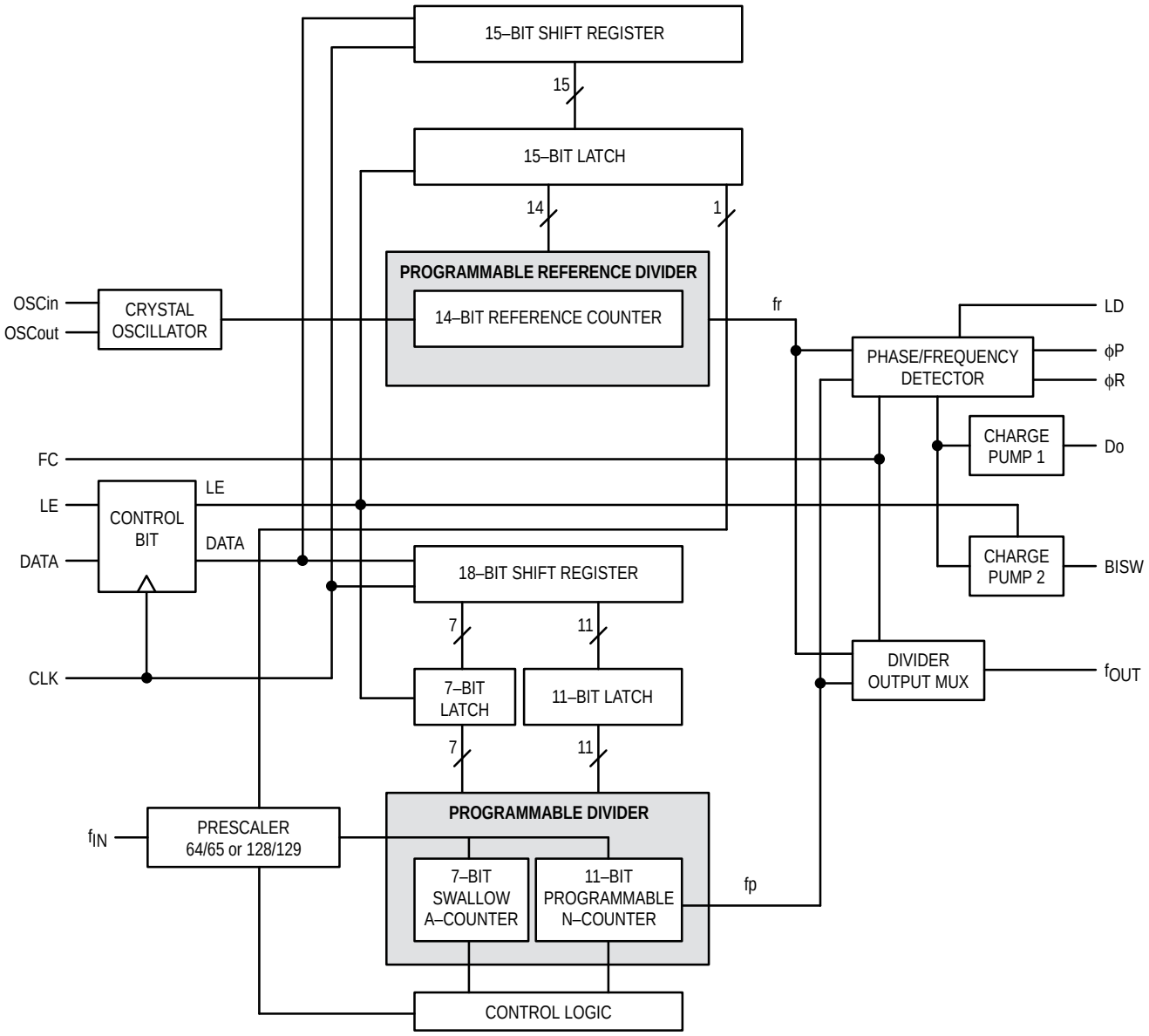


Figure 1. MC12206 Block Diagram

DATA ENTRY FORMAT

The three wire interface of DATA pin, CLK (clock) pin and LE (load enable) pin controls the serial data input of the 14–bit programmable reference divider plus the prescaler setting bit, and the 18–bit programmable divider. A rising edge of the clock shifts one bit of serial data into the internal shift registers. Depending upon the level of the control bit, stored data is transferred into the latch when load enable pin is HIGH or OPEN.

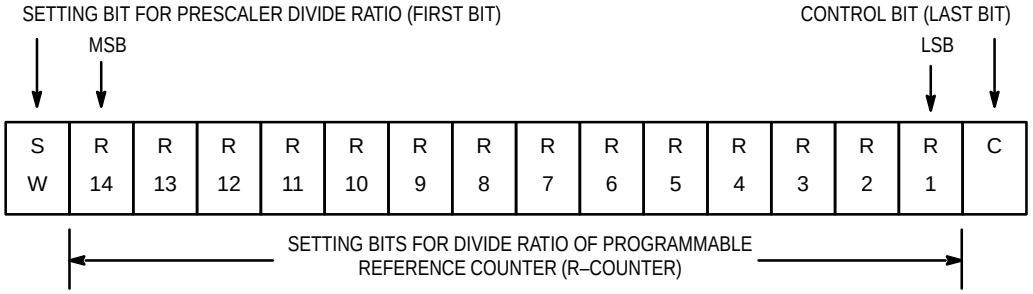
Control bit: "H" = data is transferred into 15–bit latch of programmable reference divider

"L" = data is transferred into 18–bit latch of programmable divider

PROGRAMMABLE REFERENCE DIVIDER

16–bit serial data format for the programmable reference counter, "R–counter", and prescaler select bit (SW) is shown below. If the control bit is HIGH, data is transferred from the 15–bit shift register into the 15–bit latch which specifies the R divide ratio (8 to 16383) and the prescaler divide ratio (SW=0 for ÷128/129, SW=1 for ÷64/65). An R divide ratio less than 8 is prohibited.

For Control bit (C) = HIGH:



DIVIDE RATIO OF PROGRAMMABLE REFERENCE (R) COUNTER

Divide Ratio R	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

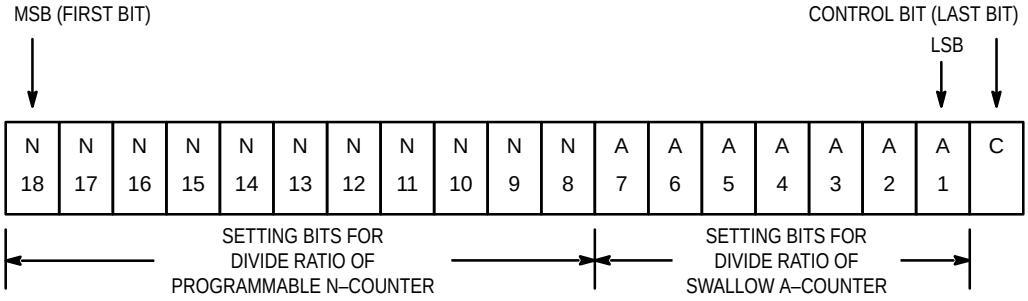
PRESCALER SELECT BIT

Prescaler Divide Ratio P	SW
128/129	0
64/65	1

PROGRAMMABLE DIVIDER

19–bit serial data format for the programmable divider is shown below. If the control bit is LOW, data is transferred from the 18–bit shift register into the 18–bit latch which specifies the swallow A–counter divide ratio (0 to 127) and the programmable N–counter divide ratio (16 to 2047). An N–counter divide ratio less than 16 is prohibited.

For Control bit (C) = LOW:



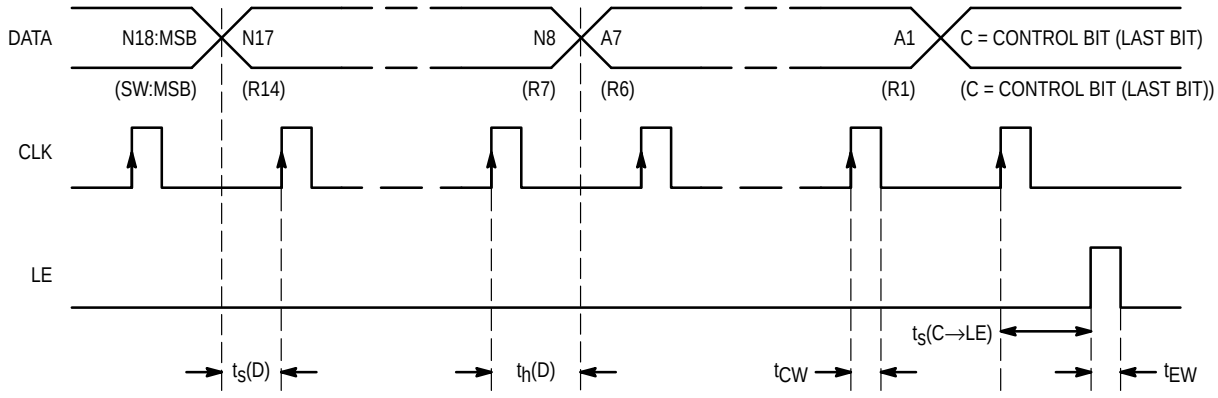
DIVIDE RATIO OF PROGRAMMABLE N–COUNTER **DIVIDE RATIO OF SWALLOW A–COUNTER**

Divide Ratio N	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8	Divide Ratio A	A 7	A 6	A 5	A 4	A 3	A 2	A 1
16	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1	127	1	1	1	1	1	1	1

DIVIDE RATIO SETTING

fvco = [(P•N)+A]•fosc ÷ R with A<N

- fvco: Output frequency of external voltage controlled oscillator (VCO)
- N: Preset divide ratio of binary 11–bit programmable counter (16 to 2047)
- A: Preset divide ratio of binary 7–bit swallow counter (0 to 127, A<N)
- fosc: Output frequency of the external frequency oscillator
- R: Preset divide ratio of binary 14–bit programmable reference counter (8 to 16383)
- P: Preset mode of dual modulus prescaler (64 or 128)



NOTES:Programmable reference divider data shown in parenthesis. Data shifted into register on rising edge of CLK.

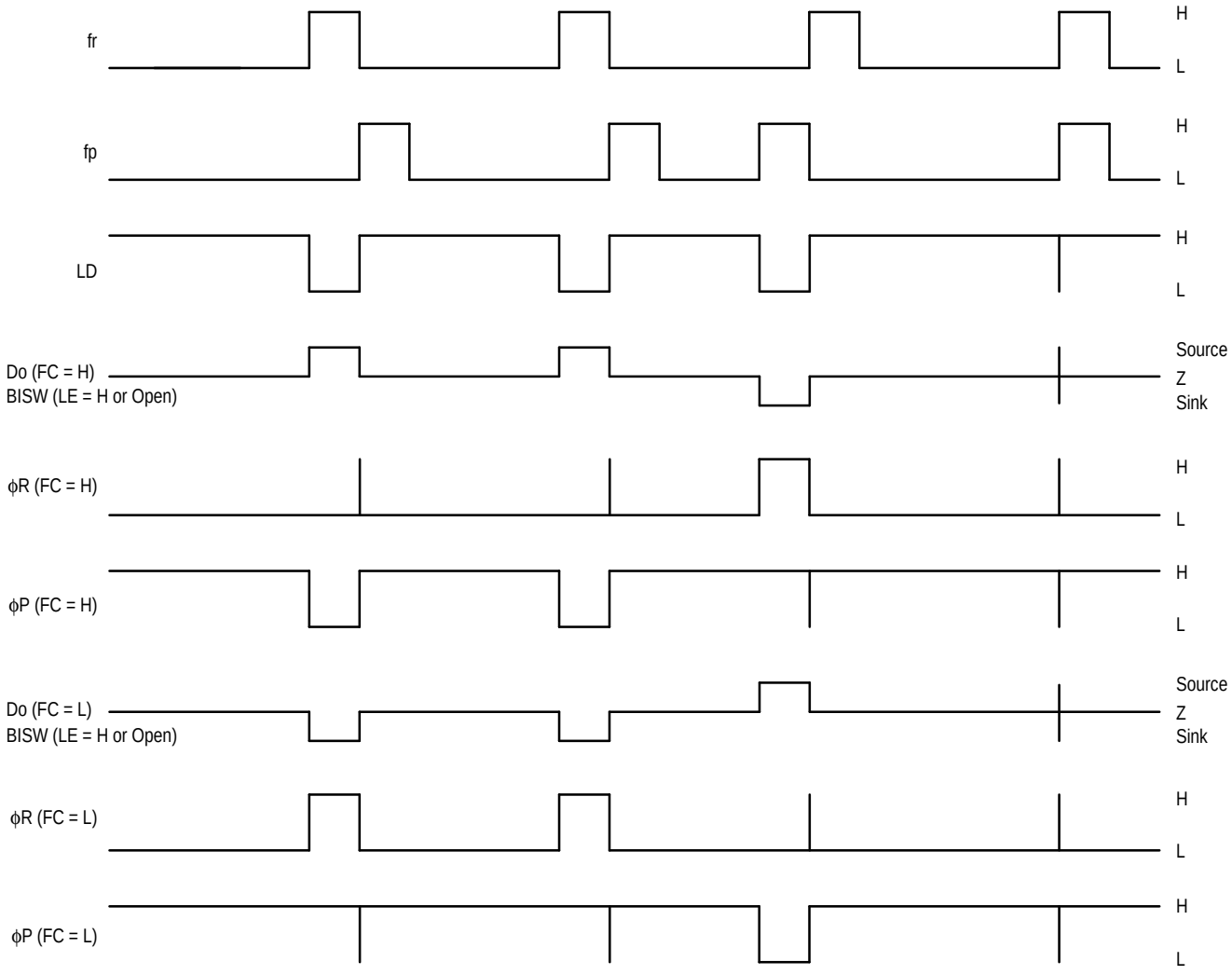
$t_S(D)$ = Setup Time DATA to CLK	$t_S(D) \geq 10ns$
$t_h(D)$ = Hold Time DATA to CLK	$t_h(D) \geq 20ns$
t_{CW} = CLK Pulse Width	$t_{CW} \geq 30ns$
t_{EW} = LE Pulse Width	$t_{EW} \geq 20ns$
$t_S(C \rightarrow LE)$ = Setup Time CLK to LE	$t_S(C \rightarrow LE) \geq 30ns$

Figure 2. Serial Data Input Timing

PHASE CHARACTERISTICS/VCO CHARACTERISTICS

The phase comparator in the MC12206 is a high speed digital phase frequency detector circuit. The circuit determines the “lead” or “lag” phase relationship and time difference between the leading edges of the VCO (fp) signal and the reference (fr) input. Since these edges occur only once per cycle, the detector has a range of $\pm 2\pi$ radians. The phase comparator outputs are standard CMOS rail–to–rail levels (V_P to GND for ϕP and V_{CC} to GND for ϕR), designed for up to 20MHz operation into a 15pF load. These phase comparator outputs can be used along with an external charge pump to enhance the PLL characteristics.

The operation of the phase comparator is shown in Figures NO TAG and NO TAG. The phase characteristics of the phase comparator are controlled by the FC pin. The polarity of the phase comparator outputs, ϕR and ϕP, as well as the charge pump output Do can be reversed by switching the FC pin.



NOTES: Do and BISW are current outputs.
Phase difference detection range: -2π to $+2\pi$
Spike difference depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.
When fr > fp or fr < fp, spike might not appear depending upon charge pump characteristics.

$$\text{Internal Charge Pump Gain} \approx \left| \frac{I_{source} + I_{sink}}{4\pi} \right| = \frac{4mA}{4\pi}$$

Figure 3. Phase/Frequency Detector, Internal Charge Pump and Lock Detect Waveforms

For FC = HIGH:
fr lags fp in phase OR fp>fr in frequency

When the phase of fr lags that of fp or the frequency of fp is greater than fr, the ϕP output will remain in a HIGH state while the ϕR output will pulse from LOW to HIGH. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕR indicates to the VCO to decrease in frequency to bring the loop into lock.

fr leads fp in phase OR fp<fr in frequency

When the phase of fr leads that of fp or the frequency of fp is less than fr, the ϕR output will remain in a LOW state while the ϕP output pulses from HIGH to LOW. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕP indicates to the VCO to increase in frequency to bring the loop to lock.

fr = fp in phase and frequency

When the phase and frequency of fr and fp are equal, the output ϕP will remain in a HIGH state and ϕR will remain in a LOW state except for voltage spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

When FC = LOW, the operation of the phase comparator is reversed from the above explanation.

For FC = LOW:
fr lags fp in phase OR fp>fr in frequency

When the phase of fr lags that of fp or the frequency of fp is greater than fr, the ϕR output will remain in a LOW state while the ϕP output will pulse from HIGH to LOW. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕP indicates to the VCO to increase in frequency to bring the loop into lock.

fr leads fp in phase OR fp<fr in frequency

When the phase of fr leads that of fp or the frequency of fp is less than fr, the ϕP output will remain in a HIGH state while the ϕR output pulses from LOW to HIGH. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on ϕR indicates to the VCO to decrease in frequency to bring the loop to lock.

fr = fp in phase and frequency

When the phase and frequency of fr and fp are equal, the output ϕP will remain in a HIGH state and ϕR will remain in a LOW state except for voltage spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

The FC pin controls not only the phase characteristics, but also controls the f_{OUT} test pin. The FC pin permits the user to monitor either of the phase comparator input signals, fr or fp, at the f_{OUT} output providing a test mode where the programming of the dividers and the output of the counters can be checked. When FC is HIGH, f_{OUT} = fr, the programmable reference divider output. When FC is LOW, f_{OUT} = fp, the programmable divider output.

Hence,

If VCO characteristics are like (1), FC should be set HIGH or OPEN. f_{OUT} = fr

If VCO characteristics are like (2), FC should be set LOW. f_{OUT} = fp

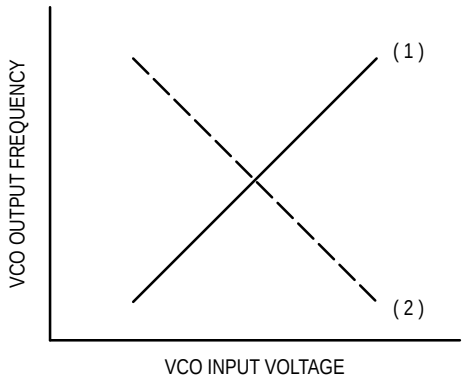


Figure 4. VCO Characteristics

	FC = HIGH or OPEN				FC = LOW			
	Do	**ϕR**	**ϕP**	**f_{OUT}**	**Do**	**ϕR**	**ϕP**	**f_{OUT}**
fp < fr	H	L	L	fr	L	H	H	fp
fp > fr	L	H	H	fr	H	L	L	fp
fp = fr	Z	L	H	fr	Z	L	H	fp

NOTES: Z = High impedance
When LE is HIGH or Open, BISW has the same characteristics as Do.

Figure 5. Phase Comparator, Internal Charge Pump, and f_{OUT} Characteristics

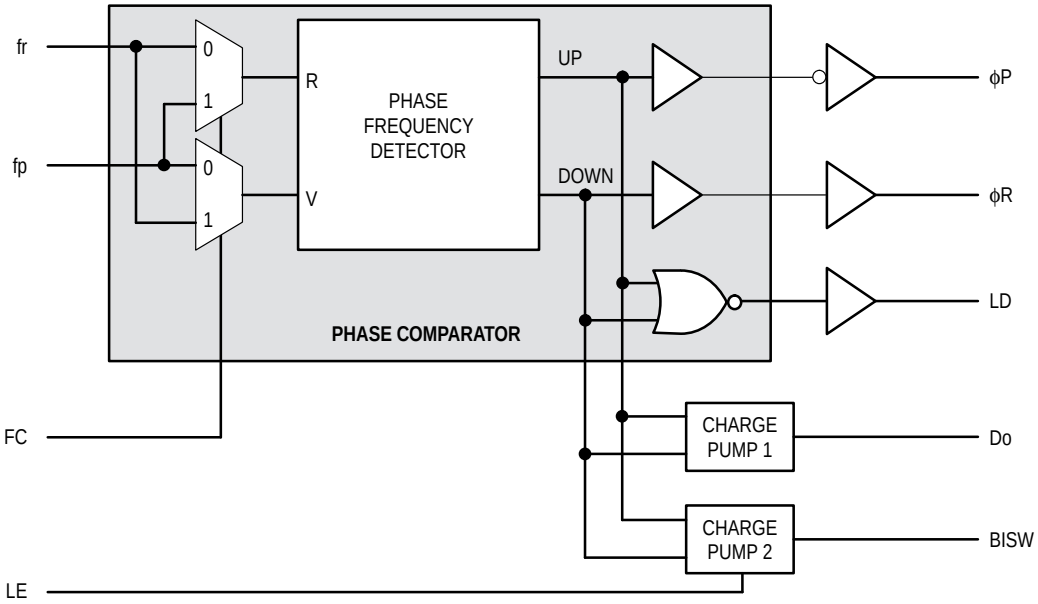


Figure 6. Detailed Phase Comparator Block Diagram

LOCK DETECT

The Lock Detect (LD) output pin provides a LOW pulse when fr and fp are not equal in phase or frequency. The output is normally HIGH. LD is designed to be the logical NORing of the phase frequency detector's outputs UP and DOWN. See Figure NO TAG. In typical applications the output signal drives external circuitry which provides a steady LOW signal when the loop is locked. See Figure NO TAG.

OSCILLATOR INPUT

The device incorporates an on–chip reference oscillator/buffer so that an external parallel–resonant fundamental crystal can be connected between OSCin and OSCout. External capacitor C1 and C2 as shown in Figure NO TAG are required to set the proper crystal load capacitance and oscillator frequency. The values of the capacitors are dependent on the crystal chosen (up to a maximum of 30 pF each including parasitic and stray capacitance).

If an external reference oscillator is available, the signal should be AC–coupled to the OSCin pin through a coupling capacitor. In this case, no connection to OSCout is required. The magnitude of the AC–coupled signal must be between 500 and 2200 mV peak–to–peak.

DUAL INTERNAL CHARGE PUMPS ("ANALOG SWITCH")

Due to the pure Bipolar nature of the MC12206 design, the "analog switch" function is implemented with dual internal charge pumps. The loop filter time constant can be decreased by bypassing the first stage of the loop filter with the charge pump output BISW as shown in Figure NO TAG below. This enables the VCO to lock in a shorter amount of time.

When LE is HIGH or OPEN ("analog switch is ON"), the output of the second internal charge pump is connected to the BISW pin, and the Do output is ON. The charge pump 2 output on BISW is essentially equal to the charge pump 1 output on Do. When LE is LOW, BISW is in a high impedance state and Do output is active.

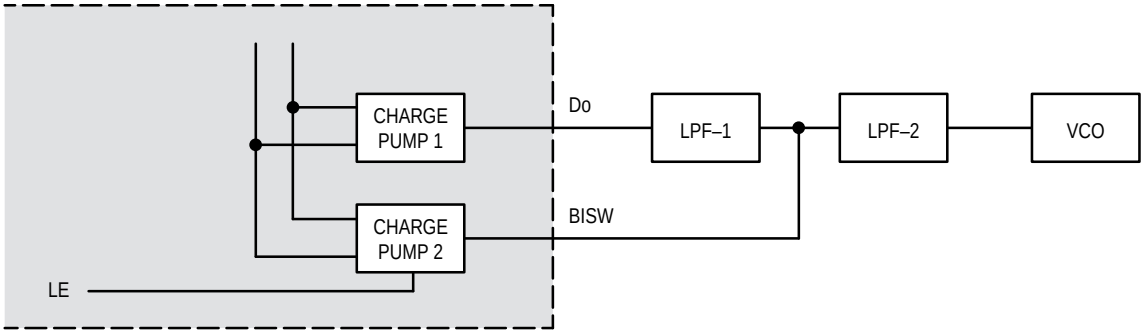


Figure 7. "Analog Switch" Block Diagram

ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 to 5.5V; T_A = –40 to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
I_{CC}	Supply Current for V_{CC}		6.7	10.5	mA	Note 1
			8.1	12.5		Note 2
I_P	Supply Current for V_P		0.7	1.1	mA	Note 3
			0.8	1.3		Note 4
F_{IN}	Operating Frequency f_{IN}max f_{IN}min	2000		 500	MHz	Note 5
F_{OSC}	Operating Frequency (OSCin)		12	20	MHz	Crystal Mode
				40	MHz	External Reference Mode
V_{IN}	Input Sensitivity f_{IN}	200		1000	$mV_{P–P}$	
V_{OSC}	OSCin	500		2200	$mV_{P–P}$	
V_{IH}	Input HIGH Voltage CLK, DATA, LE, FC	$0.7V_{CC}$			V	
V_{IL}	Input LOW Voltage CLK, DATA, LE, FC			$0.3V_{CC}$	V	V_{CC} = 5.5V
I_{IH}	Input HIGH Current (DATA and CLK)		1.0	2.0	µA	V_{CC} = 5.5V
I_{IL}	Input LOW Current (DATA and CLK)	–10	–5.0		µA	V_{CC} = 5.5V
I_{OSC}	Input Current (OSCin)		130 –310		µA	OSCin = V_{CC} OSCin = V_{CC} – 2.2V
I_{IH}	Input HIGH Current (LE and FC)		1.0	2.0	µA	
I_{IL}	Input LOW Current (LE and FC)	–75	–60		µA	
I_{Source}[6]	Charge Pump Output Current	–2.6	–2.0	–1.4	mA	V_{Do} = V_P/2; V_P = 2.7V
I_{Sink}[6]	Do and BISW	+1.4	+2.0	+2.6		V_{BISW} = V_P/2; V_P = 2.7V
$I_{Hi–Z}$		–15		+15	nA	0.5 < V_{DO} < V_P – 0.5 0.5 < V_{BISW} < V_P – 0.5
V_{OH}	Output HIGH Voltage (LD, ϕR, ϕP, f_{OUT})	4.4			V	V_{CC} = 5.0V
		2.4			V	V_{CC} = 3.0V
V_{OL}	Output LOW Voltage (LD, ϕR, ϕP, f_{OUT})			0.4	V	V_{CC} = 5.0V
				0.4	V	V_{CC} = 3.0V
I_{OH}	Output HIGH Current (LD, ϕR, ϕP, f_{OUT})	–1.0			mA	
I_{OL}	Output LOW Current (LD, ϕR, ϕP, f_{OUT})	1.0			mA	

1. V_{CC} = 3.3V, all outputs open.
2. V_{CC} = 5.5V, all outputs open.
3. V_P = 3.3V, all outputs open.
4. V_P = 6.0V, all outputs open.
5. AC coupling, F_{IN} measured with a 1000pF capacitor.
6. Source current flows out of the pin and sink current flows into the pin.

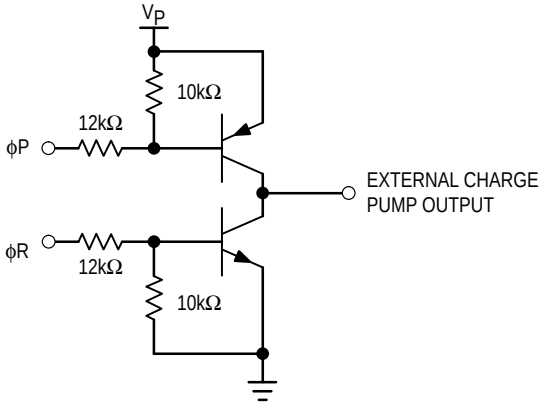


Figure 8. Typical External Charge Pump Circuit

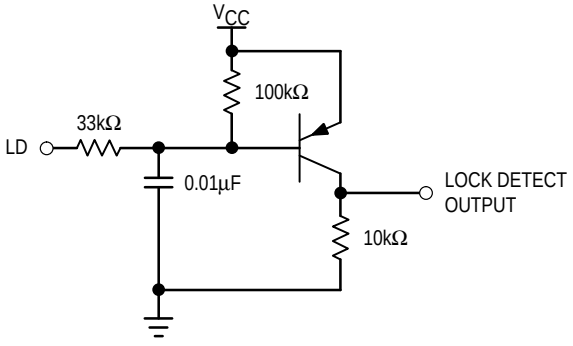
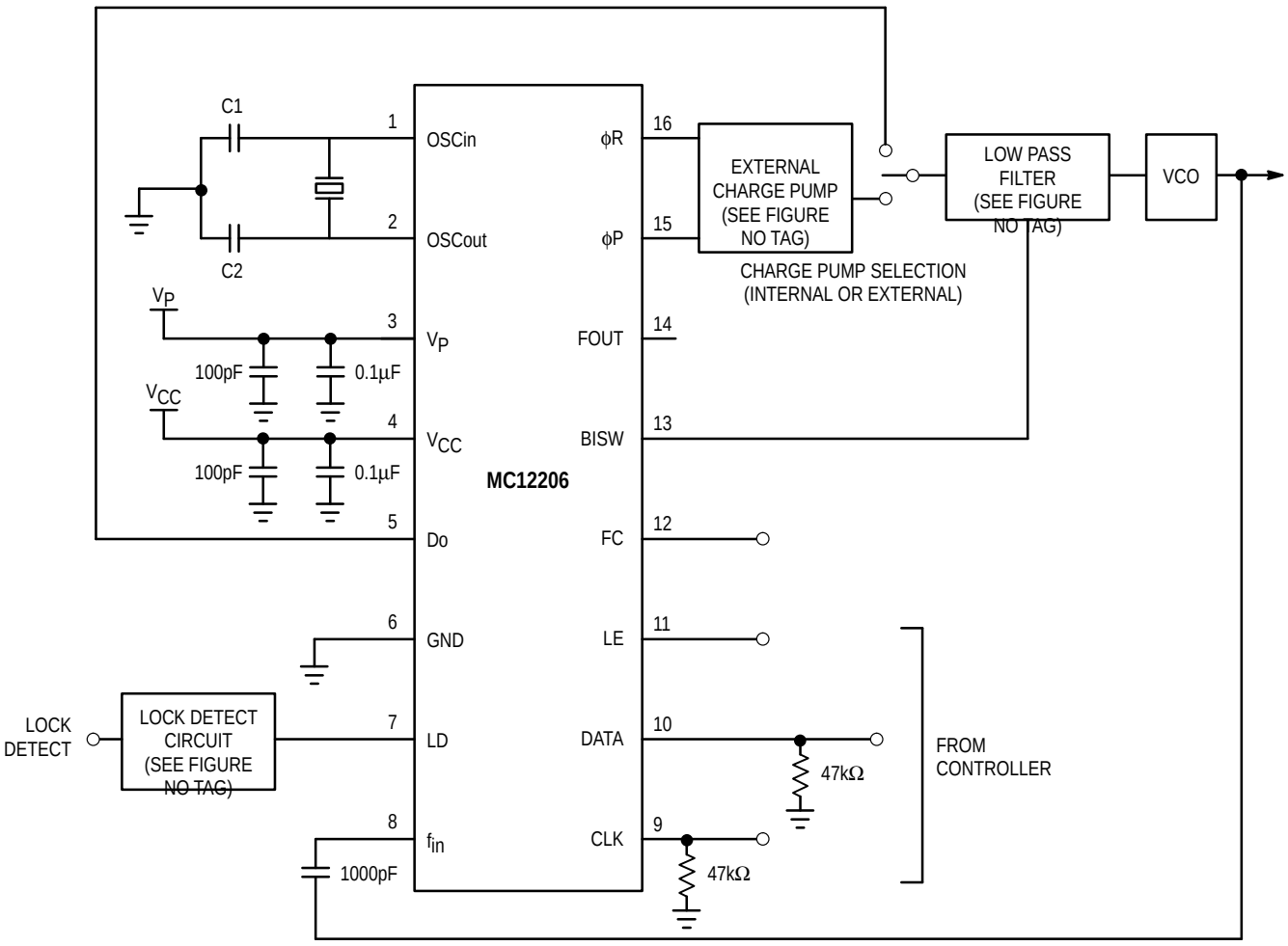


Figure 9. Typical Lock Detect Circuit



C1, C2: Dependent on Crystal Oscillator

Figure 10. Typical Applications Example (16–Pin Package)

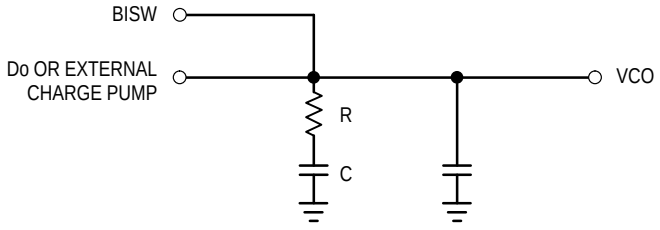
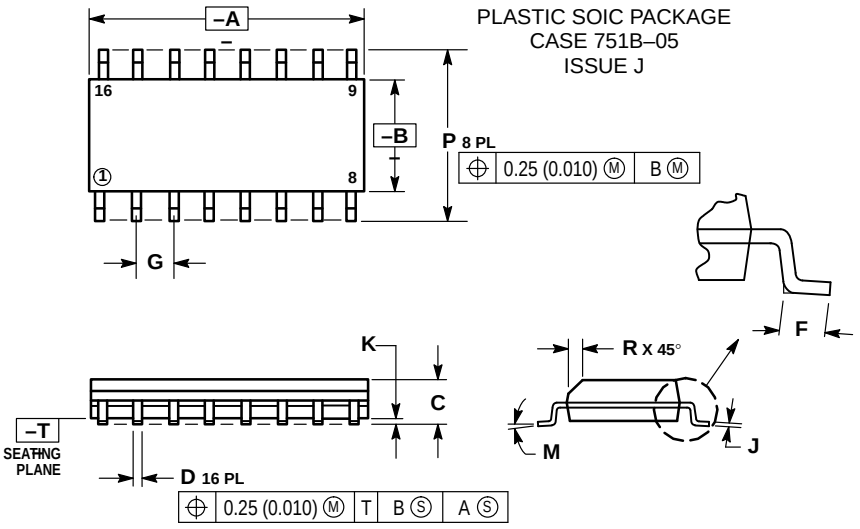


Figure 11. Typical Loop Filter

OUTLINE DIMENSIONS

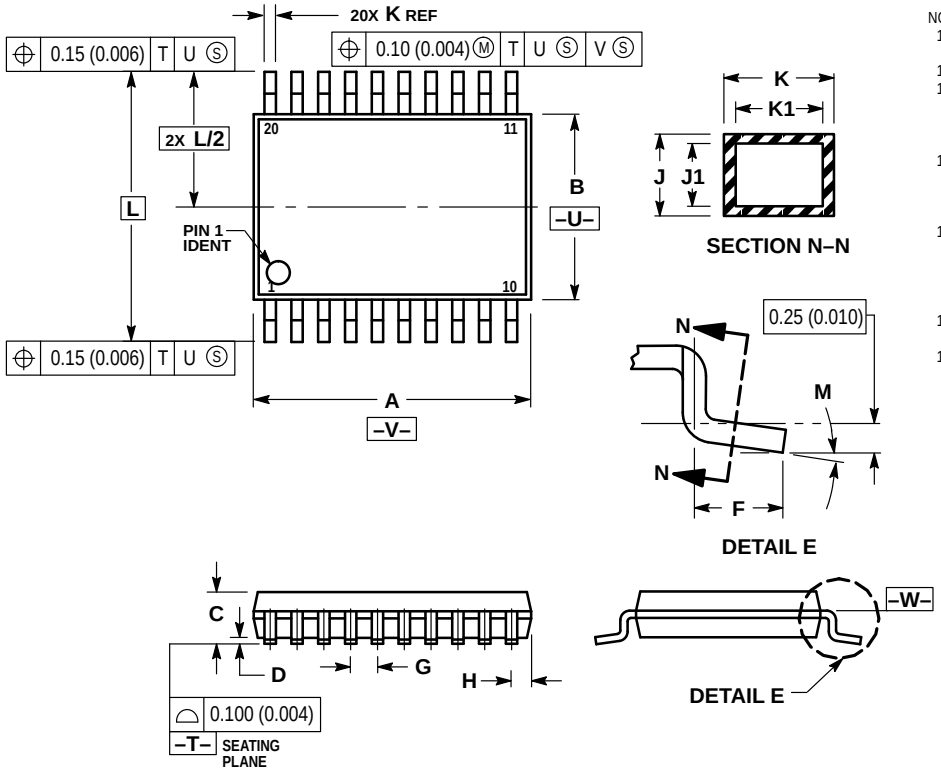
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A



NOTES:
12 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
13 CONTROLLING DIMENSION: MILLIMETER.
14 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
15 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
16 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
17 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
18 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

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