# 2.0GHz Dual Modulus Prescaler

**MC12032A**
**MC12032B**

**MECL PLL COMPONENTS**

**÷64/65, ÷128/129**
**DUAL MODULUS**
**PRESCALER**

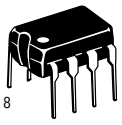
The MC12032A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 2.0GHz in programmable frequency steps.

The MC12032B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5V
- MC12032A for Positive Edge Triggered Synthesizers
- MC12032B for Negative Edge Triggered Synthesizers
- 12mA Maximum, –40° to +85°C, $V_{CC}$ = 5.5Vdc
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL
- Low–Power 8.5mA Typical




**P SUFFIX**
PLASTIC PACKAGE
CASE 626–05

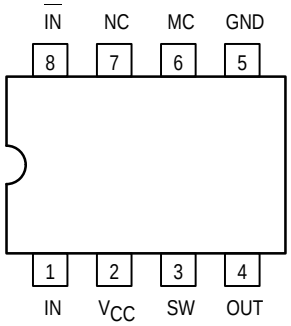

**D SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751–05

**FUNCTIONAL TABLE**

| SW | MC | Divide Ratio |
|---|---|---|
| H | H | 64 |
| H | L | 65 |
| L | H | 128 |
| L | L | 129 |

Note: SW: H = $V_{CC}$, L = Open
MC: H = 2.0 V to $V_{CC}$, L = GND to 0.8 V

**Pinout: 8–Lead Plastic** (Top View)




**DESIGN GUIDE**

| Criteria | Value | Unit |
|---|---|---|
| Internal Gate Count* | 67 | ea |
| Internal Gate Propagation Delay | 200 | ps |
| Internal Gate Power Dissipation | 0.75 | mW |
| Speed Power Product | 0.15 | pJ |

* Equivalent to a two–input NAND gate

**MAXIMUM RATINGS**

| Symbol | Characteristic | Range | Unit |
|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage, Pin 2 | –0.5 to + 7.0 | Vdc |
| $T_A$ | Operating Temperature Range | –40 to + 85 | °C |
| $T_{stg}$ | Storage Temperature Range | –65 to + 150 | °C |
| MC | Modulus Control Input, Pin 6 | –0.5 to + 6.5 | Vdc |







MOTOROLA

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 4.5 to 5.5V; $T_A$ = –40°C to +85°C)

| Symbol | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_t$ | Toggle Frequency (Sine Wave Input) | 0.5 | 2.4 | 2.0 | GHz |
| $I_{CC}$ | Supply Current Output Unloaded (Pin 2) | | 8.5 | 12 | mA |
| $V_{IH1}$ | Modulus Control Input High (MC) | 2.0 | | $V_{CC}$ + 0.5V | V |
| $V_{IL1}$ | Modulus Control Input Low (MC) | | | 0.8 | V |
| $V_{IH2}$ | Divide Ratio Control Input High (SW) | $V_{CC}$ – 0.5V | $V_{CC}$ | $V_{CC}$ + 0.5V | Vdc |
| $V_{IL2}$ | Divide Ratio Control Input Low (SW) | Open | Open | Open | — |
| $V_{out}$ | Output Voltage Swing ($C_L$ = 12pF; $R_L$ = 2.2kΩ) | 1.0 | 1.6 | | $V_{p–p}$ |
| $t_{set}$ | Modulus Setup Time MC to Out | | 8.0 | 10 | ns |
| $V_{in(min)}$ | Input Voltage Sensitivity 500–2000 MHz | 100 | | 1500 | mVpp |
| $I_O$ | Output Current ($C_L$ = 12pF; $R_L$ = 2.2kΩ) | | 1.5 | 4.0 | mA |

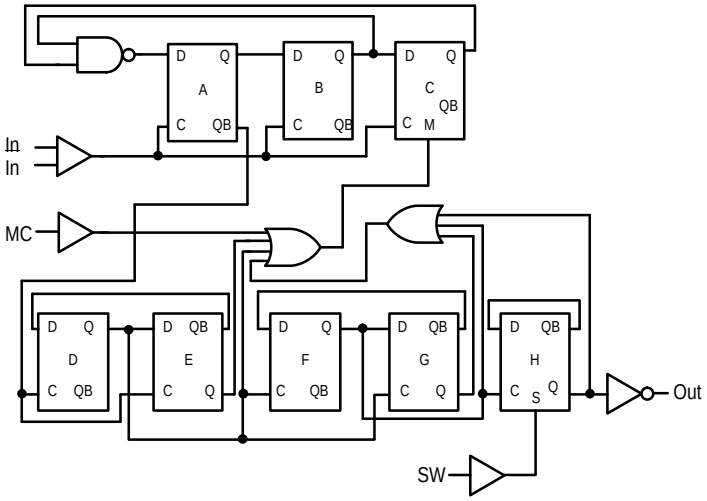
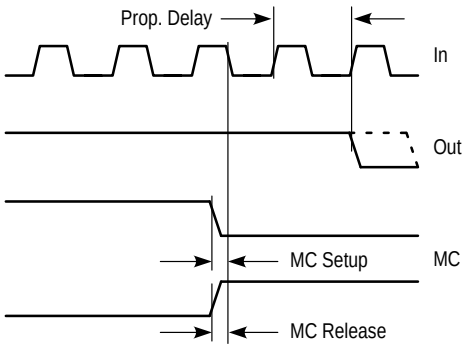
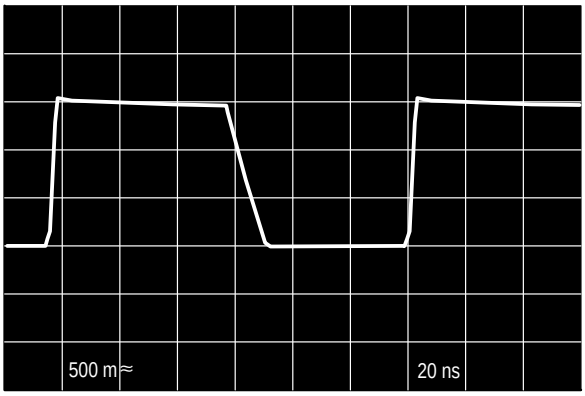



**Figure 1. Logic Diagram (MC12032A)**

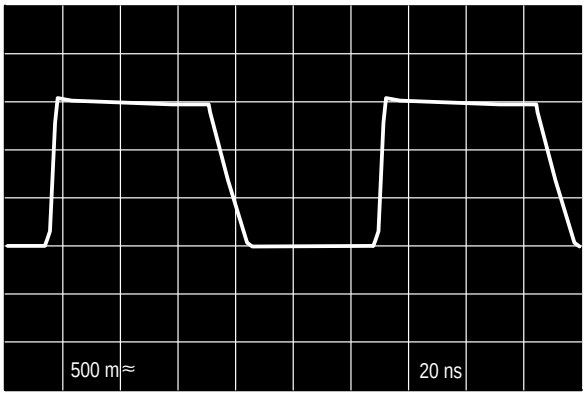



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

**Figure 2. Modulus Setup Time**




(÷64, 500MHz Input Frequency, $V_{CC}$ = 5.0V, $T_A$ = 25°C, Output Loaded)




(÷128, 1.1GHz Input Frequency, $V_{CC}$ = 5.0V, $T_A$ = 25°C, Output Loaded)

**Figure 3. Typical Output Waveforms**

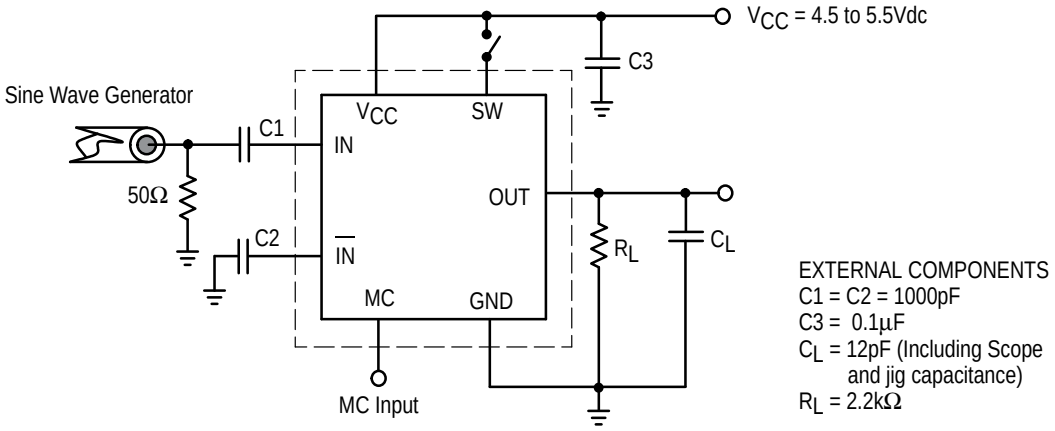



**Figure 4. AC Test Circuit**

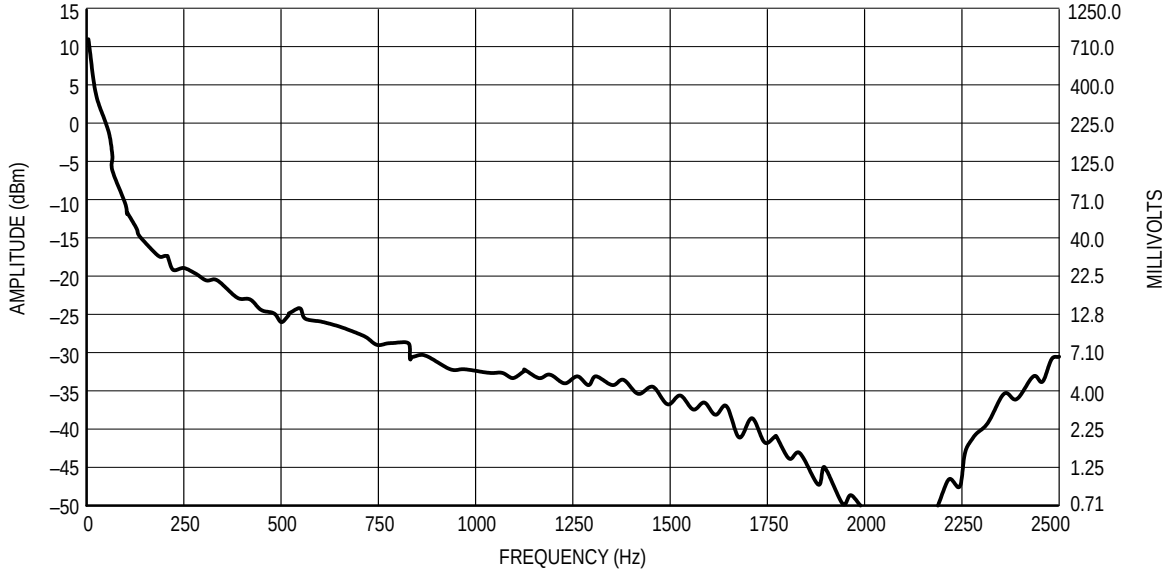



**Figure 5. Input Signal Amplitude versus Input Frequency**
Divide Ratio = 128

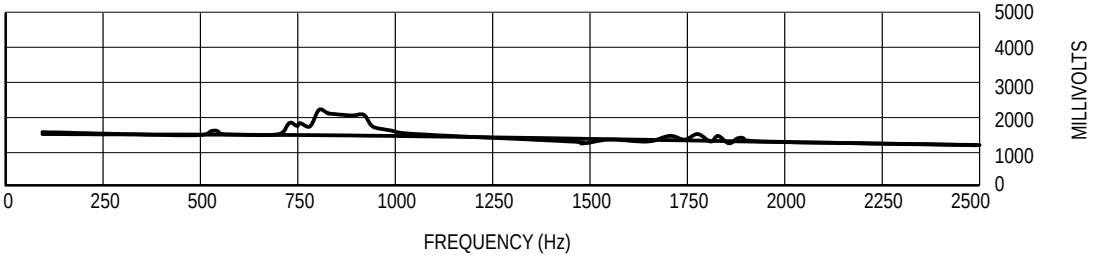



**Figure 6. Output Amplitude versus Input Frequency**

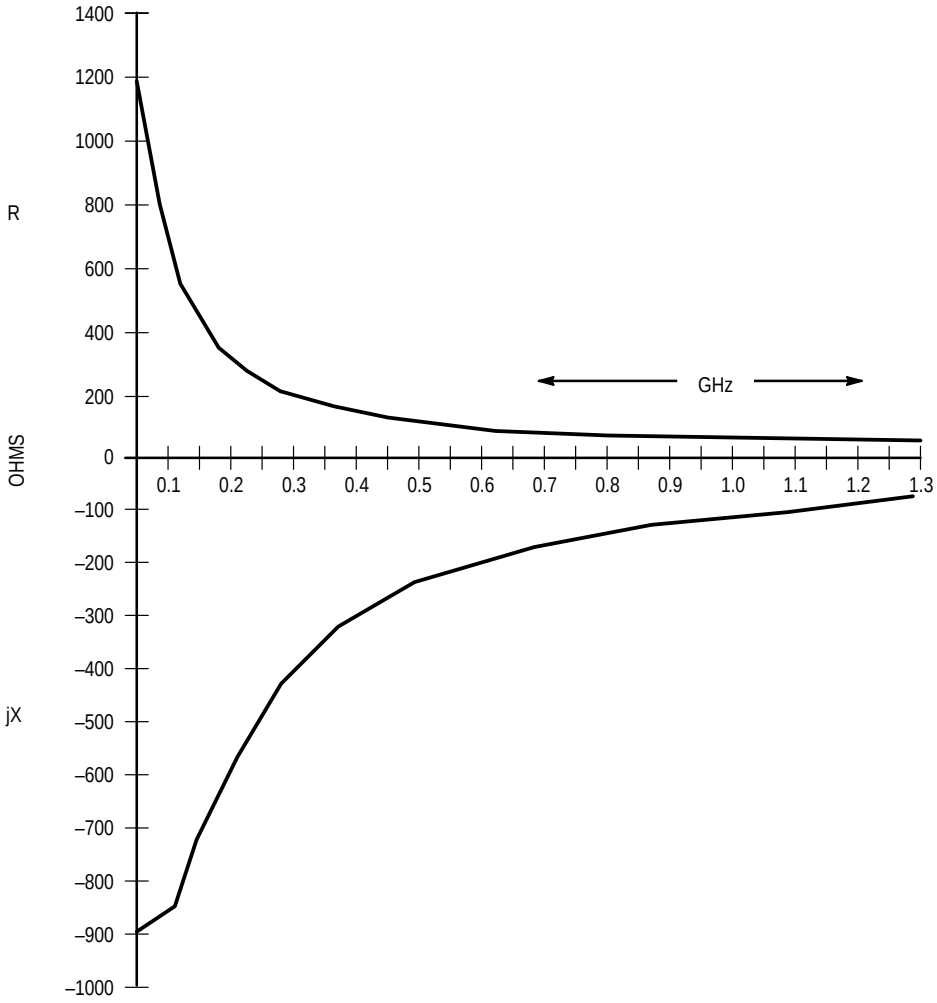
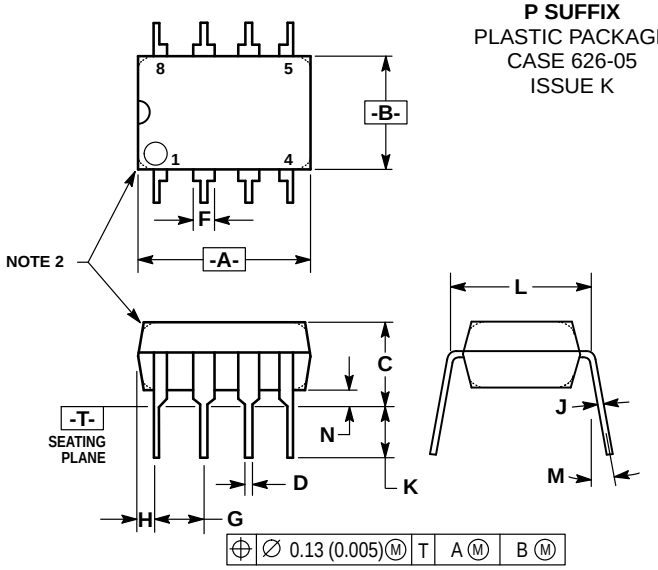



**Figure 7. Typical Input Impedance versus Input Frequency**

## OUTLINE DIMENSIONS

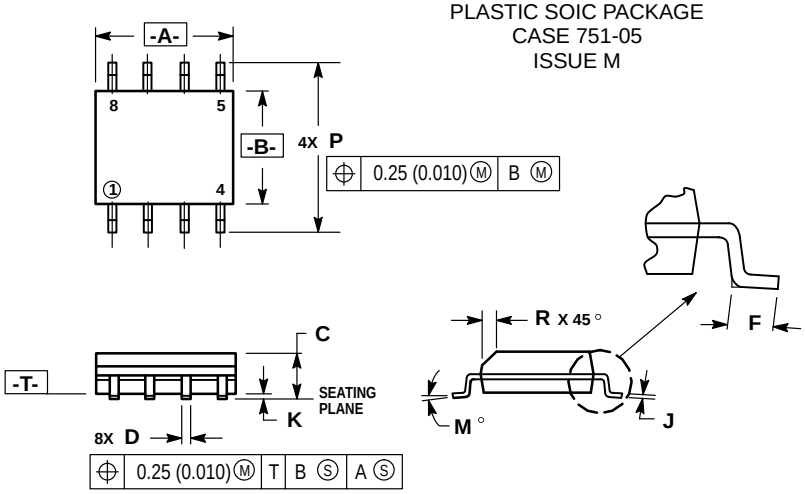
**P SUFFIX**
PLASTIC PACKAGE
CASE 626-05
ISSUE K




NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.40 | 10.16 | 0.370 | 0.400 |
| B | 6.10 | 6.60 | 0.240 | 0.260 |
| C | 3.94 | 4.45 | 0.155 | 0.175 |
| D | 0.38 | 0.51 | 0.015 | 0.020 |
| F | 1.02 | 1.78 | 0.040 | 0.070 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 0.76 | 1.27 | 0.030 | 0.050 |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 7.62 BSC | | 0.300 BSC | |
| M | — | 10° | — | 10° |
| N | 0.76 | 1.01 | 0.030 | 0.040 |

**D SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751-05
ISSUE M




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.196 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.18 | 0.25 | 0.007 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |



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