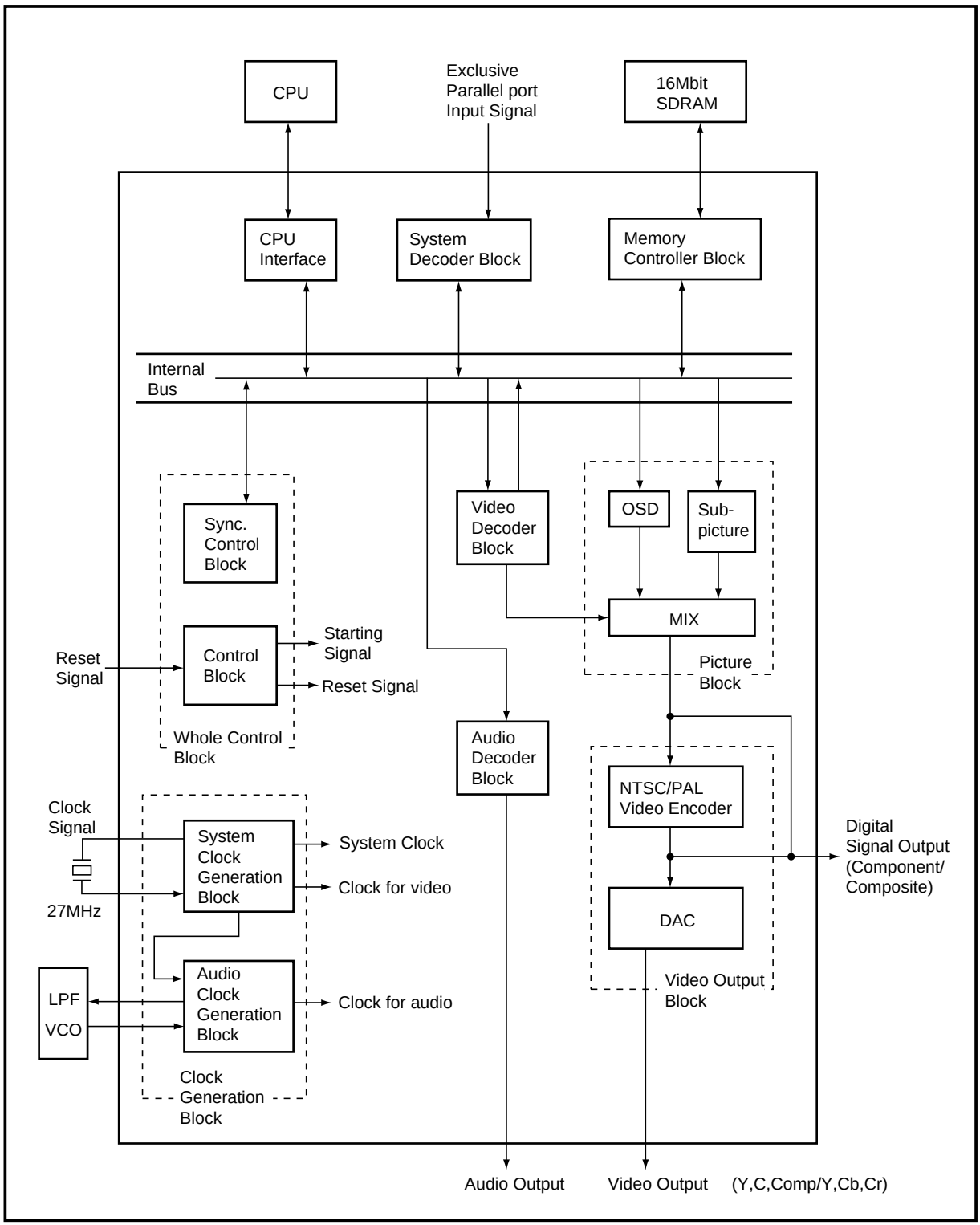
● **Block Diagram**



● **Pin Function**

No.	Pin Name	I/O	Function	No.	Pin Name	I/O	Function
1	CLKSEL	I	ON/OFF signal of PLL ("H" : ON, "L" : OFF)	27	VDD	–	2.5V power supply
2	DIGCPN7	O	Digital component signal output (MSB) Digital Y signal output (9-bit) (MSB)	28	DIGCOMP4	O	Digital composite signal output Digital C signal output
3	VSS	–	GND	29	DIGCOMP3		
4	DIGCPN6	O	Digital component signal output Digital Y signal output (9-bit)	30	DIGCOMP2		
5	DIGCPN5			31	DIGCOMP1		
6	DIGCPN4			32	DIGCOMP0		Digital composite signal output (LSB) Digital C signal output (LSB)
7	DIGCPN3			33	DACK	O	27 MHz clock output
8	DIGCPN2			34	N.C.	–	Non connection
9	DIGCPN1			35	VSSA3	–	GND (D/A converter)
10	VDD	–	2.5V power supply	36	ANAC	O	Analog color (C) output signal
11	DIGCPN0	O	Digital component signal output (LSB) Digital Y signal output (9-bit) (LSB)	37	VDDA3	–	2.5V power supply (for built-in D/A converter only)
12	RBSEL	O	Cb and Cr discrimination signal at the digital component signal output. LSB at the digital Y signal output.	38	VSSA2	–	GND (D/A converter)
13	XHS	O	Horizontal sync. output signal	39	ANAY	O	Analog luminance (Y) output signal
14	XVS	O	Vertical sync. output signal	40	VDDA2	–	2.5V power supply (for built-in D/A converter only)
15	VSS	–	GND	41	VREF	I	Reference voltage for D/A converter
16	XRESET	I	LSI reset signal	42	VRO	O	Internal current setting pin of D/A converter
17	XLDCSYNC	I	External sync. signal input (LD mode)	43	VDDA4	–	2.5V power supply (for built-in D/A converter only)
18	KEY	O	KEY signal for LD and OSD overlay (LD mode)	44	VSSA1	–	GND (D/A converter)
19	PD	O	Phase comparison result output signal of horizontal sync. (LD mode)	45	ANACOMP	O	Analog composite output signal
20	VFLD	O	Field discrimination signal at the digital signal output H : even field L : odd field	46	VDDA1	–	2.5V power supply (for built-in D/A converter only)
21	DIGCOMP9	O	Digital composite signal output (MSB) Digital C signal output (MSB)	47	BF	O	Burst flag signal
22	DIGCOMP8		Digital composite signal output Digital C signal output	48	XBLK	O	H/V composite blanking signal
23	DIGCOMP7			49	TEST4	O	Normally, set to "open".
24	DIGCOMP6			50	VSS	–	GND
25	DIGCOMP5			51	TEST0	I	Normally, set to "open".
26	VSS	–	GND	52	TEST1	I	"L" status normally

No.	Pin Name	I/O	Function	No.	Pin Name	I/O	Function
53	DAIIN	I	Digital data input of external input (SPDIF)	92	HADRS10	I	CPU address bus signal (MSB)
54	CDDATA	I	Audio data input of external input (correspond to CD)	93	HADRS9	I	CPU address bus signal
55	CDLR	I	Data channel clock input of external input (correspond to CD)	94	HADRS8		
56	CDBCK	I	Data clock input of external input (correspond to CD)	95	HADRS7		
57	AODATA3	O	Audio decode data	96	VSS	–	GND
58	AODATA2			97	VDD	–	2.5V power supply
59	AODATA1			98	HADRS6	I	CPU address bus signal
60	VSS	–	GND	99	HADRS5		
61	VDD	–	2.5V power supply	100	HADRS4		
62	AODATA0	O	Audio decode data	101	HADRS3		
63	AOPCM	O	Digital audio interface output (compression data)	102	HADRS2		CPU address bus signal (LSB)
64	AODAI	O	Digital audio interface output (decode data)	103	HDATA15	I/O	CPU data bus signal (MSB)
65	LRCK	O	Data channel clock for D/A and digital filter	104	HDATA14		CPU data bus signal
66	AOMCK	O	Master clock for D/A and digital filter	105	HDATA13		
67	BCK	O	Bit clock for D/A and digital filter	106	HDATA12		
68	TEST2	I	Normally, set to "open".	107	VSS	–	GND
69	TEST3			108	HDATA11	I/O	CPU data bus signal
70	NC	–	Non connection	109	HDATA10		
71	XDSPRST	I	Normally, set to "open".	110	HDATA9		
72	VSS	–	GND	111	HDATA8		
73	TEST5	O	Normally, set to "open".	112	HDATA7		
74	NC	–	Normally, set to "open".	113	HDATA6		
75	NC			114	VDD	–	2.5V power supply
76	NC			115	HDATA5	I/O	CPU data bus signal
77	NC			116	HDATA4		
78	SD7	I	Parallel data input	117	HDATA3		
79	VDD	–	2.5V power supply	118	HDATA2		
80	SD6	I	Parallel data input	119	VSS	–	GND
81	SD5			120	HDATA1	I/O	CPU data bus signal
82	SD4			121	HDATA0		CPU data bus signal (LSB)
83	SD3			122	BUSSEL	I	Bus width selection signal (0 : 8-bit bus, 1 : 16-bit bus)
84	SD2			123	XOSDACK	I	OSD data acknowledge signal
85	VSS	–	GND	124	XOSDREQ	O	OSD data request signal
86	SD1	I	Parallel data input	125	HCPUSEL1	I	CPU selection signal (00 :SPARC, 01 :86 system, 10 :68 system, 11 :Reserve)
87	SD0			126	HCPUSEL0		
88	XERR	I	Error input signal	127	XINT3	O	Interrupt request signal to the CPU
89	XSACK	I	Acknowledge signal	128	XINT2		
90	XTEST	I	Set to "H" at normal use	129	XINT1		
91	SREQ	O	Data request signal	130	VSS	–	GND

No.	Pin Name	I/O	Function	No.	Pin Name	I/O	Function
131	VDD	–	2.5V power supply	170	XMDRCAS	O	CAS signal for SDRAM
132	XINT0	O	Interrupt request signal to CPU	171	XMDRDQM1	O	Input mask / output enable signal for SDRAM
133	XEXTRDY	O	SPARC, 68 system : Ready signal to CPU 86 system : Acknowledge (ACK) signal to CPU	172	VSS	–	GND
134	HRW	I	CPU read / write signal	173	XMDRWE	O	Write enable signal for SDRAM
135	HCLKIN	I	Host clock input	174	XMDRDQM0	O	Input mask / output enable signal for SDRAM
136	XHCS	I	LSI chip select signal	175	MDRDAT8	I/O	Data bus signal for SDRAM
137	XHAS	I	SPARC, 68 system : CPU address strobe 86 system : CPU address status	176	VSS	–	GND
138	XHBE3	I	CPU byte enable signal	177	MDRDAT7	I/O	Data bus signal for SDRAM
139	XHBE2			178	MDRDAT9		
140	XHBE1			179	MDRDAT6		
141	XHBE0			180	MDRDAT10		
142	VSS	–	GND	181	MDRDAT5		
143	MDRADR4	O	Address signal for SDRAM	182	VSS	–	GND
144	MDRADR3			183	VDD	–	2.5V power supply
145	MDRADR5			184	MDRDAT11	I/O	Data bus signal for SDRAM
146	MDRADR2			185	MDRDAT4		
147	VDD	–	2.5V power supply	186	MDRDAT12		
148	VSS	–	GND	187	MDRDAT3		
149	MDRADR6	O	Address signal for SDRAM	188	MDRDAT13		
150	MDRADR1			189	VSS	–	GND
151	MDRADR7			190	MDRDAT2	I/O	Data bus signal for SDRAM
152	MDRADR0		Address signal for SDRAM (LSB)	191	MDRDAT14		
153	MDRADR8		Address signal for SDRAM	192	MDRDAT1		
154	VSS	–	GND	193	MDRDAT15		Data bus signal for SDRAM (MSB)
155	TEST6	I	"L" status normally	194	MDRDAT0	I/O	Data bus signal for SDRAM (LSB)
156	TEST7			195	VSS	–	GND
157	TEST8			196	N.C.	–	Non connection
158	TEST9			197	ICK27M	I	System clock input
159	MDRADR10	O	Address signal for SDRAM	198	VSS	–	GND
160	MDRADR9			199	OCK27M	O	System clock output
161	MDRADR11		Address signal for SDRAM (MSB)	200	VSSA(VCO)	–	GND (for VCO only)
162	XMDRCS	O	Chip select signal for SDRAM	201	VDDA(VCO)	–	2.5V power supply (for VCO only)
163	MDRCKE	O	Clock enable signal for SDRAM	202	ILPF	O	PLL block inverter output for audio
164	VSS	–	GND	203	MLPF	I	PLL block inverter input for audio
165	VDD	–	2.5V power supply	204	OLPF	O	Phase detector output for audio
166	XMDRRAS	O	RAS signal for SDRAM	205	OVCO	I	VCO input for audio clock
167	MDRCLK	O	Clock output signal for SDRAM	206	VSS	–	GND
168	VSS	–	GND	207	XPLLRST	I	PLL section reset signal
169	MDRCLKIN	I	Clock input signal for SDRAM	208	XSYNCRST	I	SYNC reset signal