19-2223; Rev 0; 10/01

MAXIM

Quad Differential LVECL/LVPECL Buffer/Receivers

General Description

The MAX9400/MAX9402/MAX9403/MAX9405 are extremely fast, low-skew quad LVECL/ECL or LVPECL/PECL buffer/receivers designed for high-speed data and clock driver applications. These devices feature an ultra-low propagation delay of 335ps and channel-to-channel skew of 16ps in asynchronous mode with 86mA supply current.

The four channels can be operated synchronously with an external clock, or in asynchronous mode determined by the state of the SEL input. An enable input provides the ability to force all the outputs to a differential low state.

A variety of input and output terminations are offered for maximum design flexibility. The MAX9400 has open inputs and open emitter outputs. The MAX9402 has open inputs and 50Ω series outputs. The MAX9403 has 100Ω differential input impedance and open emitter outputs. The MAX9405 has 100Ω differential input impedance and 50Ω series outputs.

These devices operate with a supply voltage of (V_{CC} - V_{EE}) = +2.375V to +5.5V, and are specified for operation from -40°C to +85°C. These devices are offered in space-saving 32-pin 5mm × 5mm TQFP and 32-lead 5mm × 5mm QFN packages.

Applications

Data and Clock Driver and Buffer

Central Office Backplane Clock Distribution

DSLAM Backplane

Base Station

ATE

Functional Diagram appears at end of data sheet.

Features

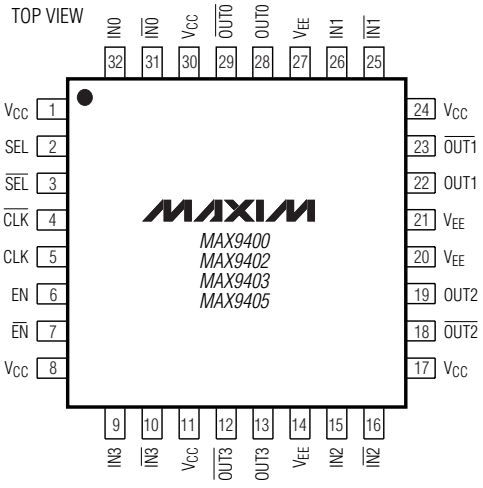
- **400mV Differential Output at 3.0GHz Data Rate**
- **335ps Propagation Delay in Asynchronous Mode**
- **8ps Channel-to-Channel Skew in Synchronous Mode**
- **Integrated 50Ω Outputs (MAX9402/MAX9405)**
- **Integrated 100Ω Inputs (MAX9403/MAX9405)**
- **Synchronous/Asynchronous Operation**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	DATA INPUT	OUTPUT
MAX9400EHJ	-40°C to +85°C	32 TQFP	Open	Open
MAX9400EGJ*	-40°C to +85°C	32 QFN	Open	Open
MAX9402EHJ*	-40°C to +85°C	32 TQFP	Open	50Ω
MAX9402EGJ*	-40°C to +85°C	32 QFN	Open	50Ω
MAX9403EHJ	-40°C to +85°C	32 TQFP	100Ω	Open
MAX9403EGJ*	-40°C to +85°C	32 QFN	100Ω	Open
MAX9405EHJ*	-40°C to +85°C	32 TQFP	100Ω	50Ω
MAX9405EGJ*	-40°C to +85°C	32 QFN	100Ω	50Ω

**Future product—contact factory for availabilty.*

Pin Configurations



TQFP (5mm x 5mm)

Pin Configurations continued at end of data sheet.

Quad Differential LVECL/LVPECL Buffer/Receivers

ABSOLUTE MAXIMUM RATINGS

V_{CC} to V_{EE} .....-0.3V to +6V
Inputs to V_{EE}.....-0.3V to (V_{CC} + 0.3V)
Differential Input Voltage .....±3V
Continuous Output Current.....50mA
Surge Output Current.....100mA
Continuous Power Dissipation (T_A = +70°C)
32-Pin 5mm x 5mm TQFP
(derate 9.5mW/°C above +70°C).....761mW
32-Lead 5mm x 5mm QFN
(derate 21.3mW/°C above +70°C).....1.7W
Junction-to-Ambient Thermal Resistance in Still Air
32-Pin 5mm x 5mm TQFP.....+105°C/W
32-Lead 5mm x 5mm QFN .....+47°C/W
Junction-to-Ambient Thermal Resistance with 500LFPM Airflow
32-Pin 5mm x 5mm TQFP.....+73°C/W
Junction-to-Case Thermal Resistance
32-Pin 5mm x 5mm TQFP.....+25°C/W
32-Lead 5mm x 5mm QFN .....+2°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
ESD Protection
Human Body Model (Inputs and Outputs).....2kV
Soldering Temperature (10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = +2.375V to +5.5V, MAX9400/MAX9403 outputs terminated with 50Ω ±1% to V_{CC} - 2.0V. Typical values are at V_{CC} - V_{EE} = +3.3V, V_{IHD} = V_{CC} - 0.9V, V_{ILD} = V_{CC} - 1.7V, T_A = +25°C, unless otherwise noted.) (Notes 1, 2, and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUTS (IN_, $\overline{IN\_}$, CLK, $\overline{CLK}$, EN, $\overline{EN}$, SEL, $\overline{SEL}$)							
Differential Input High Voltage	V_{IHD}	Figure 1		V_{EE} + 1.4		V_{CC}	V
Differential Input Low Voltage	V_{ILD}	Figure 1		V_{EE}		V_{CC} - 0.2	V
Differential Input Voltage	V_{ID}	Figure 1	V_{CC} - V_{EE} < +3.0V	0.2		V_{CC} - V_{EE}	V
			V_{CC} - V_{EE} ≥ +3.0V	0.2		3.0	
Input Current	I_{IH}, I_{IL}	MAX9400/ MAX9402	EN, $\overline{EN}$, SEL, $\overline{SEL}$, IN_, $\overline{IN\_}$, CLK, or $\overline{CLK}$ = V_{IHD} or V_{ILD}	-10		25	µA
		MAX9403/ MAX9405	EN, $\overline{EN}$, SEL, $\overline{SEL}$, CLK, or $\overline{CLK}$ = V_{IHD} or V_{ILD}	-10		25	
Differential Input Resistance	R_{IN}	MAX9403/MAX9405		86		114	Ω
OUTPUTS (OUT_, $\overline{OUT\_}$)							
Differential Output Voltage	V_{OH} - V_{OL}	Figure 1		600	660		mV
Output Common-Mode Voltage	V_{OCM}	Figure 1		V_{CC} - 1.5	V_{CC} - 1.25	V_{CC} - 1.05	V
Internal Current Source	I_{SINK}	MAX9402/MAX9405, Figure 2			8.0		mA
Output Impedance	R_{OUT}	MAX9402/MAX9405, Figure 2			45		Ω
POWER SUPPLY							
Supply Current	I_{EE}	MAX9402/MAX9405			155		mA
		MAX9400/MAX9403			86	118	

AC ELECTRICAL CHARACTERISTICS

(V_{CC} - V_{EE} = +2.375V to +5.5V, outputs terminated with 50Ω ±1% to V_{CC} - 2.0V, enabled, CLK = 3.2GHz, f_{IN} = 1.6GHz, input transition time = 125ps (20% to 80%), V_{IHD} = V_{EE} + 1.2V to V_{CC}, V_{ILD} = V_{EE} to V_{CC} - 0.2V, V_{IHD} - V_{ILD} = 0.2V to smaller of |V_{CC} - V_{EE}| or 3V, unless otherwise noted. Typical values are at V_{CC} - V_{EE} = +3.3V, V_{IHD} = V_{CC} - 0.9V, V_{ILD} = V_{CC} -1.7V, T_A = +25°C, unless otherwise noted.) (Notes 1, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IN to OUT Differential Propagation Delay	t_{PLH1} t_{PHL1}	MAX9400/MAX9403	SEL = high, Figure 3	237	335	437	ps
		MAX9402/MAX9405					
CLK to OUT Differential Propagation Delay	t_{PLH2} t_{PHL2}	MAX9400/MAX9403	SEL = low, Figure 4	397	475	597	ps
		MAX9402/MAX9405					
IN to OUT Channel-to-Channel Skew (Note 5)	t_{SKD1}	SEL = high			16	80	ps
CLK to OUT Channel-to-Channel Skew (Note 5)	t_{SKD2}	SEL = low			8	55	ps
Maximum Clock Frequency	$f_{CLK(MAX)}$	V_{OH} - V_{OL} ≥ 500mV, SEL = low		3.0			GHz
Maximum Data Frequency	$f_{IN(MAX)}$	V_{OH} - V_{OL} ≥ 400mV, SEL = high		2			GHZ
Added Random Jitter (Note 6)	t_{RJ}	SEL = low, f_{CLK} = 3.0GHz clock, f_{IN} = 1.5GHz			0.64	1.3	$ps_{(RMS)}$
		SEL = high, f_{IN} = 2GHz			0.74	1.5	
Added Deterministic Jitter (Note 6)	t_{DJ}	SEL = low, f_{CLK} = 3.0GHz, IN_ = 3.0Gbps 2^{23} - 1 PRBS pattern			17	30	ps(p-p)
		SEL = high, IN = 2.0Gbps 2^{23} - 1 PRBS pattern			40	55	
IN-to-CLK Setup Time	t_S	Figure 4		80			ps
CLK-to-IN Hold Time	t_H	Figure 4		80			ps
Output Rise Time	t_R	Figure 3			80	120	ps
Output Fall Time	t_F	Figure 3			80	120	ps
Propagation Delay Temperature Coefficient	$\Delta t_{PD}/\Delta T$					1	ps/°C

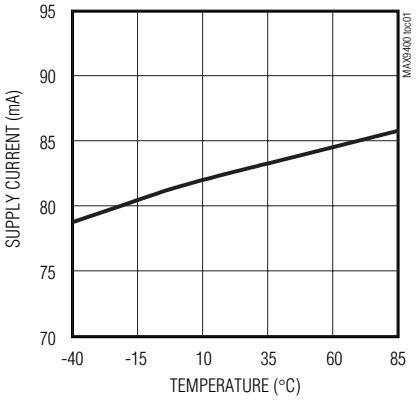
Note 1: Measurements are made with the device in thermal equilibrium.
Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.
Note 3: DC parameters are production tested at +25°C. DC limits are guaranteed by design and characterization over the full operating temperature range.
Note 4: Guaranteed by design and characterization. Limits are set to ±6 sigma.
Note 5: Measured between outputs of the same part at the signal crossing points for a same-edge transition.
Note 6: Device jitter added to the input signal.

Quad Differential LVECL/LVPECL Buffer/Receivers

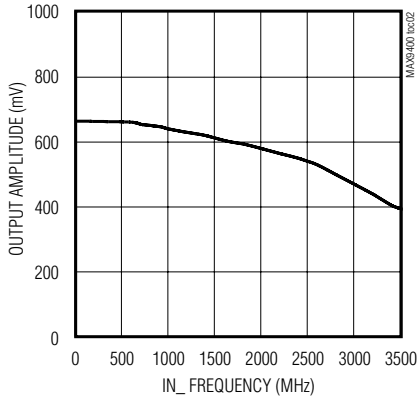
Typical Operating Characteristics

(V_{CC} - V_{EE} = +3.3V, MAX9400, outputs terminated with 50Ω ±1% to V_{CC} - 2.0V, enabled, SEL = high, CLK = 2.0GHz, f_{IN} = 1.0GHz, input transition time = 125ps (20% to 80%), V_{IHD} = V_{CC} - 1.0V, V_{ILD} = V_{CC} - 1.5V, T_A = +25°C, unless otherwise noted.)

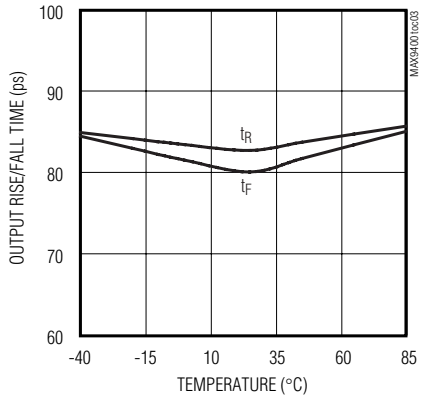
SUPPLY CURRENT (I_{EE}) vs. TEMPERATURE



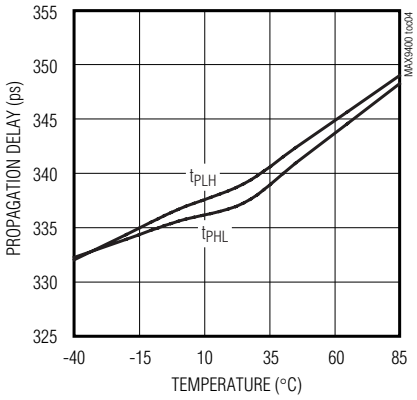
OUTPUT AMPLITUDE (V_{OH} - V_{OL}) vs. IN_ FREQUENCY



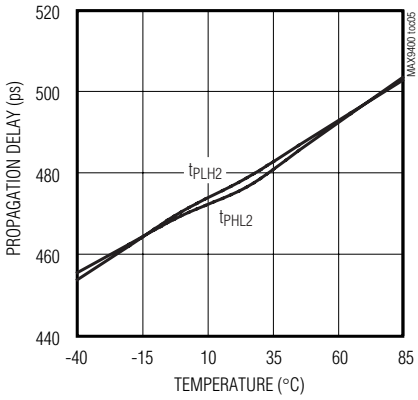
OUTPUT RISE/FALL vs. TEMPERATURE



IN-TO-OUT PROPAGATION DELAY vs. TEMPERATURE



CLK-TO-OUT PROPAGATION DELAY vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1, 8,11, 17, 24, 30	V_{CC}	Positive Supply Voltage. Bypass V_{CC} to V_{EE} with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
2	SEL	Noninverting Differential Select Input. Setting SEL = high and $\overline{SEL}$ = low (differential high) enables all four channels to operate asynchronously. Setting SEL = low and $\overline{SEL}$ = high (differential low) enables all four channels to operate in synchronous mode.
3	$\overline{SEL}$	Inverting Differential Select Input
4	$\overline{CLK}$	Inverting Differential Clock Input. A rising edge on CLK (and falling on $\overline{CLK}$) transfers data from the inputs to the outputs when SEL = low.
5	CLK	Noninverting Differential Clock Input
6	EN	Noninverting Differential Output Enable Input. Setting EN = high and $\overline{EN}$ = low (differential high) enables the outputs. Setting EN = low and $\overline{EN}$ = high (differential low) drives outputs low.
7	$\overline{EN}$	Inverting Differential Output Enable Input
9	IN3	Noninverting Differential Input 3
10	$\overline{IN3}$	Inverting Differential Input 3
12	$\overline{OUT3}$	Inverting Differential Output 3
13	OUT3	Noninverting Differential Output 3
14, 20, 21, 27	V_{EE}	Negative Supply Voltage
15	IN2	Noninverting Differential Input 2
16	$\overline{IN2}$	Inverting Differential Input 2
18	$\overline{OUT2}$	Inverting Differential Output 2
19	OUT2	Noninverting Differential Output 2
22	OUT1	Noninverting Differential Output 1
23	$\overline{OUT1}$	Inverting Differential Output 1
25	$\overline{IN1}$	Inverting Differential Input 1
26	IN1	Noninverting Differential Input 1
28	OUT0	Noninverting Differential Output 0
29	$\overline{OUT0}$	Inverting Differential Output 0
31	$\overline{IN0}$	Inverting Differential Input 0
32	IN0	Noninverting Differential Input 0
—	EP	Exposed Paddle (MAX940_EGJ only). Connected to V_{EE} internally. See package dimensions.

Quad Differential LVECL/LVPECL Buffer/Receivers

Detailed Description

The MAX9400/MAX9402/MAX9403/MAX9405 are extremely fast, low-skew quad LVECL/ECL or LVPECL/PECL buffer/receivers designed for high-speed data and clock driver applications. The devices feature ultra-low propagation delay of 335ps and channel-to-channel skew of 16ps in asynchronous mode with 86mA supply current.

The four channels can be operated synchronously with an external clock, or in asynchronous mode, determined by the state of the SEL input. An enable input provides the ability to force all the outputs to a differential low state.

A variety of input and output terminations are offered for maximum design flexibility. The MAX9400 has open inputs and open emitter outputs. The MAX9402 has open inputs and 50Ω series outputs. The MAX9403 has 100Ω differential input impedance and open emitter outputs. The MAX9405 has 100Ω differential input impedance and 50Ω series outputs.

Supply Voltage

The MAX9400/MAX9402/MAX9403/MAX9405 are designed for operation with a single supply. Using a single negative supply of V_{EE} = -2.375V to -5.5V (V_{CC} = ground) yields LVECL/ECL-compatible input and output levels. Using a single positive supply of V_{CC} = +2.375V to +5.5V (V_{EE} = ground) yields LVPECL/PECL input and output levels.

Data Inputs

Figure 2 shows the functional diagram of the MAX9400/MAX9402/MAX9403/MAX9405. The MAX9400/MAX9402 have open inputs and require external termination. The MAX9403/MAX9405 have integrated 100Ω differential input termination resistors from IN_ to $\overline{IN\_}$ reducing external component count.

Outputs

The MAX9402/MAX9405 have internal 50Ω series output termination resistors and 8mA internal pulldown current sources. Using integrated resistors reduces external component count.

The MAX9400/MAX9403 have open emitter outputs. An external termination is required. See the *Output Termination* section.

Enable

Setting EN = high and $\overline{EN}$ = low enables the device. Setting EN = low and $\overline{EN}$ = high forces the outputs to a differential low, and all changes on CLK, SEL, and IN_ are ignored.

Asynchronous Operation

Setting SEL = high and $\overline{SEL}$ = low enables the four channels to operate independently as buffer/receivers. The CLK signal is ignored in this mode. In asynchronous mode, the CLK signal should be set to either logic low or high state to minimize noise coupling.

Synchronous Operation

Setting SEL = low and $\overline{SEL}$ = high enables all four channels to operate in synchronous mode. In this mode, buffered inputs are clocked into flip-flops simultaneously on the rising edge of the differential clock input (CLK and $\overline{CLK}$).

Differential Signal Input Limit

The maximum signal magnitude of the differential inputs is V_{CC} - V_{EE} or 3V, whichever is less.

Applications Information

Input Bias

Unused inputs should be biased or driven as shown in Figure 5. This avoids noise coupling that might cause toggling at the unused outputs.

Output Termination

Terminate open emitter outputs (MAX9400/MAX9403) through 50Ω to V_{CC} - 2V or use an equivalent Thevenin termination. Terminate both outputs and use identical termination on each for the lowest output-to-output skew. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if OUT_ is used as a single-ended output, terminate both OUT_ and $\overline{OUT\_}$.

Ensure that the output currents do not exceed the current limits as specified in the *Absolute Maximum Ratings* table. Under all operating conditions, the device's total thermal limits should be observed.

Power-Supply Bypassing

Adequate power-supply bypassing is necessary to maximize the performance and noise immunity. Bypass V_{CC} to V_{EE} with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors as close to the device as possible with the 0.01µF capacitor closest to the device pins. Use multiple bypass vias for connection to minimize inductance.

Circuit Board Traces

Input and output trace characteristics affect the performance of the MAX9400/MAX9402/MAX9403/MAX9405. Connect each of the inputs and outputs to a 50Ω characteristic impedance trace. Avoid discontinuities in differential impedance and maximize common-mode noise immunity by maintaining the distance between

differential traces and avoid sharp corners. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50Ω characteristic impedance through connectors and across cables. Minimize skew by matching the electrical length of the traces.

Chip Information

TRANSISTOR COUNT: 713

PROCESS: Bipolar

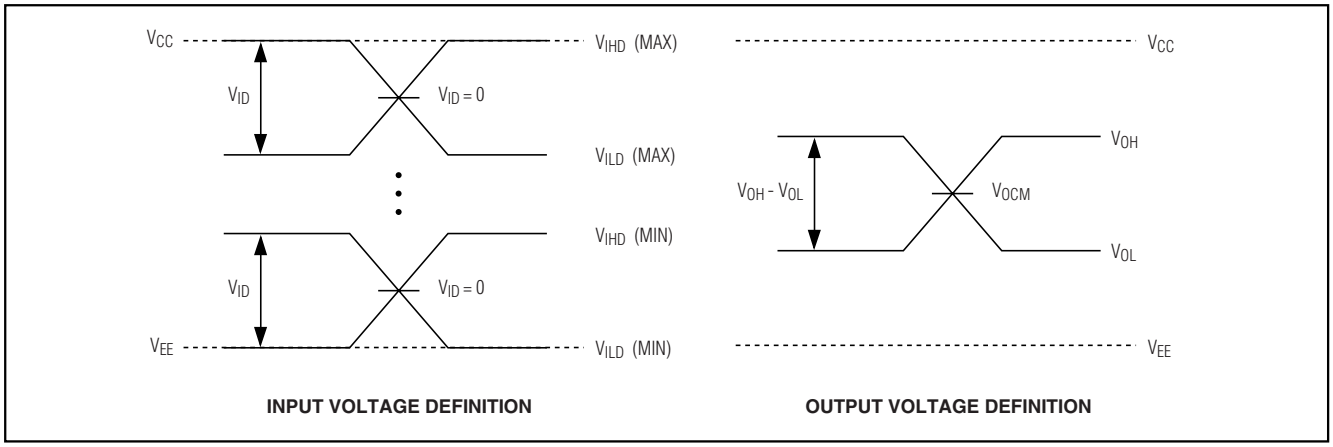


Figure 1. Input and Output Voltage Definitions

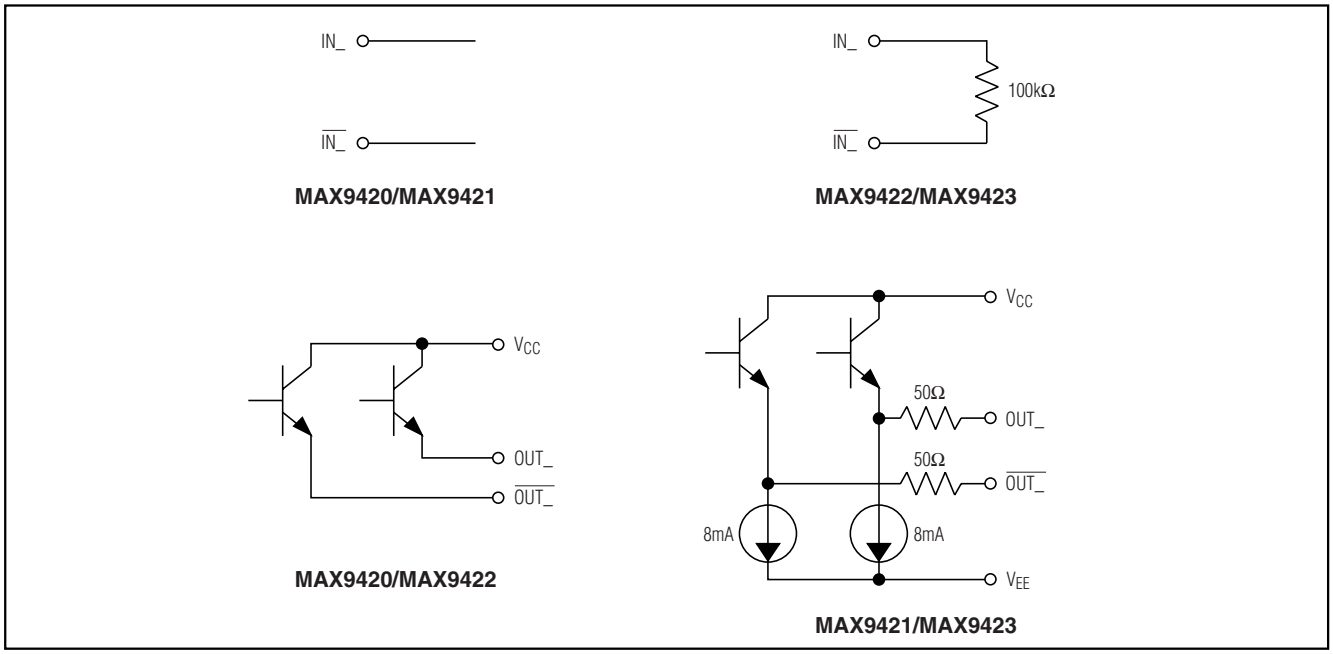


Figure 2. Input and Output Configurations

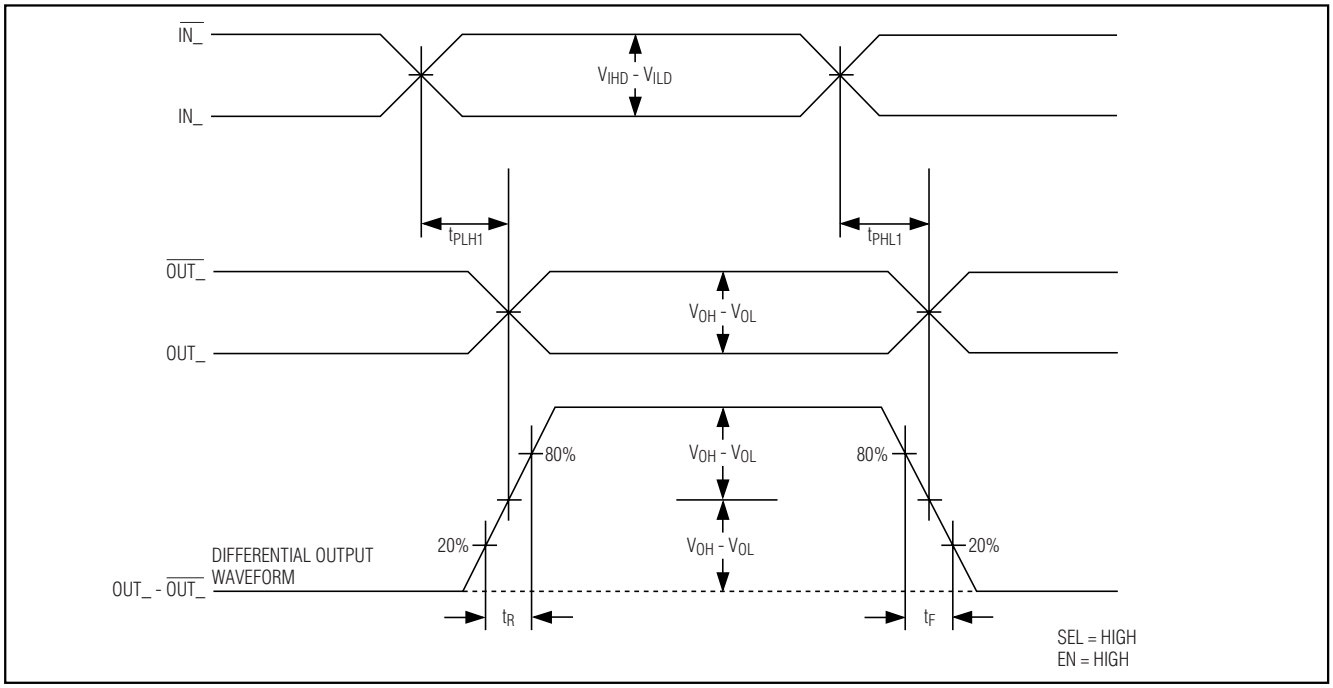


Figure 3. IN to OUT Propagation Delay and Transition Timing Diagram

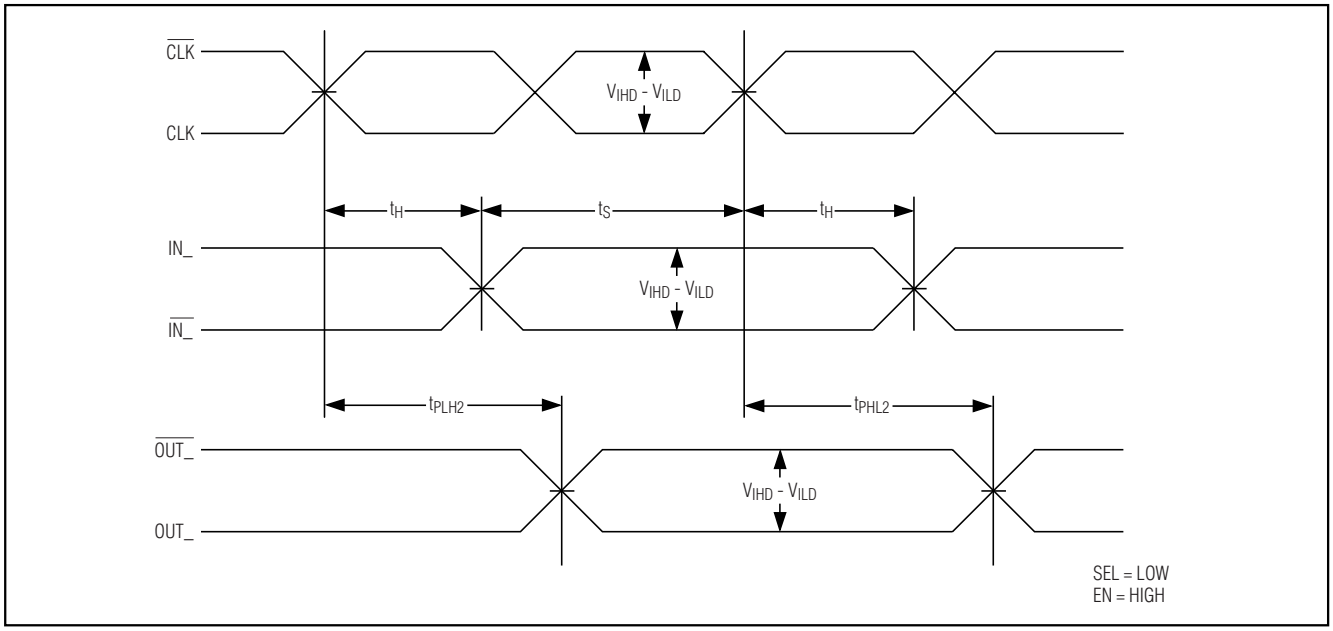


Figure 4. CLK to OUT Propagation Delay Timing Diagram

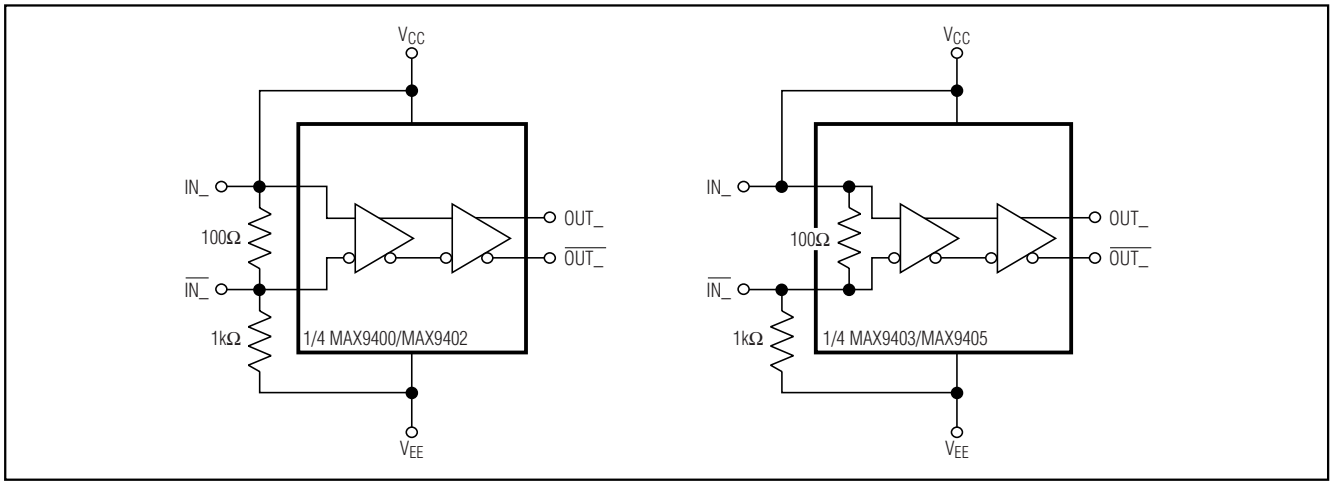
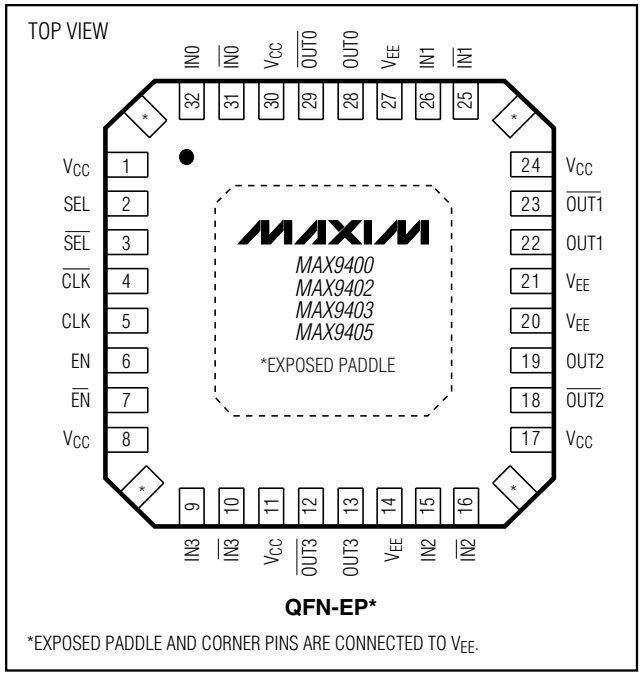


Figure 5. Input Bias Circuits for Unused Inputs

_____Pin Configurations (continued)

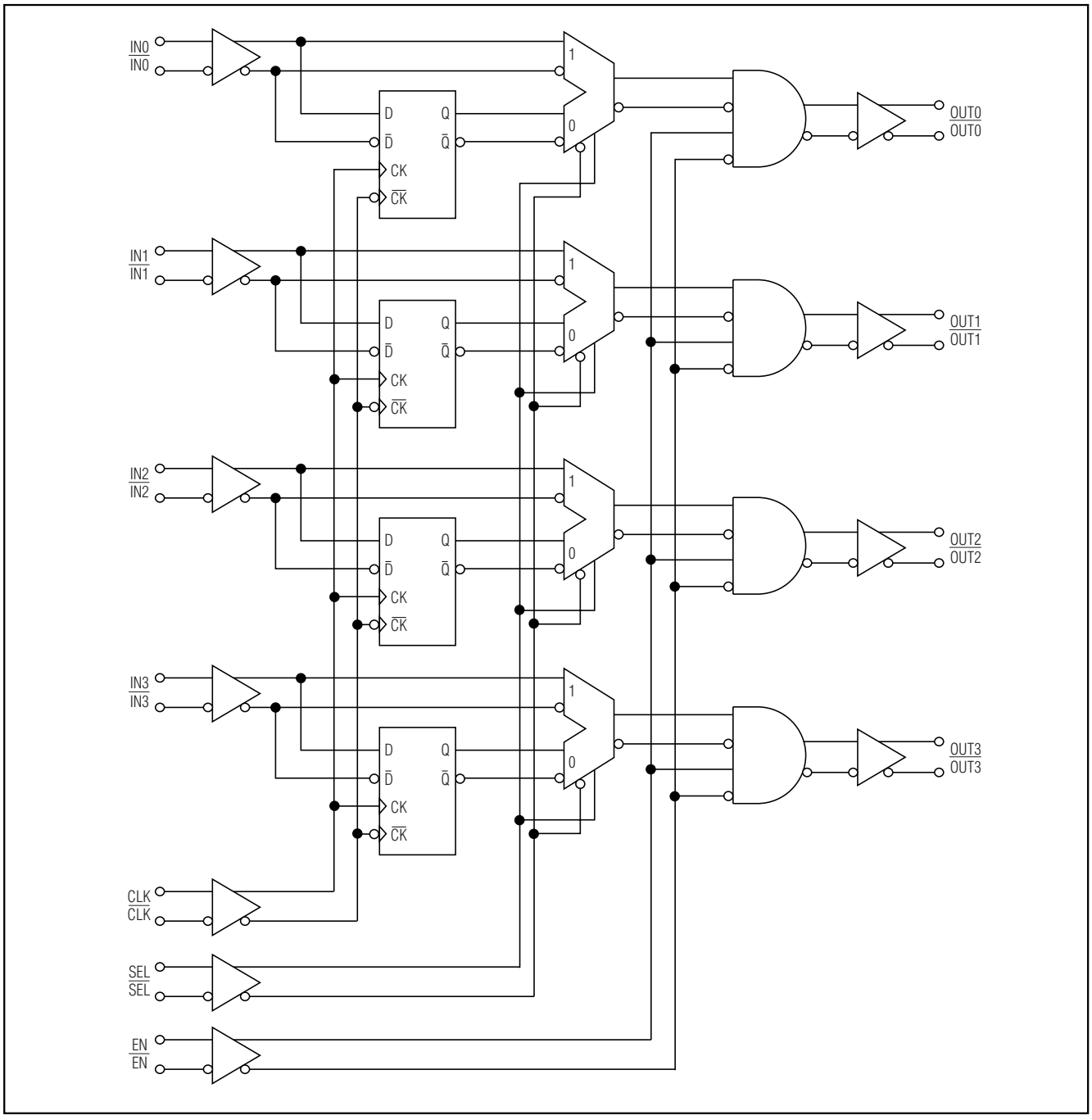


QFN-EP*

*EXPOSED PADDLE AND CORNER PINS ARE CONNECTED TO V_{EE}.

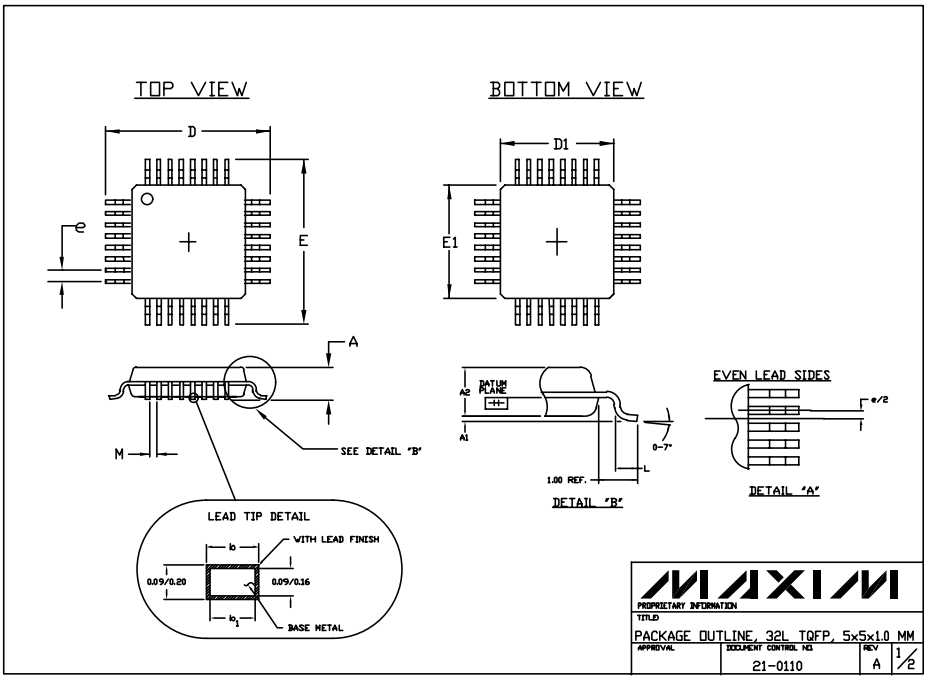
Quad Differential LVECL/LVPECL Buffer/Receivers

Functional Diagram



Package Information

32L TQFP, 5x5x01.0.EPS



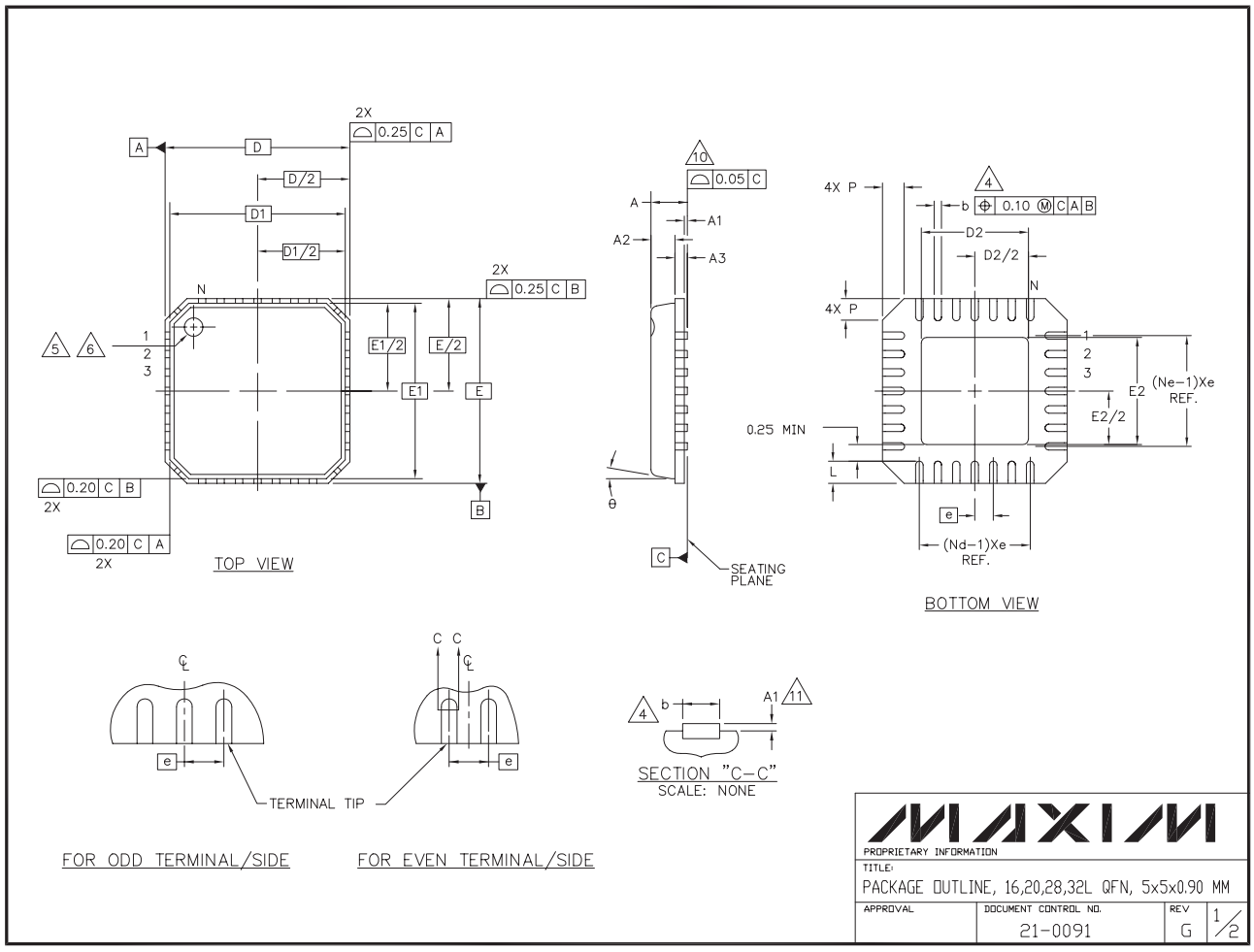
NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MO-136.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

	JEDEC VARIATIONS	
	DIMENSIONS IN MILLIMETERS	
	AA	
	5x5x1.0 MM	
	MIN.	MAX.
A	~~	1.20
A_1	0.05	0.15
A_2	0.95	1.05
D	7.00 BSC.	
D_1	5.00 BSC.	
E	7.00 BSC.	
E_1	5.00 BSC.	
L	0.45	0.75
M	0.15	~~
N	32	
e	0.50 BSC.	
b	0.17	0.27
b1	0.17	0.23

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, 32L TQFP, 5x5x1.0 MM
APPROVAL
DOCUMENT CONTROL NO.
21-0110
REV
A
2/2

Quad Differential LVECL/LVPECL Buffer/Receivers

Package Information (continued)



Package Information (continued)

NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/ LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES) AND TO SAW SINGULATION (STRAIGHT SIDES) QFN STYLES.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	1.00	
A3		0.20 REF.		
D		5.00 BSC		
D1		4.75 BSC		
E		5.00 BSC		
E1		4.75 BSC		
θ	0°	–	12°	
P	0		0.60	
D2	1.25	–	3.25	
E2	1.25	–	3.25	

SYMBOL	PITCH VARIATION B			NOTE
	MIN.	NOM.	MAX.	
e		0.80 BSC		
N		16		3
Nd		4		3
Ne		4		3
L	0.35	0.55	0.75	
b	0.28	0.33	0.40	4

SYMBOL	PITCH VARIATION B			NOTE
	MIN.	NOM.	MAX.	
e		0.65 BSC		
N		20		3
Nd		5		3
Ne		5		3
L	0.35	0.55	0.75	
b	0.23	0.28	0.35	4

SYMBOL	PITCH VARIATION C			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		28		3
Nd		7		3
Ne		7		3
L	0.35	0.55	0.75	
b	0.18	0.23	0.30	4

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		32		3
Nd		8		3
Ne		8		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0091	G	2/2