19-2538; Rev 0; 7/02

1:9 Differential LVPECL/LVECL/HSTL Clock and Data Driver

MAX9326

General Description

The MAX9326 low-skew, 1:9 differential driver features extremely low output-to-output skew (50ps max) and part-to-part skew (225ps max). These features make the device ideal for clock and data distribution across a backplane or board. The device repeats an HSTL or LVECL/LVPECL differential input at nine differential outputs. Outputs are compatible with LVECL and LVPECL, and can directly drive 50Ω terminated transmission lines.

The differential inputs can be configured to accept a single-ended signal when the unused complementary input is connected to the on-chip reference output voltage V_{BB}. All inputs have internal pulldown resistors to V_{EE}. The internal pulldowns and a fail-safe circuit ensure differential low default outputs when the inputs are left open or at V_{EE}.

The MAX9326 operates over a +2.375V to +3.8V supply range for interfacing to differential HSTL and LVPECL signals. This allows high-performance clock or data distribution in systems with a nominal +2.5V or +3.3V supply. For LVECL operation, the device operates with a -2.375V to -3.8V supply.

The MAX9326 is offered in 28-lead PLCC and space-saving 28-lead QFN packages. The MAX9326 is specified for operation from -40°C to +85°C.

Applications

Precision Clock Distribution

Low-Jitter Data Repeaters

Features

- ♦ **50ps (max) Output-to-Output Skew**
- ♦ **1.5ps$_{RMS}$ (max) Random Jitter**
- ♦ **Guaranteed 300mV Differential Output at 1.0GHz**
- ♦ **+2.375V to +3.8V Supplies for Differential HSTL/LVPECL**
- ♦ **-2.375V to -3.8V Supplies for Differential LVECL**
- ♦ **On-Chip Reference for Single-Ended Inputs**
- ♦ **Outputs Low for Inputs Open or at V_{EE}**
- ♦ **Pin Compatible with MC100LVE111**

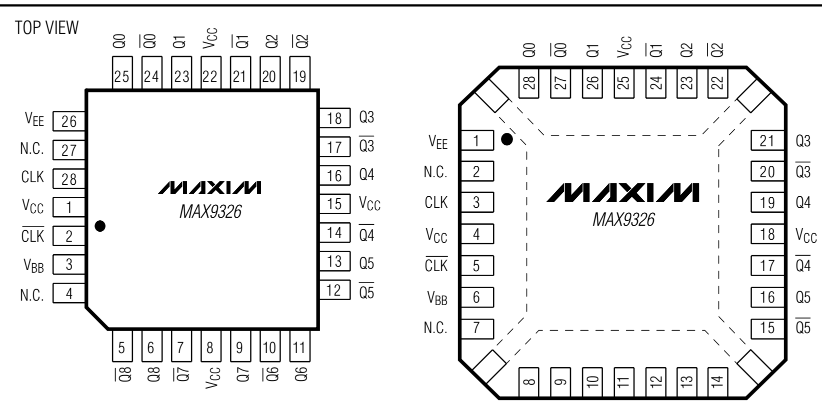
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9326EQI	-40°C to +85°C	28 PLCC
MAX9326ETI*	-40°C to +85°C	28 QFN 5mm x 5mm

*Future product—contact factory for availability.

Functional Diagram appears at end of data sheet.

Pin Configurations



PLCC

QFN*

*CORNER PINS AND EXPOSED PAD ARE CONNECTED TO V_{EE}.

1:9 Differential LVPECL/LVECL/HSTL Clock and Data Driver

ABSOLUTE MAXIMUM RATINGS

V_{CC} - V_{EE} ....-0.3V to +4.1V
Inputs (CLK, $\overline{CLK}$) to V_{EE} ....-0.3V to (V_{CC} + 0.3V)
CLK to $\overline{CLK}$ ....±3.0V
Continuous Output Current 50mA
Surge Output Current 100mA
V_{BB} Sink/Source Current ....±0.65mA
Continuous Power Dissipation (T_A = +70°C)
28-Lead PLCC (derate 10.5mW/°C above +70°C) 842mW
θ_{JA} in Still Air ....+95°C/W
θ_{JC} ....+25°C/W
28-Lead QFN (derate 20.8mW/°C above +70°C) 1667mW
θ_{JA} in Still Air ....+48°C/W
θ_{JC} ....+2°C/W
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
ESD Protection
Human Body Model (CLK, $\overline{CLK}$, Q_, $\overline{Q\_}$) ....≥2kV
Soldering Temperature (10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

((V_{CC} - V_{EE}) = 2.375V to 3.8V, R_L = 50Ω ±1% to V_{CC} - 2V. Typical values are at (V_{CC} - V_{EE}) = 3.3V, V_{IH} = (V_{CC} - 1V), V_{IL} = (V_{CC} - 1.5V.) (Notes 1–4)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DIFFERENTIAL INPUT (CLK_, $\overline{CLK\_}$)												
Single-Ended Input High Voltage	V_{IH}	Figure 1	V_{CC} - 1.165		V_{CC}	V_{CC} - 1.165		V_{CC}	V_{CC} - 1.165		V_{CC}	V
Single-Ended Input Low Voltage	V_{IL}	Figure 1	V_{EE}		V_{CC} - 1.475	V_{EE}		V_{CC} - 1.475	V_{EE}		V_{CC} - 1.475	V
Differential Input High Voltage	V_{IHD}	Figure 1	V_{EE} + 1.2		V_{CC}	V_{EE} + 1.2		V_{CC}	V_{EE} + 1.2		V_{CC}	V
Differential Input Low Voltage	V_{ILD}	Figure 1	V_{EE}		V_{CC} - 0.095	V_{EE}		V_{CC} - 0.095	V_{EE}		V_{CC} - 0.095	V
Differential Input Voltage	V_{IHD} - V_{ILD}	(V_{CC} - V_{EE}) < 3.0V, Figure 1	0.095		V_{CC} - V_{EE}	0.095		V_{CC} - V_{EE}	0.095		V_{CC} - V_{EE}	V
		(V_{CC} - V_{EE}) ≥ 3.0V, Figure 1	0.095		3.0	0.095		3.0	0.095		3.0	
Input Current	I_{IN}	V_{IH}, V_{IL}, V_{IHD}, V_{ILD}	-10.0		+150.0	-10.0		+150.0	-10.0		+150.0	µA

DC ELECTRICAL CHARACTERISTICS (continued)

((V_{CC} - V_{EE}) = 2.375V to 3.8V, R_L = 50Ω ±1% to V_{CC} - 2V. Typical values are at (V_{CC} - V_{EE}) = 3.3V, V_{IH} = (V_{CC} - 1V), V_{IL} = (V_{CC} - 1.5V.) (Notes 1–4)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT (Q_, $\overline{Q\_}$)												
Single-Ended Output High Voltage	V_{OH}	Figure 2	V_{CC} - 1.085	V_{CC} - 0.977	V_{CC} - 0.880	V_{CC} - 1.025	V_{CC} - 0.949	V_{CC} - 0.88	V_{CC} - 1.025	V_{CC} - 0.929	V_{CC} - 0.88	V
Single-Ended Output Low Voltage	V_{OL}	Figure 2	V_{CC} - 1.810	V_{CC} - 1.695	V_{CC} - 1.620	V_{CC} - 1.810	V_{CC} - 1.697	V_{CC} - 1.62	V_{CC} - 1.810	V_{CC} - 1.698	V_{CC} - 1.62	V
Differential Output Voltage	V_{OH} - V_{OL}	Figure 2	535	718		595	749		595	769		mV
REFERENCE VOLTAGE OUTPUT (V_{BB})												
Reference Voltage Output	V_{BB}	I_{BB} = ±0.5mA (Note 5)	V_{CC} - 1.38	V_{CC} - 1.318	V_{CC} - 1.26	V_{CC} - 1.38	V_{CC} - 1.325	V_{CC} - 1.26	V_{CC} - 1.38	V_{CC} - 1.328	V_{CC} - 1.26	V
SUPPLY												
Supply Current	I_{EE}	(Note 6)		35	50		39	55		42	65	mA

AC ELECTRICAL CHARACTERISTICS

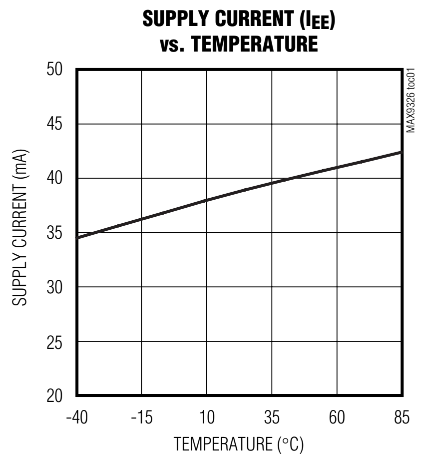
((V_{CC} - V_{EE}) = 2.375V to 3.8V, R_L = 50Ω ±1% to V_{CC} - 2V, f_{IN} ≤ 500MHz, input transition time = 125ps (20% to 80%). Typical values are at (V_{CC} - V_{EE}) = 3.3V, V_{IH} = (V_{CC} - 1V), V_{IL} = (V_{CC} - 1.5V.) (Note 7)

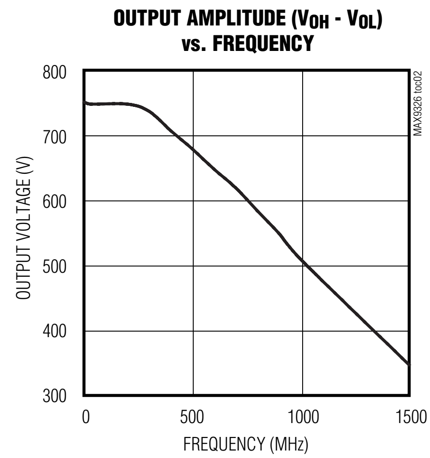
PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Differential Input-to-Output Delay	t_{PLHD} t_{PHLD}	Figure 2	365		615	375		605	383		653	ps
Single-Ended Input-to-Output Delay	t_{PLH} t_{PHL}	Figure 3 (Note 8)	350		635	360		685	360		705	ps
Output-to-Output Skew	t_{SKOO}	(Note 9)			50			50			50	ps
Part-to-Part Skew	t_{SKPP}	Differential input (Note 10)			190			125			240	ps
Added Random Jitter	t_{RJ}	f_{IN} = 0.5GHz clock pattern (Note 11)			1.5			1.5			1.5	ps_{RMS}
Added Deterministic Jitter	t_{DJ}	f_{IN} = 1.0Gbps, $2E^{23}$ - 1 PRBS pattern (Note 11)			95			95			95	ps_{P-P}
Switching Frequency	f_{MAX}	V_{OH} - V_{OL} ≥ 300mV clock pattern	1.5			1.5			1.5			GHz
Output Rise/Fall Time (20% to 80%)	t_R, t_F	Figure 2	140		440	140		440	140		440	ps

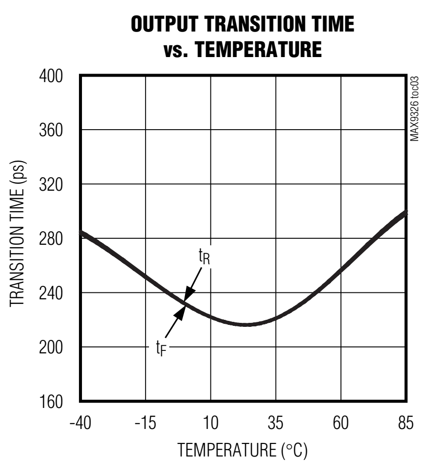
Note 1: Measurements are made with the device in thermal equilibrium.
Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.
Note 3: DC parameters production tested at T_A = +25°C and guaranteed by design over the full operating temperature range.
Note 4: Single-ended input operation using V_{BB} is limited to (V_{CC} - V_{EE}) = 3.0V to 3.8V.
Note 5: Use V_{BB} only for inputs that are on the same device as the V_{BB} reference.
Note 6: All pins open except V_{CC} and V_{EE}.
Note 7: Guaranteed by design and characterization. Limits are set at ±6 sigma.
Note 8: Measured from the 50% point of the input signal with the 50% point equal to V_{BB}, to the 50% point of the output signal.
Note 9: Measured between outputs of the same part at the signal crossing points for a same-edge transition. Differential input signal.
Note 10: Measured between outputs of different parts under identical conditions for same-edge transition.
Note 11: Device jitter added to the input signal. Differential input signal.

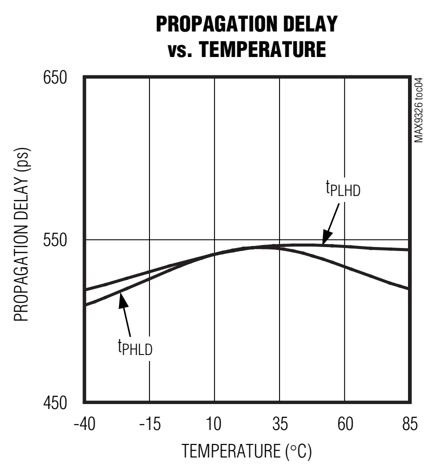
Typical Operating Characteristics

(Typical values are at (V_{CC} - V_{EE}) = 3.3V, V_{IH} = (V_{CC} - 1V), V_{IL} = (V_{CC} - 1.5V), R_L = 50Ω ±1% to V_{CC} - 2V, f_{IN} = 500MHz, input transition time = 125ps (20% to 80%).)









1:9 Differential LVPECL/LVECL/HSTL Clock and Data Driver

Pin Description

PIN		NAME	FUNCTION
PLCC	QFN		
1, 8, 15, 22	4, 11, 18, 25	V_{CC}	Positive Supply Voltage. Bypass each V_{CC} to V_{EE} with 0.1µF and 0.01µF ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.
2	5	$\overline{CLK}$	Inverting Differential Clock Input. Internal 105kΩ pulldown to V_{EE}.
3	6	V_{BB}	Reference Output Voltage. Connect to the inverting or noninverting clock input to provide a reference for single-ended operation. When used, bypass V_{BB} to V_{CC} with a 0.01µF ceramic capacitor. Otherwise leave open.
4, 27	2, 7	N.C.	Not Connected
5	8	$\overline{Q8}$	Inverting Q8 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
6	9	Q8	Noninverting Q8 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
7	10	$\overline{Q7}$	Inverting Q7 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
9	12	Q7	Noninverting Q7 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
10	13	$\overline{Q6}$	Inverting Q6 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
11	14	Q6	Noninverting Q6 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
12	15	$\overline{Q5}$	Inverting Q5 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
13	16	Q5	Noninverting Q5 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
14	17	$\overline{Q4}$	Inverting Q4 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
16	19	Q4	Noninverting Q4 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
17	20	$\overline{Q3}$	Inverting Q3 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
18	21	Q3	Noninverting Q3 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
19	22	$\overline{Q2}$	Inverting Q2 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
20	23	Q2	Noninverting Q2 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
21	24	$\overline{Q1}$	Inverting Q1 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
23	26	Q1	Noninverting Q1 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
24	27	$\overline{Q0}$	Inverting Q0 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
25	28	Q0	Noninverting Q0 Output. Typically terminate with 50Ω resistor to V_{CC} - 2V.
26	1	V_{EE}	Negative Supply Voltage
28	3	CLK	Noninverting Differential Clock Input. Internal 105kΩ pulldown to V_{EE}.
—	Exposed Pad	—	Internally Connected to V_{EE}

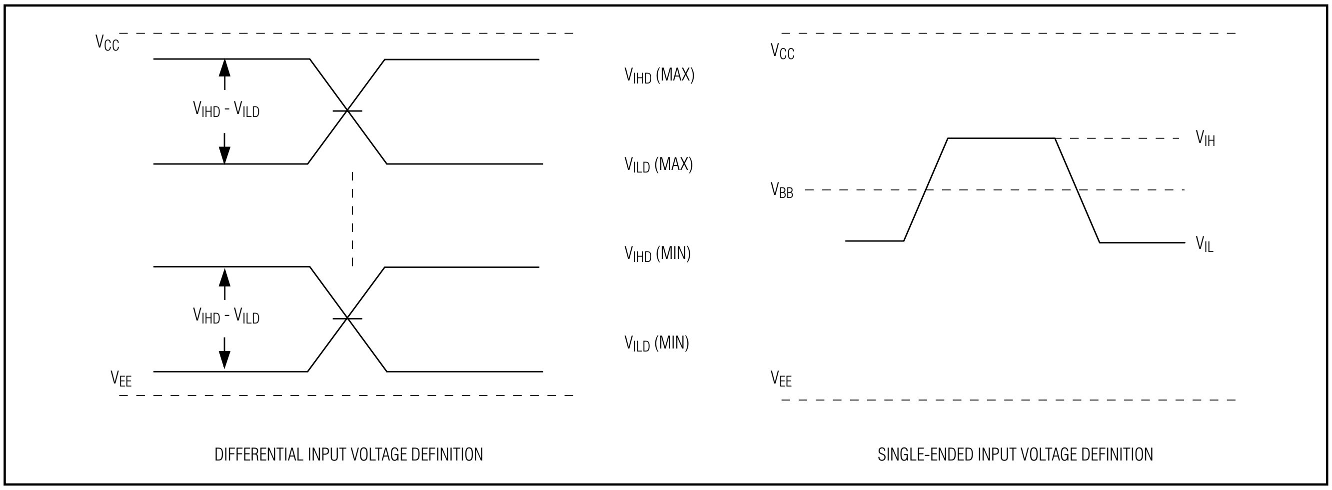


Figure 1. Input Voltage Definitions

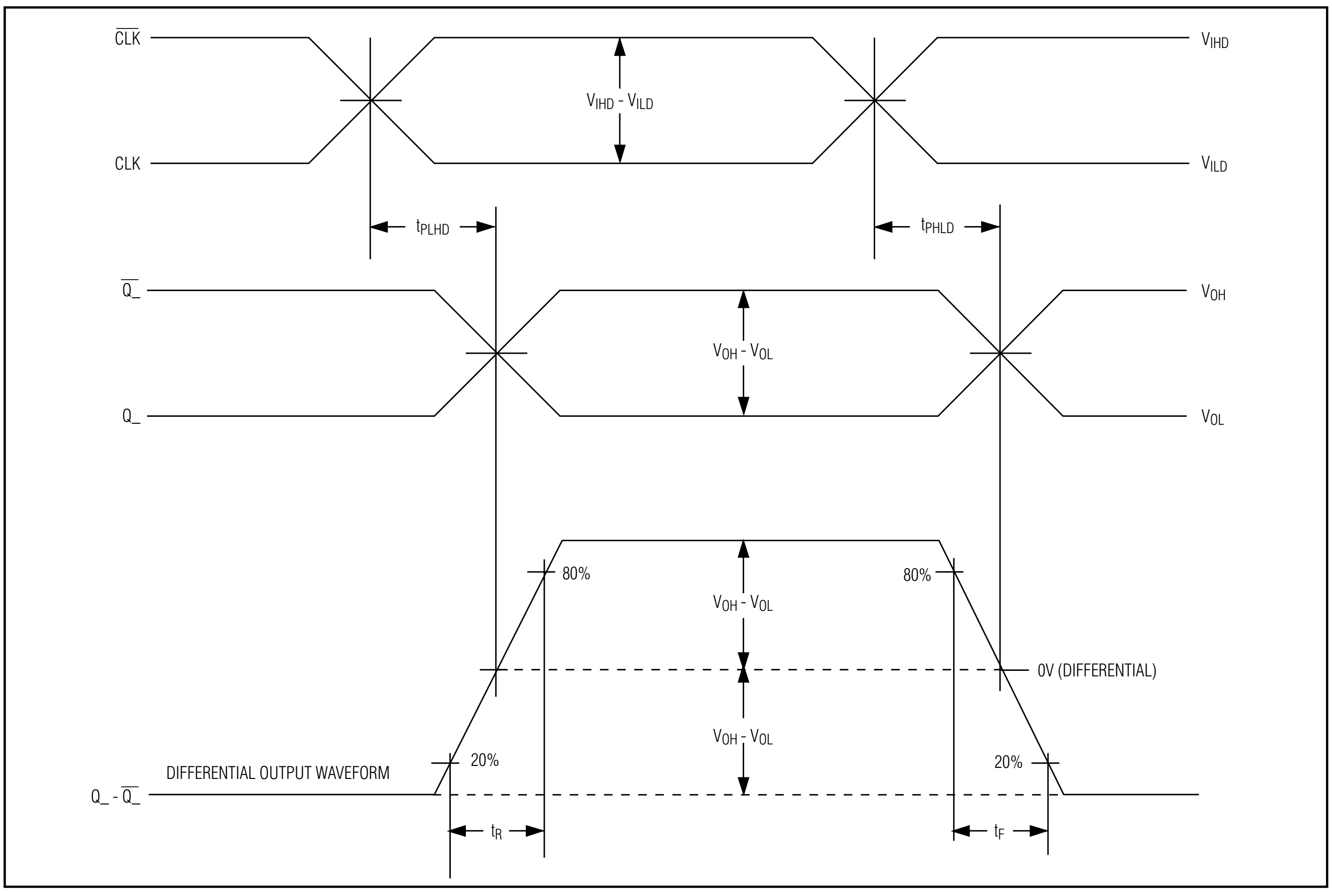


Figure 2. Differential Input (CLK, $\overline{CLK}$) to Output (Q_, $\overline{Q\_}$) Delay Timing Diagram

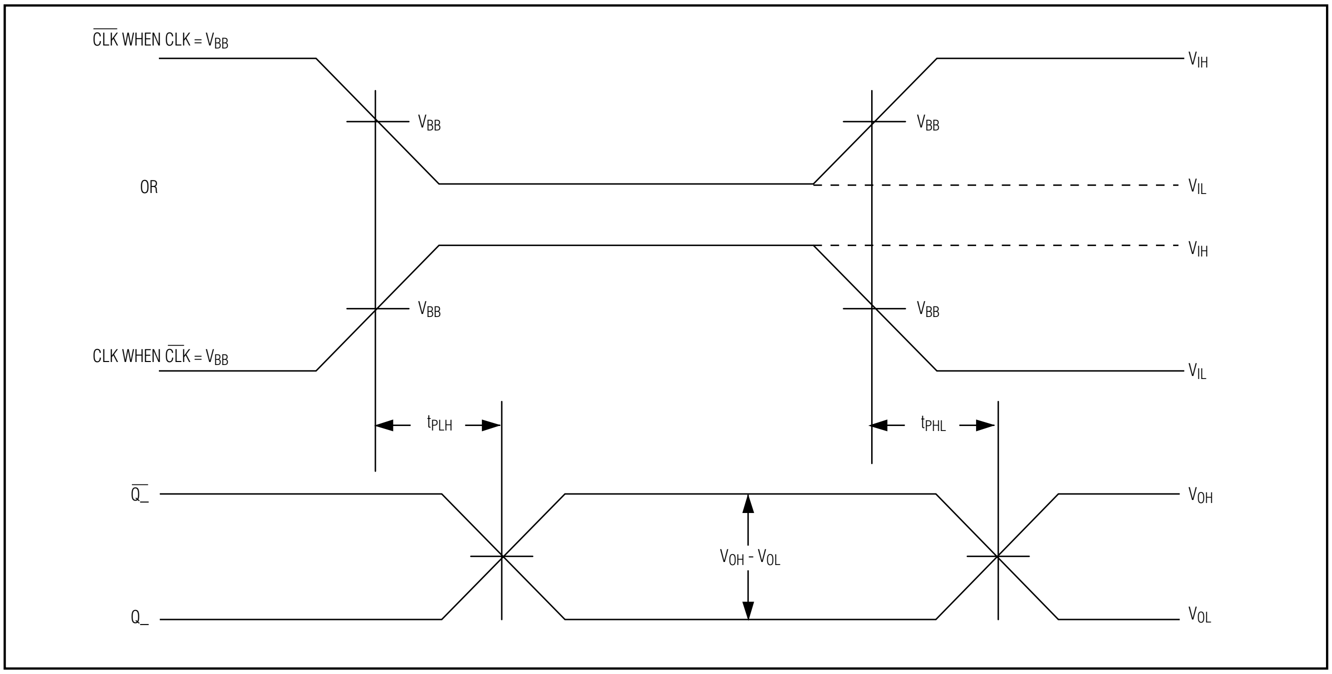


Figure 3. Single-Ended Input (CLK, $\overline{CLK}$) to Output (Q_, $\overline{Q\_}$) Delay Timing Diagram

Detailed Description

The MAX9326 low-skew, 1:9 differential driver features extremely low output-to-output skew (50ps max) and part-to-part skew (225ps max). These features make the device ideal for clock and data distribution across a backplane or board. The device repeats an HSTL or LVECL/LVPECL differential input at nine differential outputs. Outputs are compatible with LVECL and LVPECL, and can directly drive 50Ω terminated transmission lines.

The differential inputs (CLK, $\overline{CLK}$) can be configured to accept a single-ended signal when the unused complementary input is connected to the on-chip reference output voltage (V_{BB}). A single-ended input of at least V_{BB} ±95mV or a differential input of at least 95mV switches the outputs to the V_{OH} and V_{OL} levels specified in the *DC Electrical Characteristics.* The maximum magnitude of the differential input from CLK to $\overline{CLK}$ is ±3.0V or ±(V_{CC} - V_{EE}), whichever is less. This limit also applies to the difference between a single-ended input and any reference voltage input.

All the differential inputs have 105kΩ pulldowns to V_{EE}. Internal pulldowns and a fail-safe circuit ensure differential low default outputs when the inputs are left open or at V_{EE}.

Specifications for the high and low voltages of a differential input (V_{IHD} and V_{ILD}) and the differential input voltage (V_{IHD} - V_{ILD}) apply simultaneously.

For interfacing to differential HSTL and LVPECL signals, these devices operate over a 2.375V to 3.8V supply range, allowing high-performance clock or data distribution in systems with a nominal 2.5V or 3.3V supply. For differential LVECL operation, these devices operate from a -2.375V to -3.8V supply.

Single-Ended Operation

The differential inputs (CLK, $\overline{CLK}$) can be configured to accept single-ended inputs when operating at supply voltages greater than 2.58V. The recommended supply voltage for single-ended operation is 3.0V to 3.8V. A differential input is configured for single-ended operation by connecting the on-chip reference voltage, V_{BB}, to an unused complementary input as a reference. For example, the differential CLK, $\overline{CLK}$ input is converted to a noninverting, single-ended input by connecting V_{BB} to $\overline{CLK}$ and connecting the single-ended input to CLK. Similarly, an inverting input is obtained by connecting V_{BB} to CLK and connecting the single-ended input to $\overline{CLK}$. With a differential input configured as single ended (using V_{BB}), the single-ended input can be driven to V_{CC} or V_{EE} or with a single-ended LVPECL/LVECL signal.

When configuring a differential input as a single-ended input, a user must ensure that the supply voltage (V_{CC} - V_{EE}) is greater than 2.58V. This is because the input high minimum level must be at (V_{EE} + 1.2V) or higher for proper operation. The reference voltage V_{BB} must be at least (V_{EE} + 1.2V) or higher for the same reason because it becomes the high-level input when the other single-ended input swings below it. The minimum V_{BB} output for the MAX9326 is (V_{CC} - 1.38V). Substituting the minimum V_{BB} output for (V_{BB} = V_{EE} + 1.2V) results in a minimum supply (V_{CC} - V_{EE}) of 2.58V. Rounding up to standard supplies gives the single-ended operating supply ranges (V_{CC} - V_{EE}) of 3.0V to 3.8V for the MAX9326.

When using the V_{BB} reference output, bypass it with a 0.01µF ceramic capacitor to V_{CC}. If not used, leave it open. The V_{BB} reference can source or sink 0.5mA, which is sufficient to drive two inputs.

Applications Information

Output Termination

Terminate the outputs through 50Ω to V_{CC} - 2V or use equivalent Thevenin terminations. Terminate each Q and Q output with identical termination on each for the lowest output distortion. When a single-ended signal is taken from the differential output, terminate both Q_ and $\overline{Q}$_.

Ensure that output currents do not exceed the current limits as specified in the *Absolute Maximum Ratings*. Under all operating conditions, the device's total thermal limits should be observed.

Supply Bypassing

Bypass each V_{CC} to V_{EE} with high-frequency surface-mount ceramic 0.1µF and 0.01µF capacitors. Place the capacitors as close to the device as possible with the 0.01µF capacitor closest to the device pins.

Use multiple vias when connecting the bypass capacitors to ground. When using the V_{BB} reference output, bypass it with a 0.01µF ceramic capacitor to V_{CC}. If the V_{BB} reference is not used, it can be left open.

Traces

Circuit board trace layout is very important to maintain the signal integrity of high-speed differential signals. Maintaining integrity is accomplished in part by reducing signal reflections and skew, and increasing common-mode noise immunity.

Signal reflections are caused by discontinuities in the 50Ω characteristic impedance of the traces. Avoid discontinuities by maintaining the distance between differential traces, not using sharp corners or using vias. Maintaining distance between the traces also increases common-mode noise immunity. Reducing signal skew is accomplished by matching the electrical length of the differential traces.

Exposed-Pad Package

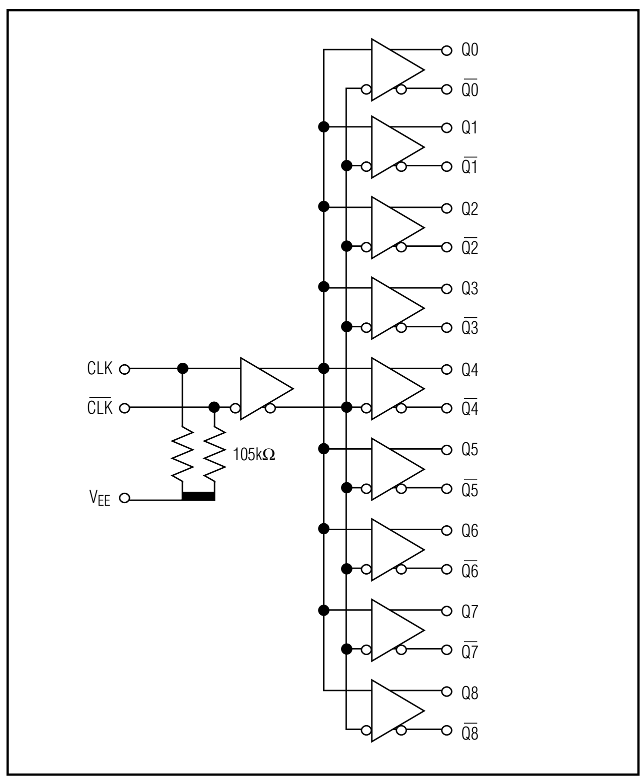
The 28-lead QFN package (MAX9326EGI) has the exposed paddle on the bottom of the package that provides the primary heat removal path from the IC to the PC board, as well as excellent electrical grounding to the PC board. **The MAX9326EGI's exposed pad is internally connected to V_{EE}. Do not connect the exposed pad to a separate circuit ground plane unless V_{EE} and the circuit ground are the same.**

Chip Information

TRANSISTOR COUNT: 1030

PROCESS: Bipolar

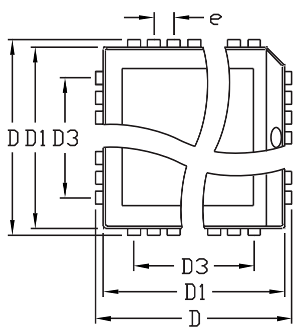
Functional Diagram



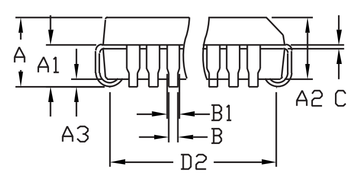
1:9 Differential LVPECL/LVECL/HSTL Clock and Data Driver

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.145	0.156	3.68	3.96
A3	0.020	---	0.51	---
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
e	0.050		1.27	



	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MO047
D	0.385	0.395	9.78	10.03	20	AA
D1	0.350	0.356	8.89	9.04		
D2	0.290	0.330	7.37	8.38		
D3	0.200 REF		5.08 REF			
D	0.485	0.495	12.32	12.57	28	AB
D1	0.450	0.456	11.43	11.58		
D2	0.390	0.430	9.91	10.92		
D3	0.300 REF		7.62 REF			
D	0.685	0.695	17.40	17.65	44	AC
D1	0.650	0.656	16.51	16.66		
D2	0.590	0.630	14.99	16.00		
D3	0.500 REF		12.70 REF			
D	0.985	0.995	25.02	25.27	68	AE
D1	0.950	0.958	24.13	24.33		
D2	0.890	0.930	22.61	23.62		
D3	0.800 REF		20.32 REF			

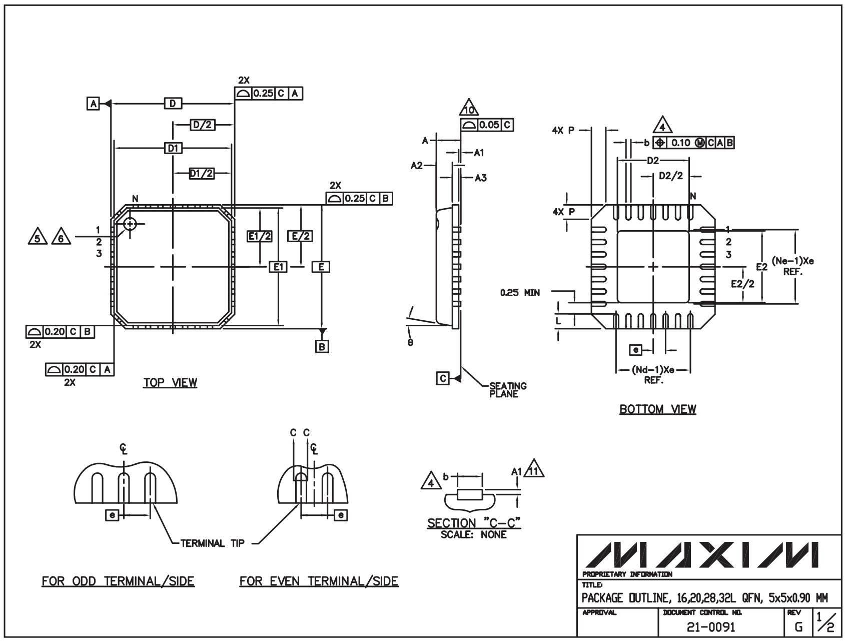
NOTES:
1. D1 DOES NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .20mm (.008") PER SIDE
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MO047-XX AS SHOWN IN TABLE
6. N = NUMBER OF PINS

MAXIM — PROPRIETARY INFORMATION | TITLE: PACKAGE FAMILY OUTLINE: PLCC | 1/1 | DOCUMENT CONTROL NUMBER: 21-0049 | REV: C

PLCC.EPS

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



NOTES:

1. DIE THICKNESS ALLOWABLE IS 0.305mm MAXIMUM (.012 INCHES MAXIMUM)
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR INK/ LASER MARKED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.05mm.
9. APPLIED FOR EXPOSED PAD AND TERMINALS.
   EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
10. MEETS JEDEC MO220.
11. THIS PACKAGE OUTLINE APPLIES TO ANVIL SINGULATION (STEPPED SIDES) AND TO SAW SINGULATION (STRAIGHT SIDES) QFN STYLES.

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.90	1.00	
A1	0.00	0.01	0.05	
A2	0.00	0.65	1.00	
A3	0.20 REF.			
D	5.00 BSC			
D1	4.75 BSC			
E	5.00 BSC			
E1	4.75 BSC			
θ	0°	–	12°	
P	0		0.60	
D2	1.25	–	3.25	
E2	1.25	–	3.25	

SYMBOL	PITCH VARIATION B			NOTE	SYMBOL	PITCH VARIATION B			NOTE	SYMBOL	PITCH VARIATION C			NOTE	SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.			MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
e	0.80 BSC				e	0.65 BSC				e	0.50 BSC				e	0.50 BSC			
N	16			3	N	20			3	N	28			3	N	32			3
Nd	4			3	Nd	5			3	Nd	7			3	Nd	8			3
Ne	4			3	Ne	5			3	Ne	7			3	Ne	8			3
L	0.35	0.55	0.75		L	0.35	0.55	0.75		L	0.35	0.55	0.75		L	0.30	0.40	0.50	
b	0.28	0.33	0.40	4	b	0.23	0.28	0.35	4	b	0.18	0.23	0.30	4	b	0.18	0.23	0.30	4

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 16,20,28,32L QFN, 5x5x0.90 MM
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