RELIABILITY REPORT

FOR

MAX917Exx

PLASTIC ENCAPSULATED DEVICES

May 8, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by:

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by:

Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX917 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX917-MAX920 nanopower comparators in space-saving SOT23 packages feature Beyond-the-Rails™ inputs and are guaranteed to operate down to +1.8V. The MAX917/MAX918 feature an on-board 1.245V ±1.5% reference and draw an ultra-low supply current of only 750nA, while the MAX919/MAX920 (without reference) require just 380nA of supply current. These features make the MAX917-MAX920 family of comparators ideal for all 2-cell battery applications, including monitoring/management.

The unique design of the output stage limits supply-current surges while switching, virtually eliminating the supply glitches typical of many other comparators. This design also minimizes overall power consumption under dynamic conditions. The MAX917/MAX919 have a push/pull output stage that sinks and sources current. Large internal output drivers allow Rail-to-Rail® output swing with loads up to 8mA. The MAX918/MAX920 have an open-drain output stage that makes them suitable for mixed-voltage system design.

B. Absolute Maximum Ratings

Item	Rating
Terminal Voltages Referenced to VEE	
V_{CC}	+6V
Voltage Inputs (IN+, IN-,REF)	(VEE -0.3V) to (V_{CC} + 0.3V)
Output Voltage	(VEE - 0.3v) to (VCC + 0.3V)
Output Current	+/-50mA
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	571mW
Derates above +70°C	7.31mW/°C

II. Manufacturing Information

A. Description/Function: Nanopower Comparator

B. Process: S12

C. Number of Device Transistors: 505

D. Fabrication Location: San Jose

E. Assembly Location: Malaysia , Thailand

F. Date of Initial Production: July 20, 1999

III. Packaging Information

A. Package Type:	5 Lead SOT23	8 Lead SO
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-Filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1501-0158	Buildsheet # 05-1501-0157
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions: 56 x 38 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Al/Si/Cu (Aluminum/ Silicon/ Copper)

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns

F. Minimum Metal Spacing: 1.2 microns

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 79 \times 2}$$

(Chi square value for MTTF upper limit)

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 13.74 \times 10^{-9}$ $\lambda = 13.74$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The CM44 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1

Reliability Evaluation Test Results

MAX917Exx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	79	0
Moisture Testing				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality (generic test vehicle)	755	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality (generic test vehicle)	77	0
Mechanical Stress				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters (generic test vehicle)	77	0

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

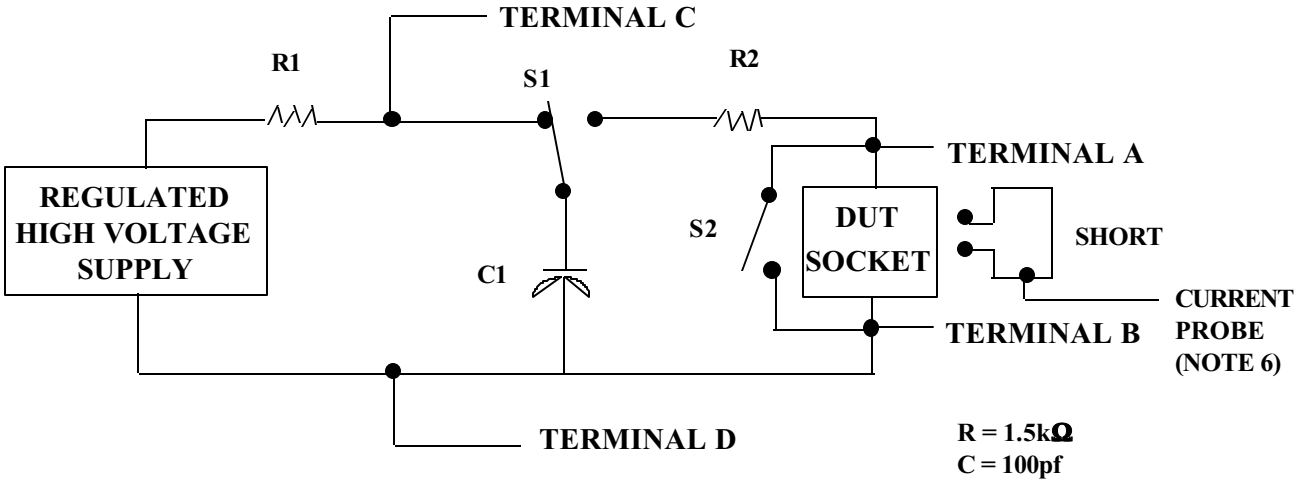
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

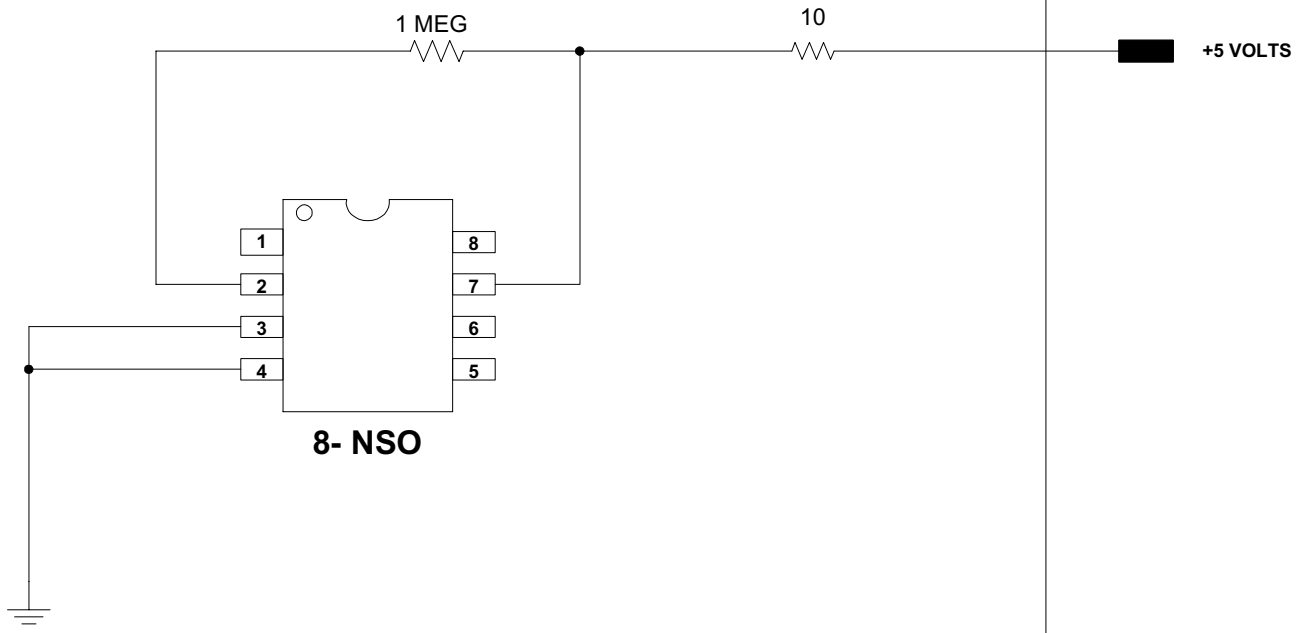
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



ONCE PER SOCKET

ONCE PER BOARD



8- NSO

DEVICES: MAX 917/918/919/920/9117/9118/9119/9120.
MAX. EXPECTED CURRENT = 5 uA

DRAWN BY: TODD BEJSOVEC

NOTES: