RELIABILITY REPORT

FOR

MAX824SExK

PLASTIC ENCAPSULATED DEVICES

July 16, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX824S successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX824S microprocessor (µP) supervisory circuit combines reset output and watchdog input functions in a 5-pin SOT23-5 or SC70 package. This device significantly improves system reliability and accuracy compared to separate ICs or discrete components. The MAX824S is specifically designed to ignore fast transients on V_{CC}.

The MAX824S has a preprogrammed reset threshold voltages of 4.38V. This device has an active-low reset output, which is guaranteed to be in the correct state for V_{CC} down to 1V. The MAX824S also has an active-high reset output.

B. Absolute Maximum Ratings

Item	Rating
V_{CC}	-0.3V to +6.0V
All Other Pins	-0.3V to (V_{CC} + 0.3V)
Input Current, All Pins Except RESET and /RESET	20mA
Output Current, RESET, /RESET	20mA
Rate of Rise, V_{CC}	100V/µs
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
5 Lead SC70	247mW
5 Lead SOT23	571mW
Derates above +70°C	
5 Lead SC70	3.1mW/°C
5 Lead SOT23	7.1mW/°C

II. Manufacturing Information

A. Description/Function: 5-Pin Microprocessor Supervisory Circuit

B. Process: S12 (Standard 1.2 micron silicon gate CMOS)

C. Number of Device Transistors: 607

D. Fabrication Location: Oregon, USA and San Jose, CA

E. Assembly Location: Malaysia and Thailand

F. Date of Initial Production: June, 1996

III. Packaging Information

A. Package Type:	**5 Lead SC70**	**5 Lead SOT23**
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Alloy 42	Solder Plate
D. Die Attach:	Non-Conductive	Silver-Filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1601-0011	Buildsheet #05-1601-0010
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions: 42 x 36 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum/Si (Si = 1%)

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns (as drawn)

F. Minimum Metal Spacing: 1.2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 100 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 160 \times 2}$$

1.83 (Chi square value for MTTF upper limit)

192 x 4389 x 160 x 2 — Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 6.78 \times 10^{-9}$

$\lambda = 6.78$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5033) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The MS05-8 die type has been found to have all pins able to withstand a transient pulse of ± 2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1

Reliability Evaluation Test Results

MAX824SExK

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION		SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		160	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	SC70	120	0
			SOT23	360	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the package.
Note 2: Generic process/package data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

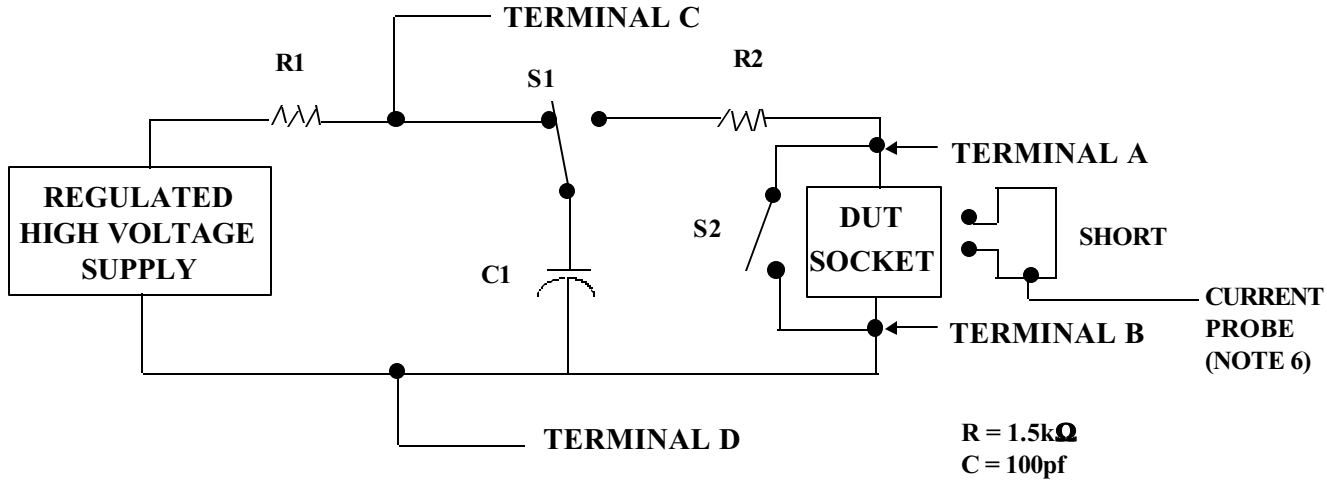
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

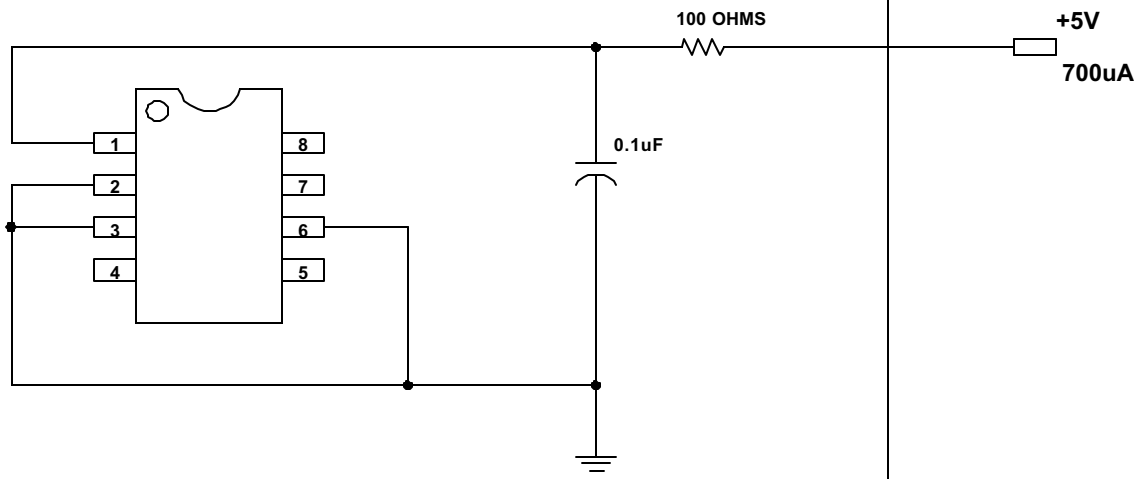
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and



the combination of all the other input and output pins shall be open.

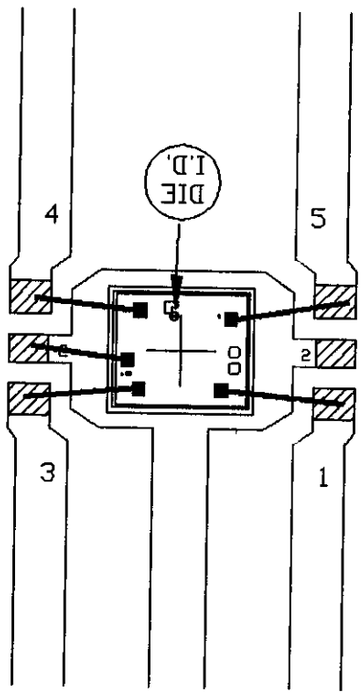
ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 941/809/810/823/824/825/803
MAX 6381
MAX. EXPECTED CURRENT = 700uA AND 15uA

DRAWN BY: HAK TAN
NOTES: 15 uA FOR MAX 6381



▨ - BONDING AREA

NOTE: CAVITY DOWN

PKG.CODE: U5-1		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 64X45	PKG.	AKhan	8/10/95	BUILDSHEET NUMBER: 05-1601-0010	REV.: A
	DESIGN	EB	7/27/95		