SCOPE: **MICROPROCESSOR SUPERVISORY CIRCUIT WITH BATTERY BACKUP**

Device Type	Generic Number
01	MAX703MJA/883B
02	MAX704MJA/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
JA	GDIP1-T8 or CDIP2-T8	8 LEAD CERDIP	J8

Absolute Maximum Ratings

Terminal Voltages (with respect to GND)
- V_{CC} ..... -0.3V to +6V
- VBATT ..... -0.3V to +6V
- All other Inputs (NOTE 1) ..... -0.3V to (V_{CB} +0.3V)

Input Current
- V_{CC} 200mA
- VBATT 50mA
- GND..... 20mA

Output Current
- V_{OUT} ..... Short-Circuit protected for up to 10 sec.
- All other Outputs 20mA

Rate-of Rise, V_{CC}, VBATT 100V/µs

Continuous Power Dissipation ..... T_A=+70°C
- Lead Temperature (soldering, 10 seconds) ..... +300°C
- Storage Temperature ..... -65°C to +160°C

- 8 lead CERDIP(derate 8.00mW/°C above +70°C) 640mW

- Junction Temperature T_J ..... +150°C
- Thermal Resistance, Junction to Case, ΘJC:
  - Case Outline 8 lead CERDIP..... 55°C/W
- Thermal Resistance, Junction to Ambient, ΘJA:
  - Case Outline 8 lead CERDIP..... 125°C/W

Recommended Operating Conditions.
- Ambient Operating Range (T_A) ..... -55°C to 125°C

NOTE 1: V_{CB} is the greater of V_{CC} and VBATT. The input voltage limits on PFI and MR may be exceeded if the current into these pins is limited to less than 10mA.

Stresses above the absolute maximum rating may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1 ELECTRICAL TESTS

TEST	Symbol	CONDITIONS -55° C <=T<= +125°C MAX703:V_{CC}=+4.75V to+5.5V,VBATT=+2.8V MAX704:V_{CC}=+4.5V to +5.5V, VBATT=+2.8V Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
Operating Voltage Range V_{CC}, VBATT		NOTE 1	1,2,3	All	0	5.5	V
Supply Current (Excluding I_{OUT})	I_{SUPPLY}		1,2,3	All		500	µA
I_{SUPPLY} in Battery-Backup Mode (Excluding I_{OUT})		V_{CC}=0V, VBATT=2.8V	1 2,3	All		1.0 5.0	µA
VBATT Standby Current NOTE 2		5.5V>V_{CC}>VBATT+0.2V	1 2,3	All	-0.1 -1.0	0.02 0.02	µA
V_{OUT} Output		I_{OUT}=5mA I_{OUT}=50mA	1,2,3	All	V_{CC}-0.05 V_{CC}-0.5		V
V_{OUT} in Battery-Backup Mode		I_{OUT}=250µA, V_{CC}<VBATT-0.2V	1,2,3	All	VBATT-0.1		V
$\overline{\text{RESET}}$ Threshold	V_{RST}	MAX703 MAX704	1,2,3	01 02	4.50 4.25	4.75 4.50	V
$\overline{\text{RESET}}$ Pulse Width	t_{RST}		9,10,11	All	140	280	ms
$\overline{\text{RESET}}$ Output Voltage	VOH VOL	I_{SOURCE}=800µA I_{SINK}=3.2mA V_{CC}=1.2V, V_{CC} falling, VBATT=0V, I_{SINK}=100µA	1,2,3	All	V_{CC}-1.5	 0.4 0.3	V
$\overline{\text{MR}}$ Input Threshold Low High	 VIL VIH		1,2,3	All	 2.0	 0.8	V
$\overline{\text{MR}}$ Pulse Width	tMR		9,10,11	All	150		ns
$\overline{\text{MR}}$ to $\overline{\text{RESET}}$ Delay	tMD		9,10,11	All		250	ns
$\overline{\text{MR}}$ Pull-Up Current		$\overline{\text{MR}}$=0V	1,2,3	All	100	600	µA
PFI Input Threshold		V_{CC}=5V	1,2,3	All	1.20	1.30	V
PFI Input Current			1,2,3	All	-25	25	nA
PFO Output Voltage	V_{OH} V_{OL}	I_{SOURCE}=800µA I_{SINK}=3.2mA	1,2,3	All	V_{CC}-1.5	 0.4	V

NOTE 1: Either V_{CC} or V_{BATT} can go to 0V if the other is greater than 2.0V.
NOTE 2: "-" = battery-charging current, "+" = battery-discharging current.

TEST	Symbol	CONDITIONS -55° C <=T<= +125°C MAX703:V_{CC}=+4.75V to+5.5V,VBATT=+2.8V MAX704:V_{CC}=+4.5V to +5.5V, VBATT=+2.8V Unless otherwise specified	Device type	Typical Limits **3/**	Units
Battery-Switch Threshold (V_{CC}-VBATT)		$V_{CC}<V_{RST}$ Power-Up $V_{CC}<V_{RST}$ Power-Down	All	20 -20	mV
Battery-Switchover Hysteresis			All	40	mV
$\overline{\text{RESET}}$ Threshold Hysteresis			All	40	mV

NOTE 3: Typical values, not production tested.

	MAX703	MAX704	MAX705	MAX707
Nominal Reset Threshold	4.65V	4.40V	4.65V	4.65V
Minimum Reset Pulse Width	140ms	140ms	140ms	140ms
Nominal Watchdog Timeout Period	NA	NA	1.6	NA
Backup-Battery Switch	yes	yes	no	no
CE Write Protect	no	no	no	no
Power-Fail Comparator	yes	yes	yes	yes
Manual Reset Input	yes	yes	yes	yes
Watchdog Output	no	no	yes	no
Low-Line Output	no	no	no	no
Active High Reset	no	no	no	yes
BATT On Output	no	no	no	no

NOTE: MAX705 and MAX707 are available as SMD 5962-9326701MPA and 5962-9326703MPA

Figure 1. Terminal Connections

CASE OUTLINE	J8	
TERMINAL NUMBER	TERMINAL SYMBOL	
1	V_{OUT}	Supply Output for CMOS RAM. When V_{CC} is above the reset threshold, V_{OUT} connects to V_{CC} through a P-channel MOSFET switch. When V_{CC} is below the reset threshold, the higher of V_{CC} or VBATT is connected to V_{OUT}.
2	V_{CC}	+5V Supply Input.
3	GND	Ground
4	PFI	Power-Fail Comparator Input. When PFI is less than 1.25V, $\overline{\text{PFO}}$ goes low: otherwise $\overline{\text{PFO}}$ remains high. Connect PFI to GND or V_{CC} when not used.
5	$\overline{\text{PFO}}$	Power-Fail Output goes low and sinks current when PFI is less than 1.25V; otherwise $\overline{\text{PFO}}$ remains high.
6	$\overline{\text{MR}}$	Manual-Reset Input generates a reset pulse when pulled below 0.8V. This active-low input is TTL/CMOS compatible and can be shorted to ground with a switch. It has an internal 250µA pull-up current. Leave floating when not used.
7	$\overline{\text{RESET}}$	Reset Output remains low while V_{CC} is below the reset threshold. It remains low for 200ms after V_{CC} rises above the reset threshold or MR goes from low to high.
8	VBATT	Backup-Battery Input. When V_{CC} falls below the reset threshold, VBATT is switched to V_{OUT} if VBATT is 20mV greater than V_{CC}. When V_{CC} rises 20mV above VBATT, V_{CC} is switched to V_{OUT}. The 40mV hysteresis prevents repeated switching if V_{CC} falls slowly.

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9, 10, 11
Group A Test Requirements Method 5005	1, 2, 3, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.