SCOPE: **MICROPROCESSOR SUPERVISORY CIRCUIT**

Device Type	Generic Number
01	MAX691AMJE/883B
02	MAX693AMJE/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
JE	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16

Absolute Maximum Ratings

Terminal Voltages (with respect to GND)
- V_{CC} ..... -0.3V to +6V
- VBATT ..... -0.3V to +6V
- All other Inputs..... -0.3V to (V_{OUT} +0.3V)

Input Current
- V_{CC} Peak 1.0A
- V_{CC} Continuous 250mA
- VBATT Peak 250mA
- VBATT Continuous..... 25mA
- GND, BATT ON 100mA
- All other Outputs 25mA

Continuous Power Dissipation ..... T_A=70°C
- Lead Temperature (soldering, 10 seconds) ..... +300°C
- Storage Temperature ..... -65°C to +150°C

- 16 lead CERDIP(derate 10.00mW/°C above +70°C) 800mW

- Junction Temperature T_J ..... +150°C
- Thermal Resistance, Junction to Case, ΘJC:
  - Case Outline 16 lead CERDIP..... 50°C/W
- Thermal Resistance, Junction to Ambient, ΘJA:
  - Case Outline 16 lead CERDIP..... 100°C/W

Recommended Operating Conditions.
- Ambient Operating Range (T_A) ..... -55°C to 125°C

Stresses above the absolute maximum rating may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1 ELECTRICAL TESTS

TEST	Symbol	CONDITIONS -55 C <=T_A<= +125°C VBATT=+2.8V V_{CC}=4.75V to 5.5V for -01, V_{CC}=4.5V to 5.5V for -02, Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Unit
Operating Voltage Range V_{CC}, VBATT		Note 1	1,2,3	All	0	5.5	V
Output Voltage	V_{OUT}	V_{CC}=4.5V I_{OUT}=250mA I_{OUT}=25mA	1,2,3	All		V_{CC}-.40 V_{CC}-.05	V
V_{CC}- to -V_{OUT} ON Resistance		V_{CC}=4.5V	1,2,3	All		1.6	Ohm
V_{OUT} in Battery-Backup Mode		VBATT=4.5V, I_{OUT}=20mA VBATT=2.8V, I_{OUT}=10mA VBATT=2.0V, I_{OUT}=5mA	1,2,3	All	VBATT-0.3 VBATT-.25 VBATT-.15		V
VBATT-to-V_{OUT} ON Resistance		VBATT=4.5V VBATT=2.8V VBATT=2.0V	1,2,3	All		15 25 30	Ohm
Supply Current in Normal Operating Mode (Excludes I_{OUT})		V_{CC}>VBATT-1V	1,2,3	All		100	µA
Supply Current in Battery-Backup Mode (Excludes I_{OUT})		V_{CC}<VBATT -1.2V, VBATT =2.8V NOTE 2	1 2,3	All		1 5	µA
VBATT Standby Current		VBATT +0.2V<=V_{CC} NOTE 3	1 2,3	All	-0.1 -1.0	0.02 0.02	µA
BATT ON Output Low Voltage		I_{SINK}=3.2mA	1,2,3	All		0.4	V
BATT ON Output Short-Circuit Current		Source Current	1,2,3	All	1.0	100	µA
RESET AND WATCHDOG TIMER							
Reset Threshold Voltage			1,2,3	01 02	4.50 4.25	4.75 4.50	V
Reset Active Timeout Period, Internal Oscillator		Power up	9,10,11	All	140	280	ms
Watchdog Timeout Period Internal Oscillator		Long Period Short Period	9,10,11	All	1.0 70	2.25 140	sec ms
Minimum Watchdog Input Pulse Width		V_{IL}=0.8V, V_{IH}=0.75 x V_{CC}	9,10,11	All	100		ns
$\overline{\text{RESET}}$ Output Voltage		I_{SINK}=50µA, V_{CC}=1V, VBATT =0V,V_{CC} Falling I_{SINK}=3.2mA,V_{CC}=4.25V I_{SOURCE}=1.6mA, V_{CC}=5V	1,2,3	All	 3.5	0.3 0.4	V
$\overline{\text{RESET}}$ Output Short-Circuit Current		Output Source Current	1,2,3	All		20	mA
RESET Output Voltage Low		I_{SINK}=3.2mA NOTE 4	1,2,3	All		0.4	V

TABLE 1 ELECTRICAL TESTS

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$\overline{\text{LL}}$ Low Line Output Voltage		I_{SINK}=3.2mA, V_{CC}=4.25V I_{SOURCE}=1µA, V_{CC}=5V	1,2,3	All	3.5	0.4	V
$\overline{\text{LL}}$ Low Line Output Short-Circuit Current		Output Source Current	1,2,3	All	+1.0	100	µA
$\overline{\text{WDO}}$ Output Voltage		I_{SINK}=3.2mA I_{SOURCE}=500µA, V_{CC}=5V	1,2,3	All	3.5	0.4	V
$\overline{\text{WDO}}$ Output Short-Circuit Current		Output Source current	1,2,3	All		10	mA
WDI Threshold Voltage		V_{IH} NOTE 5 V_{IL}	1,2,3	All	.75xV_{CC}	0.8	V
WDI Input Current		WDI=0V WDI=V_{OUT}	1,2,3	All	-50	50	µA
POWER-FAIL COMPARATOR							
PFI Input Threshold		V_{CC}=5V	1,2,3	All	1.2	1.3	V
PFI Leakage Current			1,2,3	All		±25	nA
$\overline{\text{PFO}}$ Output Voltage		I_{SINK}=3.2mA I_{SOURCE}=1µA, V_{CC}=5V	1,2,3	All	3.5	0.4	V
$\overline{\text{PFO}}$ Output Short-circuit Current		Output Source Current	1,2,3	All	1.0	100	µA
CHIP-ENABLING GATING							
$\overline{\text{CE}}$ IN Leakage Current		Disable Mode	1,2,3	All		±1.0	µA
$\overline{\text{CE}}$ IN to $\overline{\text{CE}}$ OUT Resistance		Enable Mode NOTE 6	1,2,3	All		150	Ohm
$\overline{\text{CE}}$ OUT Short-Circuit Current (Reset Active)		Disable Mode, $\overline{\text{CE}}$ OUT=0V	1,2,3	All	0.1	2.0	mA
$\overline{\text{CE}}$ IN to $\overline{\text{CE}}$ OUT Propagation Delay		50 Ohm source impedance driver, CLOAD=50pF NOTE 7	9,10,11	All		10	ns
$\overline{\text{CE}}$ OUT Output Voltage High (Reset Active)		V_{CC}=5V, I_{OUT}=-100µA V_{CC}=0V,VBATT=2.8V, I_{OUT}=1µA	1,2,3	All	3.5 2.7		V

TABLE 1 ELECTRICAL TESTS

TEST	Symbol	CONDITIONS -55 C <=T_A<= +125°C VBATT=+2.8V V_{CC}=4.75V to 5.5V for -01, V_{CC}=4.5V to 5.5V for -02, Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
INTERNAL OSCILLATOR							
OSC IN Leakage Current		OSC SEL=0V	1,2,3	All		± 5.0	µA
OSC IN Input Pullup Current		OSC SEL=V_{OUT} or floating, OSC IN=0V	1,2,3	All		100	µA
OSC SEL Input Pullup Current		OSC IN=0V	1,2,3	All		100	µA

NOTE 1: Either V_{CC} or VBATT can go to 0V, if the other is greater than 2.0V.

NOTE 2: The supply current drawn by the device from the battery excluding I_{OUT} typically goes to 10µA when (VBATT -1V)<V_{CC}<VBATT. In most applications, this is a brief period as V_{CC} falls through this region.

NOTE 3: "+" = battery-discharging current. "-" = battery-charging current.

NOTE 4: RESET is an open-drain output and sinks current only.

NOTE 5: WDI is internally connected to a voltage divider between V_{OUT} and GND. If unconnected, WDI is driven to 1.6V typical, disabling the watchdog function.

NOTE 6: The chip-enable resistance is tested with V_{CC}=4.75V for MAX691A and V_{CC}=4.5V for MAX693A

$\overline{V_{CE}\ IN}$ = $\overline{V_{CE}\ OUT}$ = $V_{CC}/2$

NOTE 7: The chip-enable propagation delay is measured from the 50% point at $\overline{CE}$ IN to the 50% point at $\overline{CE}$ out.

	MAX691A	MAX693A
Nominal Reset Threshold	4.65V	4.4V
Minimum Reset Pulse Width	140/adj.	140/adj.
Nominal Watchdog Timeout Period	1.6/adj.	1.6/adj
Backup-Battery Switch	x	x
CE Write Protect	x	x
Power-Fail Comparator	x	x
Watchdog Output	x	x
Low-Line Output	x	x
Active High Reset	x	x
BATT On Output	x	x

Figure 1. Terminal Connections

CASE OUTLINES	J16	
TERMINAL NUMBER	TERMINAL FUNCTION	TERMINAL SYMBOL
1	Battery-backup Input. Connect to external battery or capacitor and charging circuit. If backup battery is not used, connect to GND.	VBATT
2	Output Supply Voltage. When V_{CC} is greater than VBATT and above the reset threshold, V_{OUT} connects to V_{CC}. When V_{CC} falls below VBATT and is below the reset threshold, V_{OUT} connects to VBATT. Connect a 0.1µF capacitor from V_{OUT} to GND. Connect V_{OUT} to V_{CC} if no backup battery is used.	V_{OUT}
3	Input Supply Voltage, 5V input.	V_{CC}
4	Ground. 0V reference for all signals.	GND
5	Battery ON Output. When V_{OUT} switches to VBATT, BATT ON goes high. When VOUT switches to VCC, BATT ON goes low. Connect the base of a PNP through a current-limiting resistor to BATT ON for V_{OUT} current requirements greater than 250mA.	BATT ON
6	$\overline{\text{LOW LINE}}$ output goes low when V_{CC} falls below the reset threshold. It returns high as soon as V_{CC} rises above the reset threshold.	$\overline{\text{LOW LINE}}$
7	External Oscillator Input. When OSC SEL is unconnected or driven high, a 10µA pull-up connects from V_{OUT} to OSC IN, the internal oscillator sets the reset and watchdog timeout periods, and OSC IN selects between fast and slow watchdog timeout periods. When OSC SEL is driven low, the reset and watchdog timeout periods may be set either by a capacitor from OSC IN to ground or by an external clock at OSC IN.	OSC IN
8	Oscillator Select. When OSC SEL is unconnected or driven high, the internal oscillator sets the reset delay and watchdog timeout period. When OSC SEL is low, the external oscillator input (OSC IN) is enabled. OSC SEL has a 10µA internal pull-up.	OSC SEL
9	Power-Fail Input. This is the noninverting input to the power-fail comparator. When PFI is less than 1.25V, $\overline{\text{PFO}}$ goes low. When PFI is not used, connect PFI to GND or V_{OUT}.	PFI
10	Power-Fail Output. This is the output of the power-fail comparator. $\overline{\text{PFO}}$ goes low when PFI is less than 1.25V. This is an uncommitted comparator, and has no effect on any other internal circuitry.	$\overline{\text{PFO}}$
11	Watchdog Input. WDI is a three-level input. If WDI remains either high or low for longer than the watchdog time-out period, $\overline{\text{WDO}}$ goes low and reset is asserted for the reset timeout period. $\overline{\text{WDO}}$ remains low until the next transition at WDI. Leaving WDI unconnected disables the watchdog function. WDI connects to an internal voltage divider between V_{OUT} and GND, which sets it to mid-supply when left unconnected.	WDI
12	Chip-Enable Output. $\overline{\text{CE}}$ OUT goes low only when $\overline{\text{CE}}$ IN is low and V_{CC} is above the reset threshold. If $\overline{\text{CE}}$ IN is low when reset is asserted, $\overline{\text{CE}}$ OUT will stay low for 15µs or until $\overline{\text{CE}}$ IN goes high, whichever occurs first.	$\overline{\text{CE}}$ OUT
13	Chip-Enable Input. The input to chip-enable gating circuit. If $\overline{\text{CE}}$ IN is not used, connect $\overline{\text{CE}}$ IN to GND or V_{OUT}.	$\overline{\text{CE}}$ IN
14	Watchdog Output. If WDI remains high or low longer than the watchdog timeout period, $\overline{\text{WDO}}$ goes low and reset is asserted for the reset timeout period. $\overline{\text{WDO}}$ returns high on the next transition at WDI. $\overline{\text{WDO}}$ remains high if WDI is unconnected.	$\overline{\text{WDO}}$
15	$\overline{\text{RESET}}$ Output goes low whenever V_{CC} falls below the reset threshold. $\overline{\text{RESET}}$ will remain low typically for 200ms after V_{CC} crosses the reset threshold on power up.	$\overline{\text{RESET}}$
16	RESET is an active-high output. It is open drain, and the inverse of $\overline{\text{RESET}}$.	RESET

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125C, minimum
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9, 10, 11
Group A Test Requirements Method 5005	1, 2, 3, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.