19-2530; Rev 0; 7/02

MAXIM

µP Reset Circuits with Capacitor-Adjustable Reset/Watchdog Timeout Delay

General Description

The MAX6746–MAX6753 low-power microprocessor (µP) supervisory circuits monitor single/dual system supply voltages from 1.575V to 5V and provide maximum adjustability for reset and watchdog functions. These devices assert a reset signal whenever the V_{CC} supply voltage or RESET IN falls below its reset threshold or when manual reset is pulled low. The reset output remains asserted for the reset timeout period after V_{CC} and RESET IN rise above the reset threshold. The reset function features immunity to power-supply transients.

The MAX6746–MAX6753 have factory-trimmed reset threshold voltages in approximately 100mV increments from 1.575V to 5.0V and/or adjustable reset threshold voltages using external resistors.

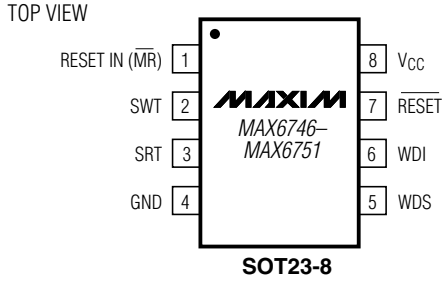
The reset and watchdog delays are adjustable with external capacitors. The MAX6746–MAX6751 contain a watchdog select input that extends the watchdog timeout period by 128x. The MAX6752/MAX6753 contain a window watchdog timer that looks for activity outside an expected window of operation.

The MAX6746–MAX6753 are available with a push-pull or open-drain active-low $\overline{RESET}$ output. The MAX6746–MAX6753 are available in an 8-pin SOT23 package and are fully specified over the automotive temperature range (-40°C to +125°C).

Applications

Medical Equipment
Automotive
Intelligent Instruments
Portable Equipment
Battery-Powered Computers/Controllers
Embedded Controllers
Critical µP Monitoring
Set-Top Boxes
Computers

Pin Configurations



SOT23-8

( ) ARE FOR MAX6746 AND MAX6747 ONLY.

Pin Configurations continued at end of data sheet.

Features

- **Factory-Set Reset Threshold Options from 1.575V to 5V in ~100mV Increments**
- **Adjustable Reset Threshold Options**
- **Single/Dual Voltage Monitoring**
- **Capacitor-Adjustable Reset Timeout**
- **Capacitor-Adjustable Watchdog Timeout**
- **Min/Max (Windowed) Watchdog Option**
- **Manual Reset Input Option**
- **Guaranteed $\overline{RESET}$ Valid for $V_{CC} \geq 1V$**
- **2.7µA Supply Current**
- **Push-Pull or Open-Drain $\overline{RESET}$ Output Options**
- **Power-Supply Transient Immunity**
- **Small 8-Pin SOT23 Packages**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX6746KA_ _-T	-40°C to +125°C	8 SOT23-8
MAX6747KA_ _-T	-40°C to +125°C	8 SOT23-8
MAX6748KA-T*	-40°C to +125°C	8 SOT23-8
MAX6749KA-T*	-40°C to +125°C	8 SOT23-8
MAX6750KA_ _-T*	-40°C to +125°C	8 SOT23-8
MAX6751KA_ _-T*	-40°C to +125°C	8 SOT23-8
MAX6752KA_ _-T*	-40°C to +125°C	8 SOT23-8
MAX6753KA_ _-T*	-40°C to +125°C	8 SOT23-8

**Future product—contact factory for availability.*

Note: *"_ _" represents the two number suffix needed when ordering the reset threshold voltage value for the MAX6746/MAX6747 and MAX6750–MAX6753. The reset threshold voltages are available in approximately 100mV increments. Table 2 contains the suffix and reset factory-trimmed voltages. All devices are available in tape-and-reel only. There is a 2500-piece minimum order increment for standard versions (see Table 3). Sample stock is typically held on standard versions only. Nonstandard versions require a minimum order increment of 10,000 pieces. Contact factory for availability.*

Selector Guide appears at end of data sheet.

Typical Operating Circuit appears at end of data sheet.

µP Reset Circuits with Capacitor-Adjustable Reset/Watchdog Timeout Delay

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6.0V
SRT, SWT, SET0, SET1, RESET IN, WDS, $\overline{MR}$, WDI, to GND .....-0.3V to (V_{CC} + 0.3V)
$\overline{RESET}$ (Push-Pull) to GND.....-0.3V to (V_{CC} + 0.3V)
$\overline{RESET}$ (Open Drain) to GND .....-0.3V to +6.0V
Input Current (All Pins) .....±20mA
Output Current ($\overline{RESET}$) .....±20mA

Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23 (derate 8.9mW/°C above +70°C).....714mW
Operating Temperature Range .....-40°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.2V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	T_A = 0°C to +125°C		1.0		5.5	V
		T_A = -40°C to 0°C		1.2		5.5	
Supply Current	I_{CC}	V_{CC} ≤ 5.5V			4.0	7.5	µA
		V_{CC} ≤ 3.3V			3.2	6.5	
		V_{CC} ≤ 2.0V			2.7	6	
V_{CC} Reset Threshold	V_{TH}	See V_{TH} selection table	T_A = 0°C to +85°C	V_{TH} - 2.5%	V_{TH}	V_{TH} + 2.5%	V
			T_A = -40°C to+125°C	V_{TH} - 3%		V_{TH} + 3%	
Hysteresis	V_{HYST}				0.8		%
V_{CC} to Reset Delay		V_{CC} falling from V_{TH} + 100mV to V_{TH} - 100mV at 1mV/µs			20		µs
Reset Timeout Period	t_{RP}	C_{SRT} = 1500pF		5.692	7.590	9.487	ms
		C_{SRT} = 100pF			0.506		
SRT Ramp Current	I_{RAMP}	V_{SRT} = 0 to 1.23V; V_{CC} = 1.6V to 5V		200	250	300	nA
SRT Ramp Threshold	V_{RAMP}	V_{CC} = 1.6V to 5V (V_{RAMP} rising)		1.200	1.265	1.330	V
Normal Watchdog Timeout Period (MAX6746–MAX6751)	t_{WD}	C_{SWT} = 1500pF		5.692	7.590	9.487	ms
		C_{SWT} = 100pF			0.506		
Extended Watchdog Timeout (MAX6746–MAX6751)	t_{WD}	C_{SWT} = 1500pF		728.6	971.5	1214.4	ms
		C_{SWT} = 100pF			64.77		
Slow Watchdog Period (MAX6752/MAX6753)	t_{WD2}	C_{SWT} = 1500pF		728.6	971.5	1214.4	ms
		C_{SWT} = 100pF			64.77		
Fast Watchdog Timeout Period, SET Ratio = 8, (MAX6752/MAX6753)	t_{WD1}	C_{SWT} = 1500pF		91.08	121.43	151.80	ms
		C_{SWT} = 100pF			8.09		
Fast Watchdog Timeout Period, SET Ratio = 16, (MAX6752/MAX6753)	t_{WD1}	C_{SWT} = 1500pF		45.53	60.71	75.89	ms
		C_{SWT} = 100pF			4.05		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +1.2V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fast Watchdog Timeout Period, SET Ratio = 64, (MAX6752/MAX6753)	t_{WD1}	C_{SWT} = 1500pF	11.38	15.18	18.98	ms
		C_{SWT} = 100pF		1.01		
Fast Watchdog Minimum Period (MAX6752/MAX6753)			2000			ns
SWT Ramp Current	I_{RAMP}	V_{SWT} = 0 to 1.23V, V_{CC} = 1.6V to 5V	200	250	300	nA
SWT Ramp Threshold	V_{RAMP}	V_{CC} = 1.6V to 5V (V_{RAMP} rising)	1.20	1.265	1.33	V
$\overline{RESET}$ Output Voltage LOW Open-Drain, Push-Pull (Asserted)	V_{OL}	V_{CC} ≥ 1.0V, I_{SINK} = 50µA			0.3	V
		V_{CC} ≥ 2.7V, I_{SINK} = 1.2mA			0.3	
		V_{CC} ≥ 4.5V, I_{SINK} = 3.2mA			0.4	
$\overline{RESET}$ Output Voltage HIGH, Push-Pull (Not Asserted)	V_{OH}	V_{CC} ≥ 1.8V, I_{SOURCE} = 200µA	0.8 x V_{CC}			V
		V_{CC} ≥ 2.25V, I_{SOURCE} = 500µA	0.8 x V_{CC}			
		V_{CC} ≥ 4.5V, I_{SOURCE} = 800µA	0.8 x V_{CC}			
$\overline{RESET}$ Output Leakage Current, Open Drain	I_{LKG}	V_{CC} > V_{TH}, reset not asserted, $V_{\overline{RESET}}$ = 5.5V			1.0	µA
DIGITAL INPUTS ($\overline{MR}$, SET0, SET1, WDI, WDS)						
Input Logic Levels	V_{IL}	V_{CC} ≥ 4.0V			0.8	V
	V_{IH}		2.4			
	V_{IL}	V_{CC} < 4.0V			0.3 x V_{CC}	
	V_{IH}		0.7 x V_{CC}			
$\overline{MR}$ Minimum Pulse Width			1			µs
$\overline{MR}$ Glitch Rejection				100		ns
$\overline{MR}$ to RESET Delay				200		ns
$\overline{MR}$ Pullup Resistance		Pullup to V_{CC}	12	20	28	kΩ
WDI Minimum Pulse Width			300			ns
RESET IN						
RESET IN Threshold	$V_{RESET\ IN}$	T_A = 0°C to +85°C	1.239	1.265	1.290	V
		T_A = -40°C to +125°C	1.227		1.303	
RESET IN Leakage Current	$I_{RESET\ IN}$		-50	±1	+50	nA
RESET IN to $\overline{RESET}$ Delay		RESET IN falling at 1mV/µs		20		µs

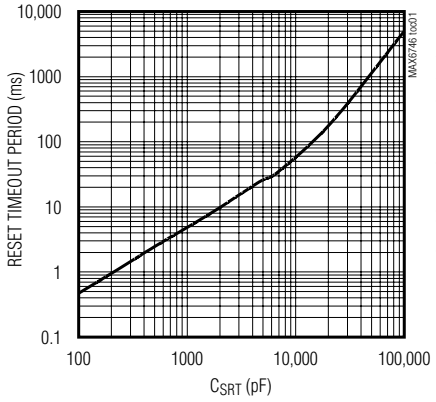
Note 1: Production testing done at T_A = +25°C. Over temperature limits are guaranteed by design.

µP Reset Circuits with Capacitor-Adjustable Reset/Watchdog Timeout Delay

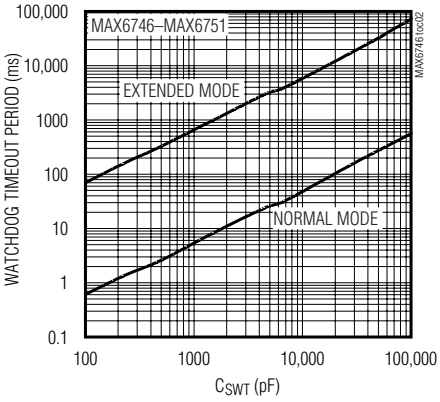
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

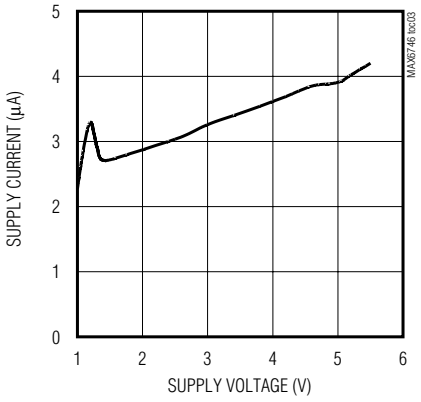
RESET TIMEOUT PERIOD vs. C_{SRT}



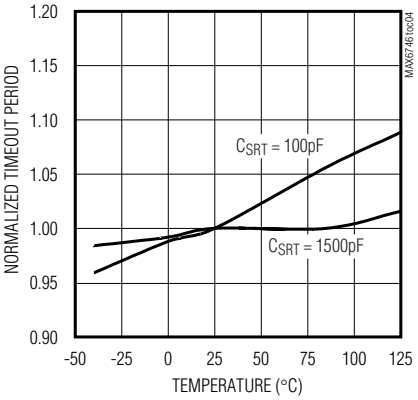
WATCHDOG TIMEOUT PERIOD vs. C_{SWT}



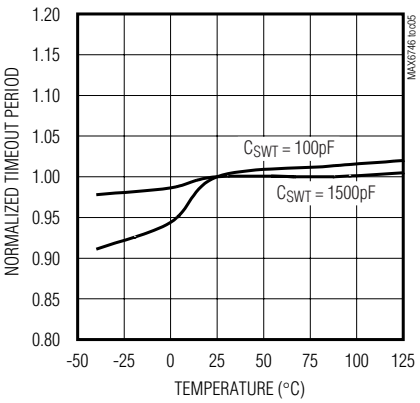
SUPPLY CURRENT vs. SUPPLY VOLTAGE



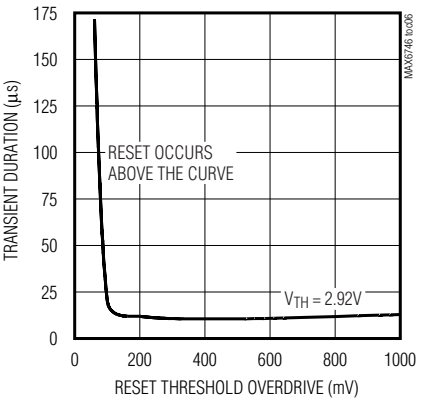
NORMALIZED RESET TIMEOUT PERIOD vs. TEMPERATURE



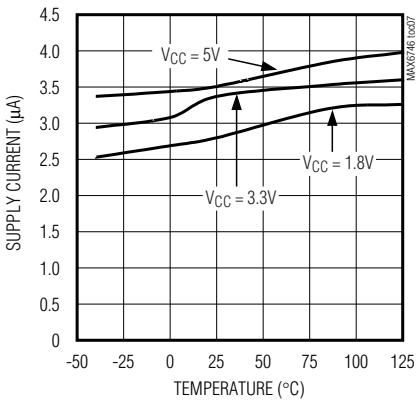
NORMALIZED WATCHDOG TIMEOUT PERIOD vs. TEMPERATURE



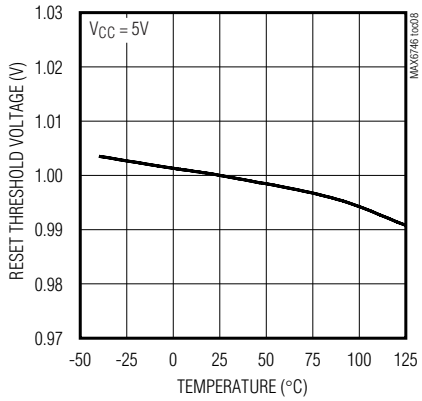
MAXIMUM TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



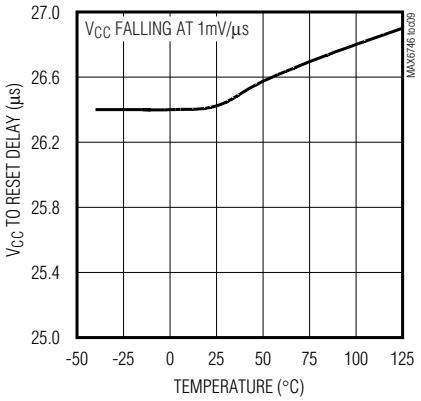
SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED RESET IN THRESHOLD VOLTAGE vs. TEMPERATURE



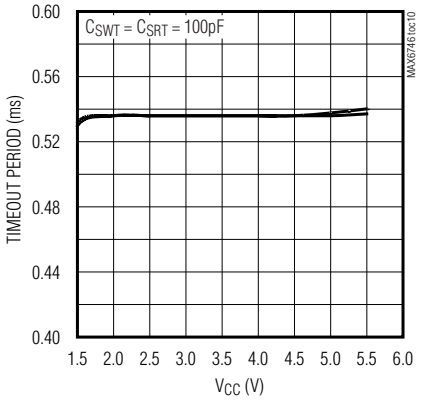
V_{CC} TO RESET DELAY vs. TEMPERATURE (V_{CC} FALLING)



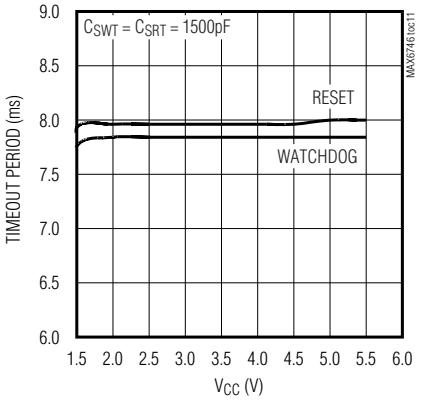
Typical Operating Characteristics (continued)

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

RESET AND WATCHDOG TIMEOUT PERIOD vs. V_{CC}



RESET AND WATCHING TIMEOUT PERIOD vs. V_{CC}



Pin Description

PIN			NAME	FUNCTION
MAX6746 MAX6747	MAX6748–MAX6751	MAX6752 MAX6753		
1	—	—	$\overline{MR}$	Manual Reset Input. Pull $\overline{MR}$ low to manually reset the device. Reset remains asserted for the reset timeout period after $\overline{MR}$ is released.
—	1	—	RESET IN	Reset Input. High-impedance input to the adjustable reset comparator. Connect RESET IN to the center point of an external resistor-divider to set the threshold of the externally monitored voltage.
—	—	1	SET0	Logic Input. SET0 selects watchdog window ratio or disables the watchdog timer. See Table 1.
2	2	2	SWT	Watchdog Timeout Input. MAX6746–MAX6751: Connect a capacitor between SWT and ground to set the basic watchdog timeout period (t_{WD}). Determine the period by the formula $t_{WD} = 5.06 \times 10^6 \times C_{SWT}$ with t_{WD} in seconds and C_{SWT} in Farads. Extend the basic watchdog timeout period by using the WDS input. MAX6752/MAX6753: Connect a capacitor between SWT and ground to set the slow watchdog timeout period (t_{WD2}). Determine the slow watchdog period by the formula: $t_{WD2} = 0.65 \times 10^9 \times C_{SWT}$ with t_{WD2} in seconds and C_{SWT} in Farads. The fast watchdog timeout period is set by pinstrapping SET0 and SET1. See Table 1.
3	3	3	SRT	Reset Timeout Input. Connect a capacitor from SRT to GND to select the reset timeout period. Determine the period as follows: $t_{RP} = 5.06 \times 10^6 \times C_{SRT}$ with t_{RP} in seconds and C_{SRT} in Farads.
4	4	4	GND	Ground

µP Reset Circuits with Capacitor-Adjustable Reset/Watchdog Timeout Delay

Pin Description (continued)

PIN			NAME	FUNCTION
MAX6746 MAX6747	MAX6748– MAX6751	MAX6752 MAX6753		
5	5	—	WDS	Watchdog Select Input. WDS selects the watchdog mode. Connect WDS to ground to select normal mode and the watchdog timeout period. Connect WDS to V_{CC} to select extended mode, multiplying the basic timeout period by a factor of 128. A change in the state of WDS clears the watchdog timer.
—	—	5	SET1	Logic Input. SET1 selects the watchdog window ratio or disables the watchdog timer. See Table 1.
6	6	6	WDI	Watchdog Input. MAX6746–MAX6751: A falling transition must occur on WDI within the selected watchdog timeout period or a reset pulse occurs. The watchdog timer clears when a transition occurs on WDI or whenever $\overline{RESET}$ is asserted. MAX6752/MAX6753: WDI falling transitions within periods shorter than t_{WD1} or longer than t_{WD2} force $\overline{RESET}$ to assert low for the reset timeout period. The watchdog timer begins to count after $\overline{RESET}$ is deasserted. The watchdog timer clears when a valid transition occurs on WDI or whenever $\overline{RESET}$ is asserted. See the *Watchdog Timer* section.
7	7	7	$\overline{RESET}$	Push/Pull or Open-Drain Reset Output. $\overline{RESET}$ asserts whenever V_{CC} or RESET IN drops below the selected reset threshold voltage (V_{TH} or $V_{RESET\ IN}$, respectively) or manual reset is pulled low. $\overline{RESET}$ remains low for the reset timeout period after all reset conditions are deasserted, and then goes high. The watchdog timer triggers a reset pulse (t_{RP}) whenever a watchdog fault occurs.
8	8	8	V_{CC}	Supply Voltage. V_{CC} is the power-supply input and the input for fixed threshold V_{CC} monitor.

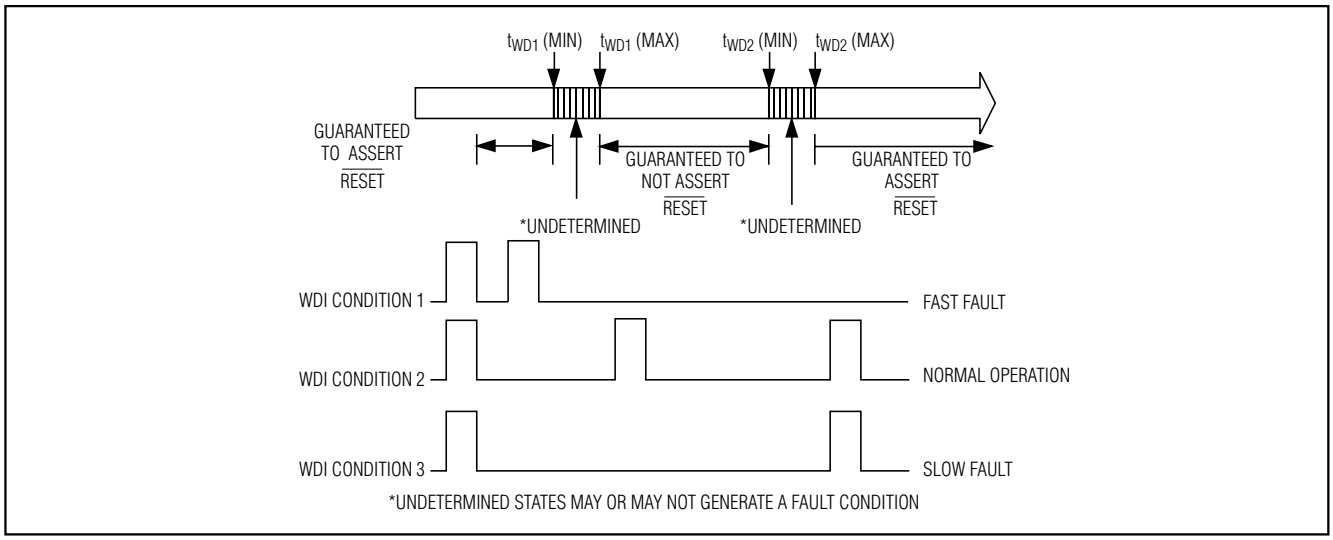


Figure 1. MAX6752/MAX6753 Detailed Watchdog Input Timing Relationship

Detailed Description

The MAX6746–MAX6753 assert a reset signal whenever the V_{CC} supply voltage or RESET IN falls below its reset threshold. The reset output remains asserted for the reset timeout period after V_{CC} and RESET IN rise above its respective reset threshold. A watchdog timer triggers a reset pulse whenever a watchdog fault occurs.

The reset and watchdog delays are adjustable with external capacitors. The MAX6746–MAX6751 contain a watchdog select input that extends the watchdog timeout period to 128x.

The MAX6752 and MAX6753 have a sophisticated watchdog timer that detects when the processor is running outside an expected window of operation. The watchdog signals a fault when the input pulses arrive too early (faster that the selected t_{WD1} timeout period) or too late (slower than the selected t_{WD2} timeout period) (see Figure 1).

Reset Output

The reset output is typically connected to the reset input of a µP. A µP's reset input starts or restarts the µP in a known state. The MAX6746–MAX6753 µP supervisory circuits provide the reset logic to prevent code-execution errors during power-up, power-down, and brownout conditions (see the *Typical Operating Circuit*). $\overline{RESET}$ changes from high to low whenever the monitored voltage, RESET IN and/or V_{CC} drop below the reset threshold voltages. Once $V_{RESET\ IN}$ and/or V_{CC} exceeds its respective reset threshold voltage(s), $\overline{RESET}$ remains low for the reset timeout period, then goes high.

$\overline{RESET}$ is guaranteed to be in the correct logic state for V_{CC} greater than 1V. For applications requiring valid reset logic when V_{CC} is less than 1V, see the section *Ensuring a Valid RESET Output Down to V_{CC} = 0V.*

RESET IN Threshold

The MAX6748–MAX6751 monitor the voltage on RESET IN using an adjustable reset threshold ($V_{RESET\ IN}$) set with an external resistor voltage-divider (Figure 2). Use the

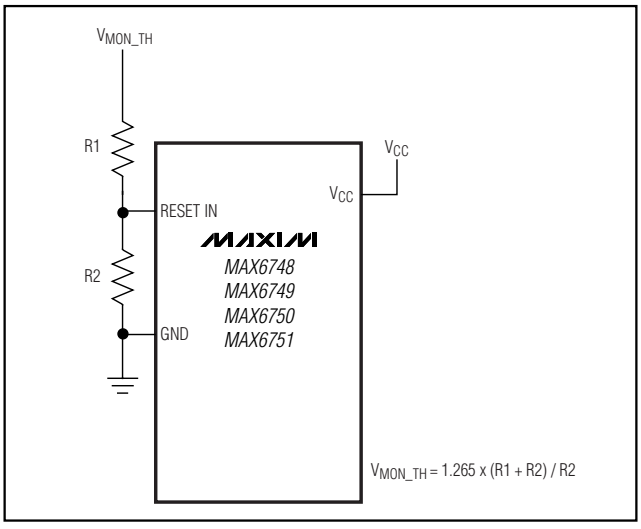


Figure 2. Calculating the Monitored Threshold Voltage (V_{MON_TH})

µP Reset Circuits with Capacitor-Adjustable Reset/Watchdog Timeout Delay

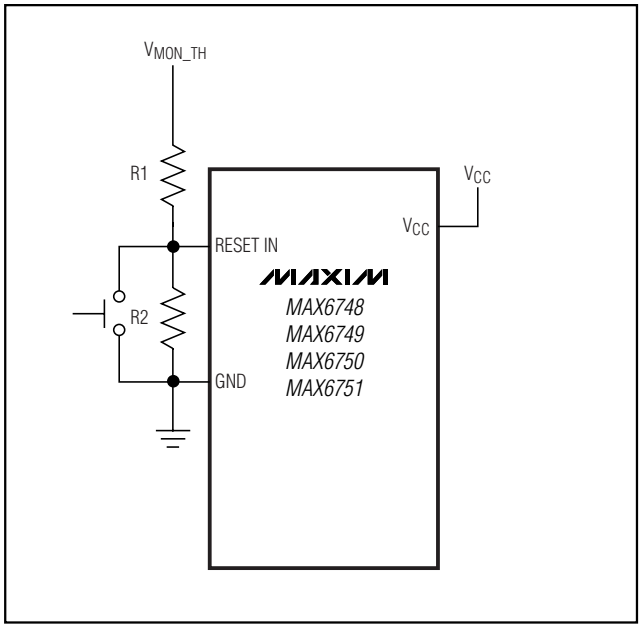


Figure 3. Adding an External Manual Reset Function to the MAX6748–MAX6751

following formula to calculate the externally monitored voltage (V_{MON_TH}):

$$V_{MON\_TH} = V_{RESET\ IN} \times (R1 + R2) / R2$$

where V_{MON_TH} is the desired reset threshold voltage and V_{TH} is the reset input threshold (1.265V). Resistors R1 and R2 can have very high values to minimize current consumption due to low leakage currents. Set R2 to some conveniently high value (500kΩ, for example) and calculate R1 based on the desired reset threshold voltage, using the following formula:

$$R1 = R2 \times (V_{MON\_TH}/V_{RESET\ IN} - 1)\ (\Omega)$$

The MAX6748 and MAX6749 do not monitor V_{CC} supply voltage, therefore, V_{CC} must be greater than 1.6V to guarantee RESET IN threshold accuracy and timing performance. The MAX6748 and MAX6749 can be configured to monitor V_{CC} voltage by connecting V_{CC} to V_{MON_TH}.

Dual-Voltage Monitoring (MAX6750/MAX6751)

The MAX6750 and MAX6751 contain both factory-trimmed threshold voltages and an adjustable reset threshold input, allowing the monitoring of two voltages, V_{CC} and V_{MON_TH} (see Figure 2). $\overline{RESET}$ is asserted when either of the voltages falls below it respective threshold voltages.

Manual Reset (MAX6746/MAX6747)

Many µP-based products require manual reset capability, to allow an operator or external logic circuitry to initiate a reset. The manual reset input ($\overline{MR}$) can connect directly to a switch without an external pullup resistor or debouncing network. $\overline{MR}$ is internally pulled up to V_{CC} and, therefore, can be left unconnected if unused.

$\overline{MR}$ is designed to reject fast, falling transients (typically 100ns pulses) and it must be held low for a minimum of 1µs to assert the reset output. A 0.1µF capacitor from $\overline{MR}$ to ground provides additional noise immunity. After $\overline{MR}$ transitions from low to high, reset remains asserted for the duration of the reset timeout period.

A manual reset option can easily be implemented with the MAX6748–MAX6751 by connecting a normally open momentary switch in parallel with R2 (Figure 3). When the switch is closed, the voltage on RESET IN goes to zero, initiating a reset. Similar to the MAX6746/MAX6747 manual reset, reset remains asserted while the voltage at RESET IN is zero and for the reset timeout period after the switch is opened.

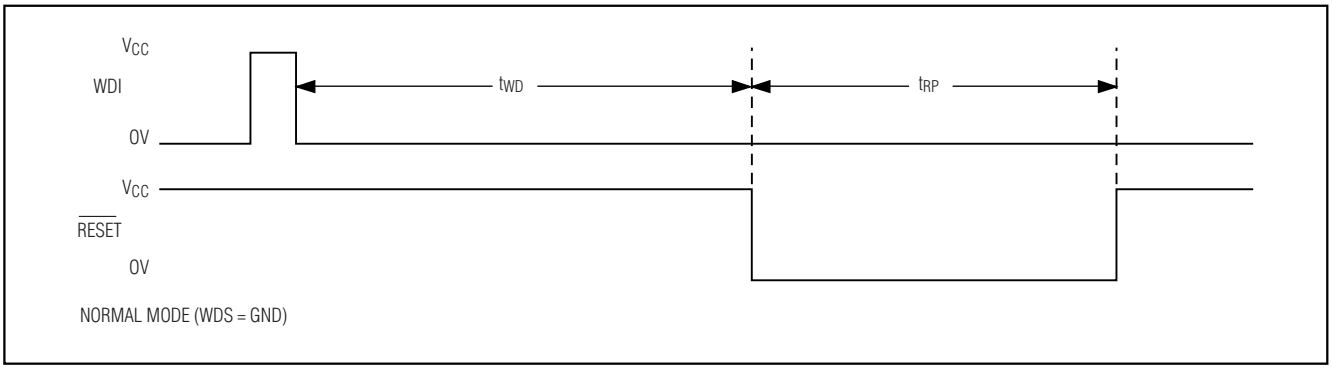


Figure 4a. Watchdog Timing Diagram, WDS = GND

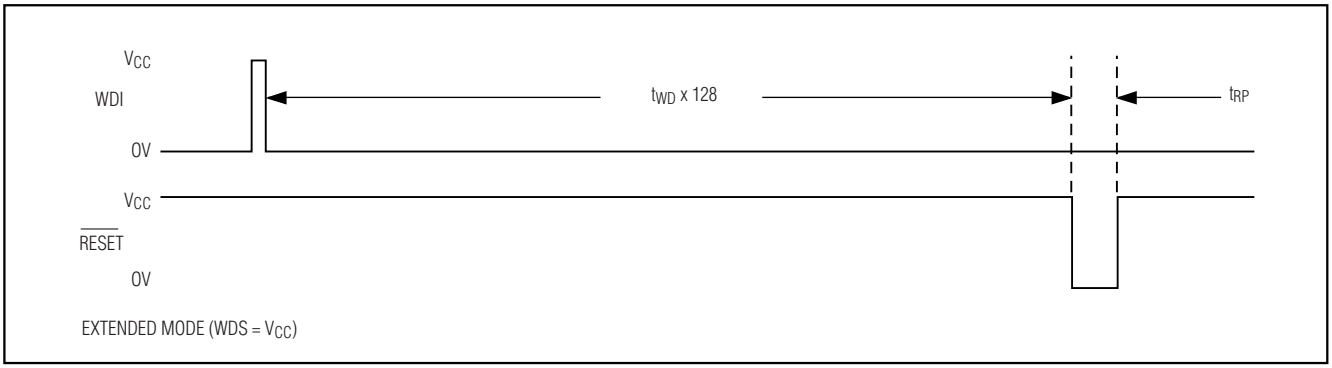


Figure 4b. Watchdog Timing Diagram, WDS = V_{CC}

Watchdog Timer

MAX6746–MAX6751

The watchdog's circuit monitors the µP's activity. It the µP does not toggle the watchdog input (WDI) within t_{WD} (user-selected), $\overline{RESET}$ asserts for the reset timeout period. The internal watchdog timer is cleared by any event that asserts $\overline{RESET}$, by a falling transition at WDI (which can detect pulses as short as 300ns) or by a transition at WDS. The watchdog timer remains cleared while reset is asserted; as soon as reset is released, the timer starts counting.

The MAX6746–MAX6751 feature two modes of watchdog operation: normal mode and extended mode. In normal mode (Figure 4a), the watchdog timeout period is determined by the value of the capacitor connected between SWT and ground. In extended mode (Figure 4b), the watchdog timeout period is multiplied by 128. For example, in extended mode, a 0.1µF capacitor gives a watchdog timeout period of 65s (see the Extended-Mode Watchdog Timeout Period vs. C_{SWT} graph in the *Typical Operating Characteristics*).

MAX6752/MAX6753

The MAX6752 and MAX6753 have a windowed watchdog timer that asserts $\overline{RESET}$ for the adjusted reset timeout period when the watchdog recognizes a fast watchdog fault ($t_{WDI} < t_{WD1}$), or a slow watchdog fault (period > t_{WD2}). The reset timeout period is adjusted independently of the watchdog timeout period.

The slow watchdog period, t_{WD2} is calculated as follows:

$$t_{WD2} = 0.65 \times 10^9 \times C_{SWT}$$

with t_{WD2} in seconds and C_{SWT} in Farads.

The fast watchdog period, t_{WD1}, is selectable as a ratio from the slow watchdog fault period (t_{WD2}). Select the fast watchdog period by pinstrapping SET0 and SET1, where HIGH is V_{CC} and LOW is GND. Table 1 illustrates the SET0 and SET1 configuration for the 8, 16, and 64 window ratio (t_{WD2}/t_{WD1}).

Table 1. Min/MAX Watchdog Setting

SET0	SET1	RATIO
LOW	LOW	8
LOW	HIGH	16
HIGH	LOW	Watchdog Disabled
HIGH	HIGH	64

For example, if C_{SWT} is 1500pF, and SET0 and SET1 are low, then t_{WD2} is 975ms (typ) and t_{WD1} is 122ms (typ).

$\overline{RESET}$ asserts if the watchdog input has two falling edges too close to each other (faster than t_{WD1}) (Figure 5a) or falling edges that are too far apart (slower than t_{WD2}) (Figure 5b). Normal watchdog operation is displayed in (Figure 5c). The internal watchdog timer is cleared when a WDI falling edge is detected within the valid watchdog window or when $\overline{RESET}$ is deasserted. All WDI inputs are ignored while $\overline{RESET}$ is asserted.

The watchdog timer begins to count after $\overline{RESET}$ is deasserted. The watchdog timer clears and begins to count after a valid WDI falling logic input. WDI falling transitions within periods shorter than t_{WD1} or longer than t_{WD2} force $\overline{RESET}$ to assert low for the reset timeout period. WDI falling transitions within the t_{WD1} and t_{WD2} window do not assert $\overline{RESET}$. WDI transitions between $t_{WD1(min)}$ and $t_{WD1(max)}$ or $t_{WD2(min)}$ and $t_{WD2(max)}$ are not guaranteed to assert or deassert the $\overline{RESET}$. To guarantee that the window watchdog does not assert the $\overline{RESET}$, strobe WDI between $t_{WD1(max)}$ and $t_{WD2(min)}$. The watchdog timer is cleared when $\overline{RESET}$ is asserted or after a falling transition on WDI or after a state change on SET0 or SET1. Disable the watchdog timer by connecting SET0 high and SET1 low.

µP Reset Circuits with Capacitor-Adjustable Reset/Watchdog Timeout Delay

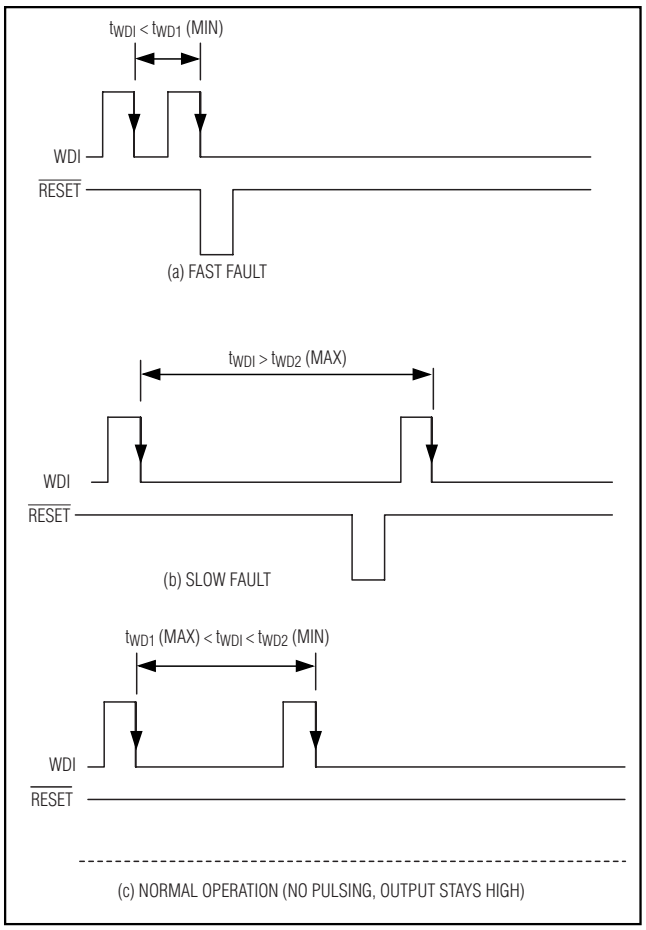


Figure 5. MAX6752/MAX6753 Window Watchdog Diagram

Applications Information

Selecting Reset/Watchdog Timeout Capacitor

The reset timeout period is adjustable to accommodate a variety of µP applications. Adjust the reset timeout period (t_{RP}) by connecting a capacitor (C_{SRT}) between SRT and ground. Calculate the reset timeout capacitor as folllows:

$$C_{SRT} = t_{RP} / (5.06 \times 10^6),$$

with t_{RP} in seconds and C_{SRT} in Farads.

The watchdog timeout period is adjustable to accommodate a variety of µP applications. With this feature, the watchdog timeout can be optimized for software execution. The programmer can determine how often the watchdog timer should be serviced. Adjust the watchdog timeout period (t_{WD}) by connecting a specific value capacitor (C_{SWT}) between SWT and GND. For

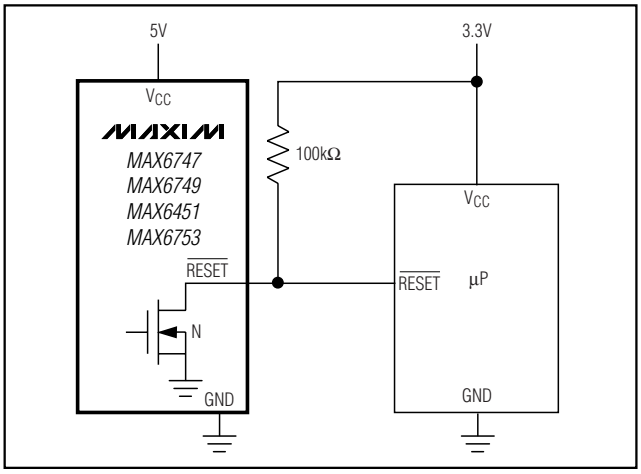


Figure 6. Interfacing to Other Voltage Levels

normal mode operation, calculate the watchdog timeout capacitor as follows:

$$C_{SWT} = t_{WD}/(5.06 \times 10^6),$$

with t_{RP} in seconds and C_{SRT} in Farads.

For the MAX6752 and MAX6753 windowed watchdog function, calculate the slow watchdog period, t_{WD2} as follows:

$$t_{WD2} = 0.65 \times 10^9 \times C_{SWT}$$

C_{SRT} and C_{SWT} must be a low-leakage (<10nA) type capacitor. Ceramic capacitors are recommended.

Transient Immunity

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration supply transients (glitches). The Maximum Transient Duration vs. Reset Threshold Overdrive graph in the *Typical Operating Characteristics* shows this relationship.

The area below the curves of the graph is the region in which these devices typically do not generate a reset pulse. This graph was generated using a falling pulse applied to V_{CC} , starting above the actual reset threshold (V_{TH}) and ending below it by the magnitude indicated (reset-threshold overdrive). As the magnitude of the transient increases (farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts 50µs or less does not cause a reset pulse to be issued.

Interfacing to Other Voltages for Logic Compatibility

The open-drain $\overline{RESET}$ output can be used to interface to a µP with other logic levels. As shown in Figure 6, the open-drain output can be connected to voltages from 0 to 6V.

Generally, the pullup resistor connected to the $\overline{RESET}$ connects to the supply voltage that is being monitored at the IC's V_{CC} pin. However, some systems can use the open-drain output to level-shift from the monitored supply to reset circuitry powered by some other supply. Keep in mind that as the supervisor's V_{CC} decreases towards 1V, so does the IC's ability to sink current at $\overline{RESET}$. Also, with any pullup resistor, $\overline{RESET}$ is pulled high as V_{CC} decays toward zero. The voltage where this occurs depends on the pullup resistor value and the voltage to which it is connected.

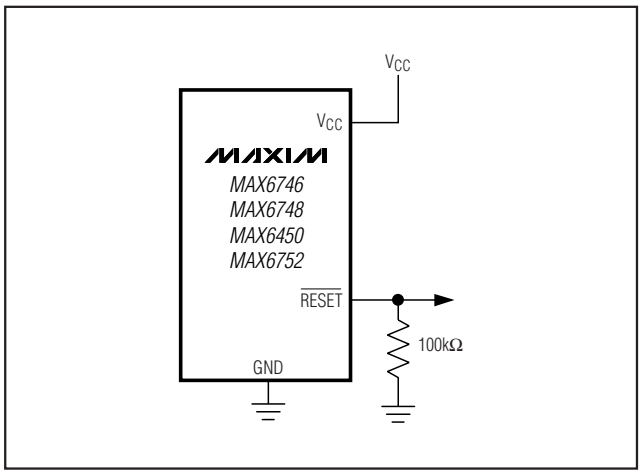


Figure 7. Ensuring RESET Valid to V_{CC} = 0

Ensuring a Valid $\overline{RESET}$ Down to V_{CC} = 0V (Push-Pull $\overline{RESET}$)

When V_{CC} falls below 1V, $\overline{RESET}$ current sinking capabilities decline drastically. The high-impedance CMOS-logic inputs connected to $\overline{RESET}$ can drift to undetermined voltages. This presents no problems in most applications, since most µPs and other circuitry do not operate with V_{CC} below 1V.

In those applications where $\overline{RESET}$ must be valid down to 0V, add a pulldown resistor between $\overline{RESET}$ and GND for the MAX6746/MAX6748/MAX6750/MAX6752 push/pull outputs. The resistor sinks any stray leakage currents, holding $\overline{RESET}$ low (Figure 7). The value of the pulldown resistor is not critical; 100kΩ is large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground. The external pulldown can not be used with the open-drain reset outputs.

µP Reset Circuits with Capacitor-Adjustable Reset/Watchdog Timeout Delay

Table 2. Reset Threshold Voltage Suffix (T_A = 0°C to +85°C)

SUFFIX	MIN	TYP	MAX
50	4.875	5.000	5.125
49	4.778	4.900	5.023
48	4.680	4.800	4.920
47	4.583	4.700	4.818
46	**4.509**	**4.625**	**4.741**
45	4.388	4.500	4.613
44	4.266	4.375	4.484
43	4.193	4.300	4.408
42	4.095	4.200	4.305
41	3.998	4.100	4.203
40	3.900	4.000	4.100
39	3.803	3.900	3.998
38	3.705	3.800	3.895
37	3.608	3.700	3.793
36	3.510	3.600	3.690
35	3.413	3.500	3.588
34	3.315	3.400	3.485
33	3.218	3.300	3.383
32	3.120	3.200	3.280
31	2.998	3.075	3.152
30	2.925	3.000	3.075
29	**2.852**	**2.925**	**2.998**
28	2.730	2.800	2.870
27	2.633	2.700	2.768
26	**2.559**	**2.625**	**2.691**
25	2.438	2.500	2.563
24	2.340	2.400	2.460
23	**2.255**	**2.313**	**2.371**
22	2.133	2.188	2.243
21	2.048	2.100	2.153
20	1.950	2.000	2.050
19	1.853	1.900	1.948
18	1.755	1.800	1.845
17	1.623	1.665	1.707
16	**1.536**	**1.575**	**1.614**

Note: *Standard versions are shown in bold. There is a 2500-piece minimum order increment for standard versions. Sample stock is typically held on standard versions only. Nonstandard versions require a minimum order increment of 10,000 pieces. Contact factory for availability.*

Table 3. Standard Version Table

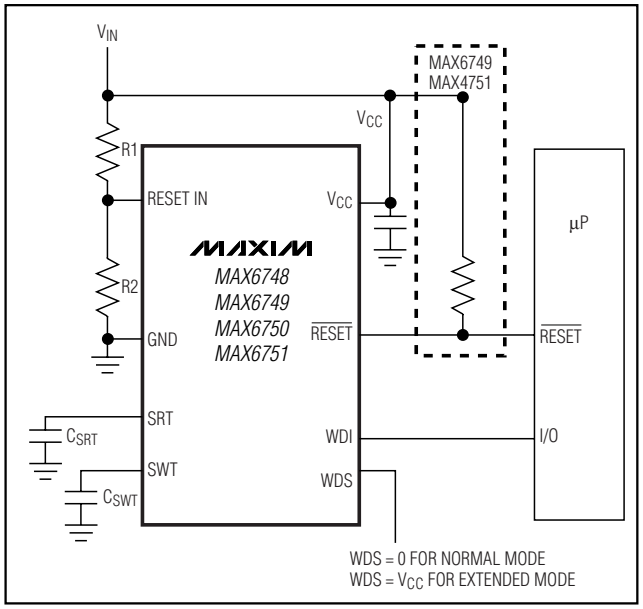
PART	TOP MARK
MAX6746KA16	AEDI
MAX6746KA23	AEDJ
MAX6746KA26	AEDK
MAX6746KA29	AALN
MAX6746KA46	AEDL
MAX6747KA16	AALO
MAX6747KA23	AEDM
MAX6747KA26	AEDN
MAX6747KA29	AEDO
MAX6747KA46	AEDP
MAX6748KA	AALP
MAX6749KA	AALQ
MAX6750KA16	AEDQ
MAX6750KA23	AALR
MAX6750KA26	AEDR
MAX6750KA29	AEDS
MAX6750KA46	AEDT
MAX6751KA16	AEDU
MAX6751KA23	AEDV
MAX6751KA26	AEDW
MAX6751KA29	AEDX
MAX6751KA46	AEDY
MAX6752KA16	AEDZ
MAX6752KA23	AEEA
MAX6752KA26	AALT
MAX6752KA29	AEEB
MAX6752KA46	AEEC
MAX6753KA16	AEED
MAX6753KA23	AEEE
MAX6753KA26	AEEF
MAX6753KA29	AEEG
MAX6753KA46	AEEH

µP Reset Circuits with Capacitor-Adjustable Reset/Watchdog Timeout Delay

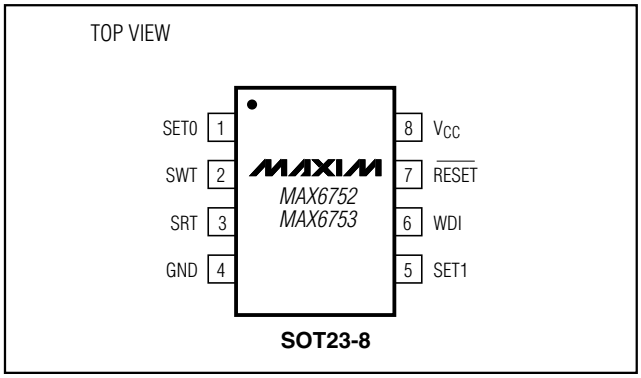
Selector Guide

PART	FIXED V_{CC} RESET THRESHOLD	ADJUSTABLE RESET THRESHOLD	STANDARD WATCHDOG TIMER	MIN/MAX WATCHDOG TIMER	PUSH/ PULL $\overline{\text{RESET}}$	OPEN-DRAIN $\overline{\text{RESET}}$	MANUAL RESET INPUT
MAX6746	*	—	*	—	*	—	*
MAX6747	*	—	*	—	—	*	*
MAX6748	—	*	*	—	*	—	—
MAX6749	—	*	*	—	—	*	—
MAX6750	*	*	*	—	*	—	—
MAX6751	*	*	*	—	—	*	—
MAX6752	*	—	—	*	*	—	—
MAX6753	*	—	—	*	—	*	—

Typical Operating Circuit



Pin Configurations (continued)



SOT23-8

Chip Information

TRANSISTOR COUNT: 1100

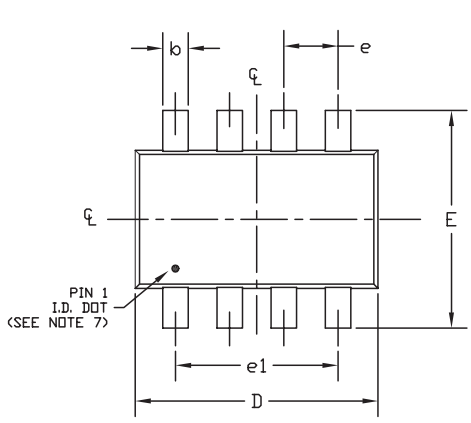
PROCESS: BiCMOS

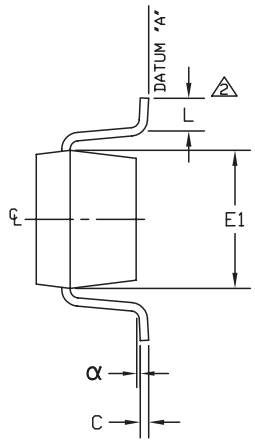
µP Reset Circuits with Capacitor-Adjustable Reset/Watchdog Timeout Delay

Package Information

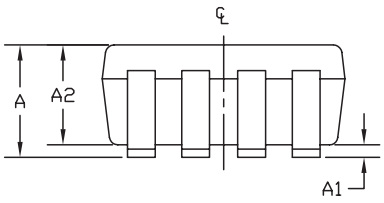
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOT23, 8L.EPS





SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.10	0.60
e	0.65 ref	
e1	1.95 ref	
α	0°	10°



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED REFERENCE TO FLAT FOOT SURFACE PARALLEL TO DATUM "A".
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. EIAJ REF. NUMBER" SC-74 (6 LEAD VERSION)
6. COPLANARITY 4 MILS. MAX.
7. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.
8. MEETS JEDEC MO178.

MAXIM

PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, SOT-23, 8L

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0078	C	1/1