RELIABILITY REPORT

FOR

MAX6338xUB

PLASTIC ENCAPSULATED DEVICES

October 9, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX6338 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX6338 quad voltage monitor is capable of monitoring up to four supplies without any external components. A variety of factory-trimmed threshold voltages and supply tolerances are available to optimize the MAX6338 for specific applications. The selection includes input options for monitoring +5.0V, +3.3V, +3.0V, +2.5V, +1.8V, and -5.0V voltages. An additional high-input impedance comparator option can be used as an adjustable voltage monitor, general-purpose comparator, or digital level translator.

Each of the monitored voltages is available with trip thresholds to support power-supply tolerances of either 5% or 10% below the nominal voltage. An internal bandgap reference ensures accurate trip thresholds across the extended (-40°C to +85°C) operating temperature range.

The MAX6338 consumes 25µA (typ) supply current and operates with supply voltages from +2.5V to +5.5V. An internal undervoltage lockout circuit forces all four digital outputs low when V_{CC} drops below the minimum operating voltage. The four digital outputs all have weak internal pull-ups to V_{CC}, allowing wire-ORed connection. Each input threshold voltage has an independent output.

The MAX6338 is available in a 10-pin µMAX package.

B. Absolute Maximum Ratings

Item	Rating
Terminal Voltage (with repsect to GND)	
Vcc	-0.3V to +6V
Output Voltage	-0.3V to +6V
Input Voltages (IN_) (except –5V)	-0.3V to +6V
Input Voltage (-5V input)	-6V to +0.3V
Continuous Output_current	20mA
Continuous Power Dissipation (T_A = +70^{0}C)	
Operatiing Teperature Range	-40^{0}C to +85^{0}C
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
10 Lead uMax	444mW
Derates above +70°C	
10 Lead uMax	5.6mW/°C

II. Manufacturing Information

A. Description/Function:	1ppm/°C, Low-Noise, +4.096V Voltage Reference
B. Process:	S12 [Standard 1.2 micron silicon gate CMOS]
C. Number of Device Transistors:	620
D. Fabrication Location:	Cailfornia or Oregon, USA
E. Assembly Location:	Philippines or Malaysia
F. Date of Initial Production:	April, 2000

III. Packaging Information

A. Package Type:	**10 Lead uMax**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1601-0109
H. Flammability Rating:	Class UL94-V0

IV. Die Information

A. Dimensions:	39 x 60 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliability Lab Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 234 \times 2}$$

(Chi square value for MTTF upper limit)

→ Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 4.64 \times 10^{-9}$ $\lambda = 4.64$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. 06-5556) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The MS46Z die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX6338xUB

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	234	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	740	`
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Small Outline package.
Note 2: Generic Package/Process Data

Attachment #3

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

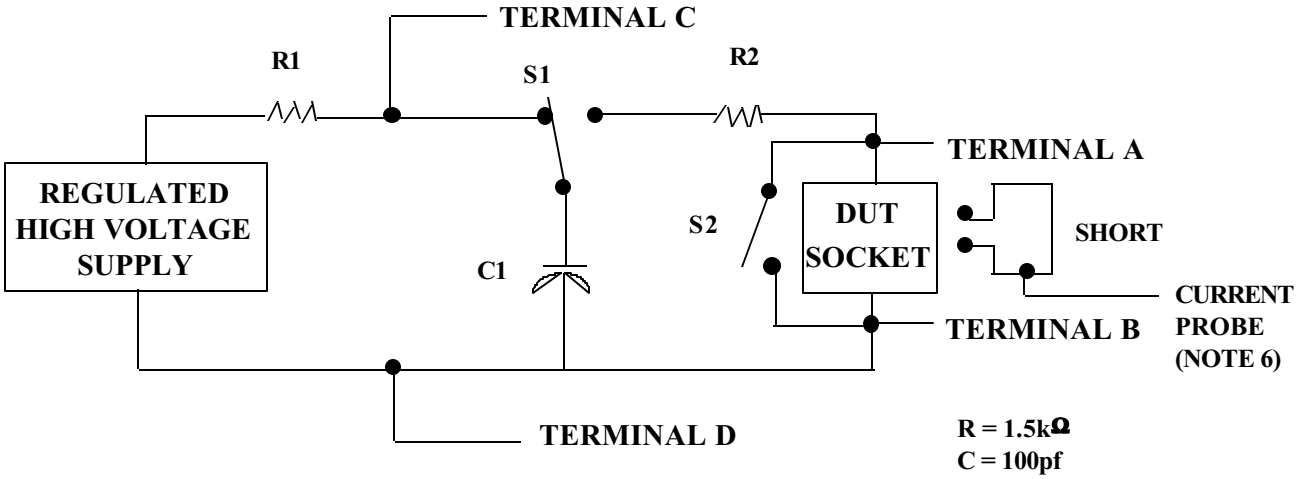
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

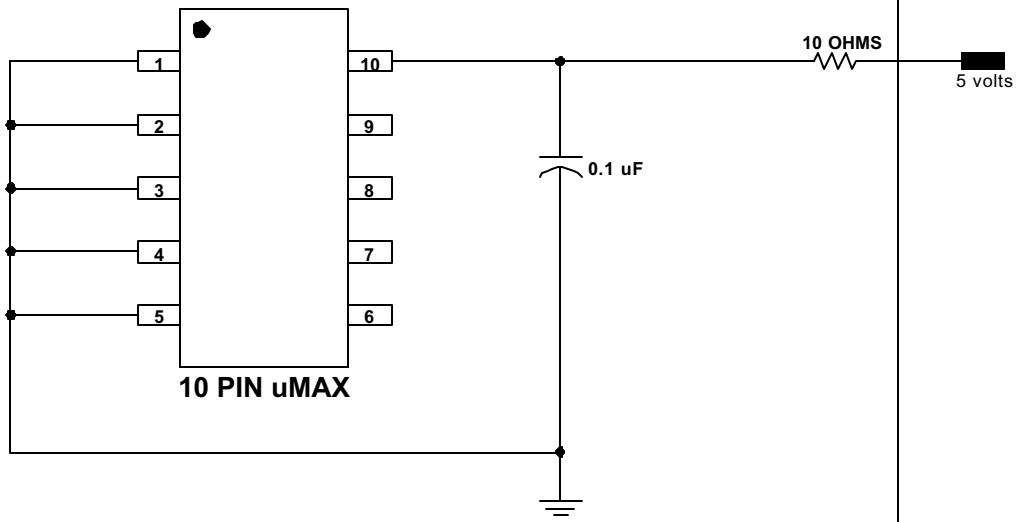
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



ONCE PER SOCKET

ONCE PER BOARD

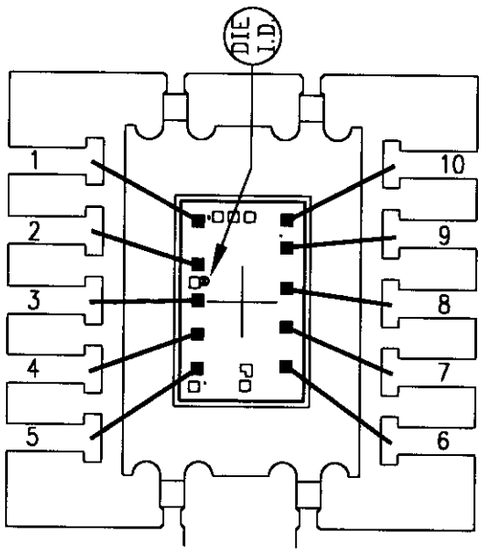


DEVICES: MAX6338/6709/6714

MAX. EXPECTED CURRENT = 60uA

DRAWN BY: TEK TAN

NOTES:



PKG. CODE: U10-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 68X94	PKG.		12/22/99	BOND DIAGRAM #: 05-1601-0109	REV: A
	DESIGN		10/23/99		