19-1838; Rev 1; 1/01

MAXIM

µP Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset

General Description

The MAX6323/MAX6324 microprocessor (µP) supervisory circuits monitor power supplies and µP activity in digital systems. A watchdog timer looks for activity outside an expected window of operation. Six laser-trimmed reset thresholds are available with ±2.5% accuracy from +2.32V to +4.63V. Valid $\overline{RESET}$ output is guaranteed down to V_{CC} = +1.2V.

The $\overline{RESET}$ output is either push-pull (MAX6323) or open-drain (MAX6324). $\overline{RESET}$ is asserted low when V_{CC} falls below the reset threshold, or when the manual reset input ($\overline{MR}$) is asserted low. $\overline{RESET}$ remains asserted for at least 100ms after V_{CC} rises above the reset threshold or $\overline{MR}$ is deasserted.

The watchdog pulse output ($\overline{WDPO}$) utilizes an open-drain configuration. It can be triggered either by a fast timeout fault (watchdog input pulses are too close to each other) or a slow timeout fault (no watchdog input pulse is observed within the timeout period). The watchdog timeout is measured from the last falling edge of watchdog input (WDI) with a minimum pulse width of 300ns. $\overline{WDPO}$ is asserted for 1ms when a fault is observed. Eight laser-trimmed timeout periods are available.

The MAX6323/MAX6324 are offered in a 6-pin SOT23 package and operate over the extended temperature range (-40°C to +125°C).

Applications

Automotive

Industrial

Medical

Embedded Control Systems

Features

- **Min/Max (Windowed) Watchdog, 8 Factory-Trimmed Timing Options**
- **Pulsed Open-Drain, Active-Low Watchdog Output**
- **Power-On Reset**
- **Precision Monitoring of +2.5V, +3.0V, +3.3V, and +5.0V Power Supplies**
- **Open-Drain or Push-Pull $\overline{RESET}$ Outputs**
- **Low-Power Operation (23µA typ)**
- **Debounced Manual Reset Input**
- **Guaranteed Reset Valid to V_{CC} = +1.2V**

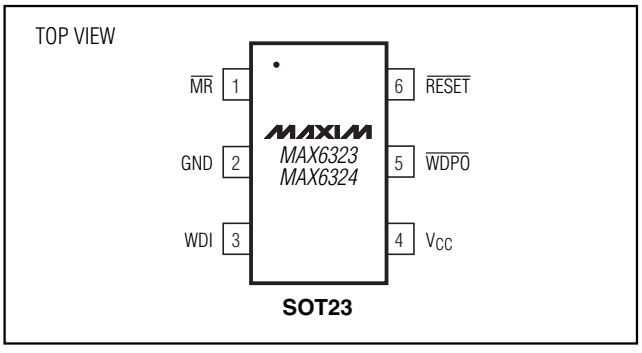
Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE	RESET OUTPUT
MAX6323_UT__-T	-40°C to +125°C	6 SOT23-6	Push-Pull
MAX6324_UT__-T	-40°C to +125°C	6 SOT23-6	Open Drain

**These devices are factory trimmed to one of eight watchdog-timeout windows and one of six reset voltage thresholds. Insert the letter corresponding to the desired watchdog-timeout window (A, B, C, D, E, F, G, or H) into the blank following the number 6323 or 6324 (see Watchdog Timeout table). Insert the two-digit code (46, 44, 31, 29, 26, or 23) after the letters UT for the desired nominal reset threshold (see Reset Threshold Range table at end of data sheet).*

***Note:** There are eight standard versions of each device available (see Standard Versions table). Sample stock is generally held on standard versions only. Standard versions have an order increment requirement of 2500 pieces. Nonstandard versions have an order increment requirement of 10,000 pieces. Contact factory for availability of nonstandard versions.*

Pin Configuration



Typical Operating Circuit appears at end of data sheet.

Watchdog Timeout

SUFFIX	WATCHDOG TIMEOUT*			
	FAST		SLOW	
	MAX	UNITS	MIN	UNITS
A	1.5	ms	10	ms
B	15	ms	100	
C	15	ms	300	
D	15	ms	10	s
E	15	ms	60	
F	23	ms	47	ms
G	39	ms	82	
H	719	ms	1.3	s

**See Figure 1 for operation.*

µP Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} .....-0.3V to +6.0V
- $\overline{MR}$, $\overline{RESET}$ (MAX6323), WDI .....-0.3V to (V_{CC} + +0.3V)
- $\overline{WDPO}$, $\overline{RESET}$ (MAX6324).....-0.3V to +6.0V

Input Current, V_{CC}, WDI, $\overline{MR}$.....20mA
Output Current, $\overline{RESET}$, $\overline{WDPO}$ 20mA
Rate of Rise, V_{CC} 100V/µs

Continuous Power Dissipation (T_A = +70°C)
- 6-Pin SOT23 (derate 8.7mW/°C above +70°C).....696mW

Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = full range, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = 3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}			1.2		5.5	V
Supply Current	I_{CC}	No load, $\overline{RESET}$ deasserted	V_{CC} = 2.5V or 3.3V		23	45	µA
			V_{CC} = 5.5V		27	57	
Reset Threshold Voltage	V_{TH}	MAX632_ _UT46		4.50	4.63	4.75	V
		MAX632_ _UT44		4.25	4.38	4.50	
		MAX632_ _UT31		3.00	3.08	3.15	
		MAX632_ _UT29		2.85	2.93	3.00	
		MAX632_ _UT26		2.55	2.63	2.70	
		MAX632_ _UT23		2.25	2.32	2.38	
Reset Timeout Delay	t_{RP}	$\overline{RESET}$ deasserted		100	180	280	ms
V_{CC} to $\overline{RESET}$ Delay		10mV/ms, V_{TH} +100mV to V_{TH} -100mV			20		µs
$\overline{WDPO}$, $\overline{RESET}$ Output Voltage	V_{OL}	I_{SINK} = 1.2mA, V_{CC} = 2.25V (MAX632_ _UT23, MAX632_ _UT26, MAX632_ _UT29, MAX632_ _UT31)				0.4	V
		I_{SINK} = 3.2mA, V_{CC} = 4.25V (MAX632_ _UT44, MAX632_ _UT46)				0.4	
		I_{SINK} = 100µA, V_{CC} > 1.2V, $\overline{RESET}$ asserted				0.4	
$\overline{RESET}$ Output Voltage (MAX6323)	V_{OH}	I_{SOURCE} = 500µA, V_{CC} = 3.15V, $\overline{RESET}$ deasserted (MAX632_ _UT23, MAX632_ _UT26, MAX632_ _UT29, MAX632_ _UT31)		0.8 x V_{CC}			V
		I_{SOURCE} = 800µA, V_{CC} = 4.75V, $\overline{RESET}$ deasserted, (MAX632_ _UT44, MAX632_ _UT46)		V_{CC} - 1.5			
$\overline{WDPO}$, $\overline{RESET}$ Output Leakage	I_{LKG}	$V_{\overline{RESET}}$ = $V_{\overline{WDPO}}$ = +5.5V, $\overline{RESET}$, $\overline{WDPO}$ deasserted				1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = full range, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = 3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WATCHDOG INPUT AND OUTPUT						
Watchdog Timeout (Fast) (Notes 2, 3)	t_{WD1}	MAX632_AUT_ _	1		1.5	ms
		MAX632_BUT_ _	10		15	
		MAX632_CUT_ _	10		15	
		MAX632_DUT_ _	10		15	
		MAX632_EUT_ _	10		15	
		MAX632_FUT_ _	17		23	
		MAX632_GUT_ _	29		39	
		MAX632_HUT_ _	543		719	
Watchdog Timeout (Slow) (Note 4)	t_{WD2}	MAX632_AUT_ _	10		15	ms
		MAX632_BUT_ _	100		150	
		MAX632_CUT_ _	300		450	
		MAX632_DUT_ _	10		15	s
		MAX632_EUT_ _	60		90	
		MAX632_FUT_ _	47		63	ms
		MAX632_GUT_ _	82		108	
		MAX632_HUT_ _	1.3		1.8	s
Minimum Watchdog Input Pulse Width			300			ns
WDI Glitch Immunity		V_{CC} = 5.5V		100		ns
WDI Input Voltage	V_{IH}		0.75 x V_{CC}			V
	V_{IL}				0.8	
WDI Input Current		WDI = 0	-1.5	-1		µA
		WDI = V_{CC}		1	1.5	
$\overline{WDPO}$ Pulse Width		V_{IL} = 0.8V, V_{IH} = 0.75V x V_{CC}	0.5	1	3	ms
MANUAL RESET INPUT						
$\overline{MR}$ Input Voltage	V_{IH}		0.7 x V_{CC}			V
	V_{IL}				0.3 x V_{CC}	
$\overline{MR}$ Minimum Pulse Width			1			µs
$\overline{MR}$ Glitch Immunity		V_{CC} = 2.5V		100		ns
$\overline{MR}$ to Reset Delay		V_{CC} = 2.5V		120		ns
$\overline{MR}$ Pullup Resistance			50	85		kΩ

Note 1: Devices are tested at T_A = +25°C and guaranteed by design for T_A = T_{MIN} to T_{MAX}, as specified.

Note 2: $\overline{WDPO}$ will pulse low if a falling edge is detected on WDI before this timeout period expires.

Note 3: To avoid a potential fake fault, the first WDI pulse after the rising edge of $\overline{RESET}$ or $\overline{WDPO}$ will not create a fast watchdog timeout fault.

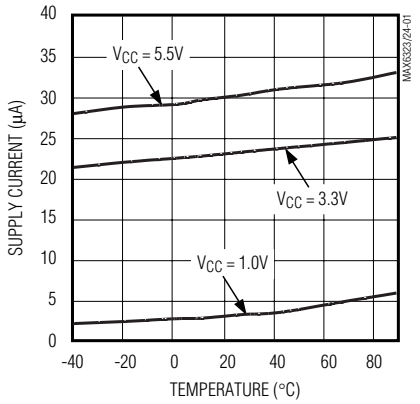
Note 4: $\overline{WDPO}$ will pulse low if no falling edge is detected on WDI after this timeout period expires.

µP Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset

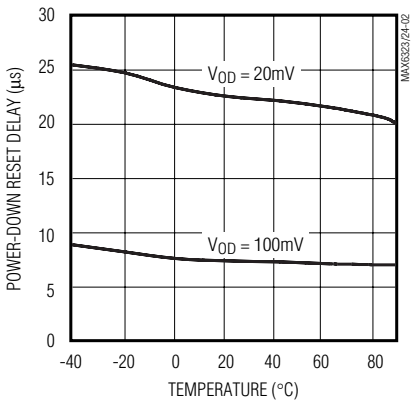
Typical Operating Characteristics

(V_{CC} = full range, T_A = +25°C, unless otherwise noted.)

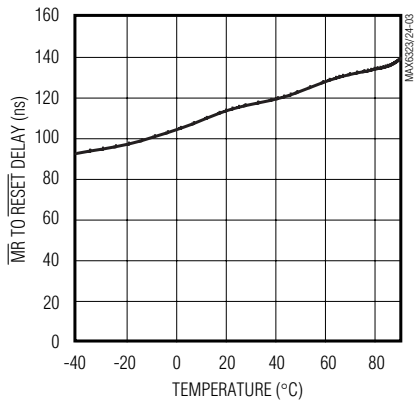
SUPPLY CURRENT vs. TEMPERATURE



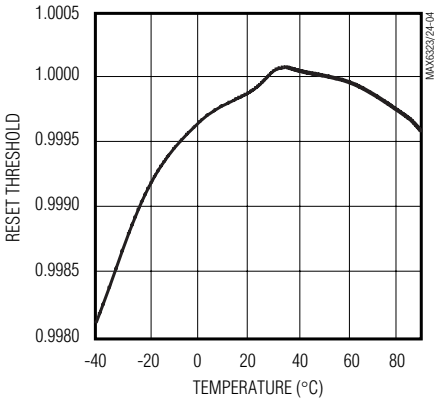
POWER-DOWN RESET DELAY vs. TEMPERATURE



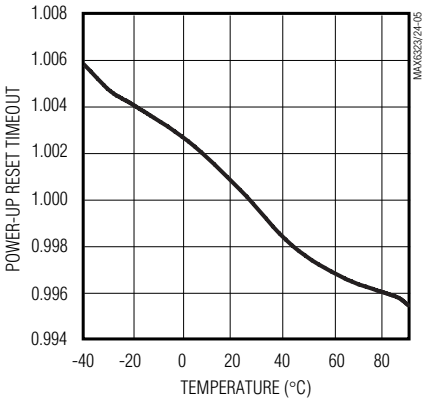
$\overline{MR}$ TO $\overline{RESET}$ DELAY vs. TEMPERATURE



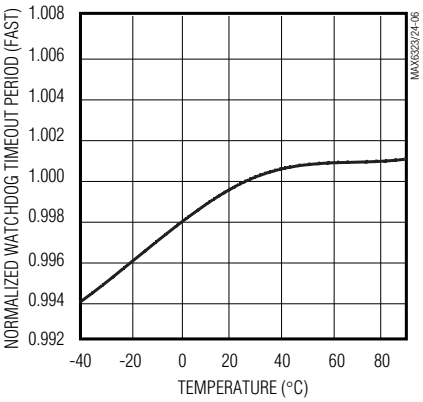
NORMALIZED RESET THRESHOLD vs. TEMPERATURE



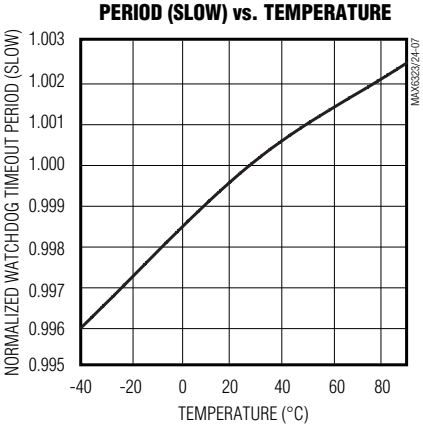
NORMALIZED POWER-UP RESET TIMEOUT vs. TEMPERATURE



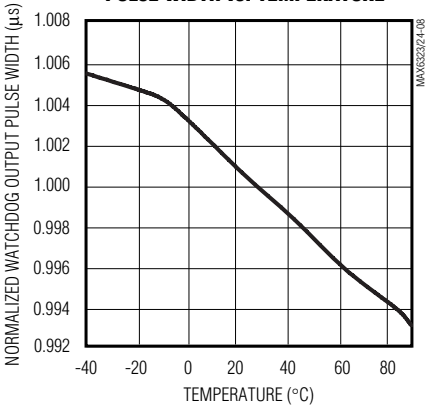
NORMALIZED WATCHDOG TIMEOUT PERIOD (FAST) vs. TEMPERATURE



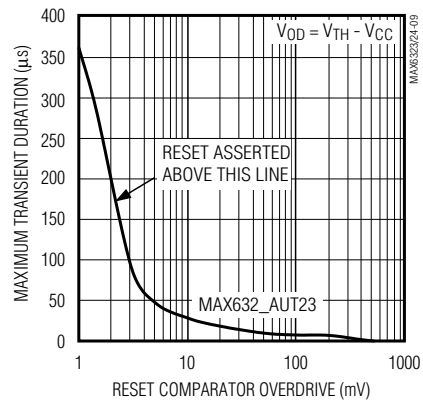
NORMALIZED WATCHDOG TIMEOUT PERIOD (SLOW) vs. TEMPERATURE



NORMALIZED WATCHDOG OUTPUT PULSE WIDTH vs. TEMPERATURE



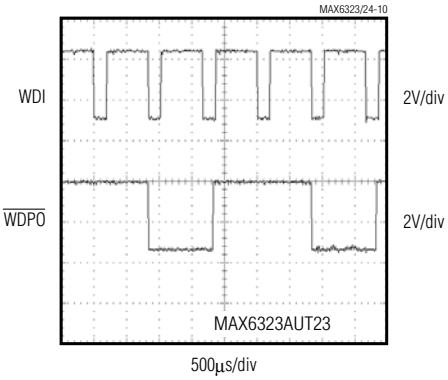
MAXIMUM TRANSIENT DURATION vs. RESET THRESHOLD OVERDRIVE



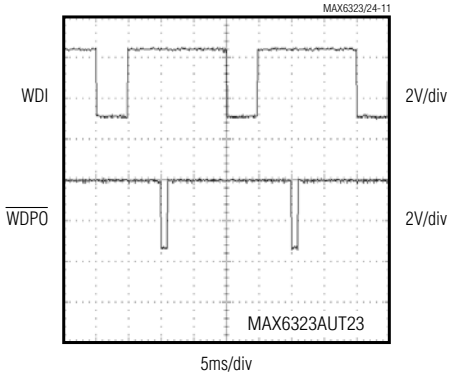
Typical Operating Characteristics (continued)

(V_{CC} = full range, T_A = +25°C, unless otherwise noted.)

FAST WATCHDOG TIMEOUT PERIOD



SLOW WATCHDOG TIMEOUT PERIOD



Pin Description

PIN	NAME	FUNCTION
1	$\overline{MR}$	Active-Low, Manual Reset Input. When $\overline{MR}$ is asserted low, $\overline{RESET}$ is asserted low, the internal watchdog timer is reset to zero, and $\overline{WDPO}$ is reset to high impedance (open drain). After the rising edge of $\overline{MR}$, $\overline{RESET}$ is asserted for at least 100ms. Leave $\overline{MR}$ unconnected or connect to V_{CC} if unused.
2	GND	Ground
3	WDI	Watchdog Input. The internal watchdog timer is reset to zero and begins to count at the falling edge of WDI if $\overline{RESET}$ is high. If WDI sees another falling edge within the factory-trimmed watchdog window, $\overline{WDPO}$ will remain unasserted. Transitions outside this window, either faster or slower, will cause $\overline{WDPO}$ to pulse low for 1ms (typ).
4	V_{CC}	Supply Voltage for the Device. Input for V_{CC} reset monitor. For noisy systems, bypass V_{CC} with a 500pF (min) capacitor.
5	$\overline{WDPO}$	Watchdog Pulse Output. The open-drain $\overline{WDPO}$ output is pulsed low for 1ms (typ) upon detection of a fast or slow watchdog fault. $\overline{WDPO}$ is only active when $\overline{RESET}$ is high.
6	$\overline{RESET}$	Active-Low. Reset is asserted when V_{CC} drops below V_{TH} and remains asserted until V_{CC} rises above V_{TH} for the duration of the reset timeout period. The MAX6323 has a push-pull output and the MAX6324 has an open-drain output. Connect a pullup resistor from $\overline{RESET}$ to any supply voltage up to +6V.

µP Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset

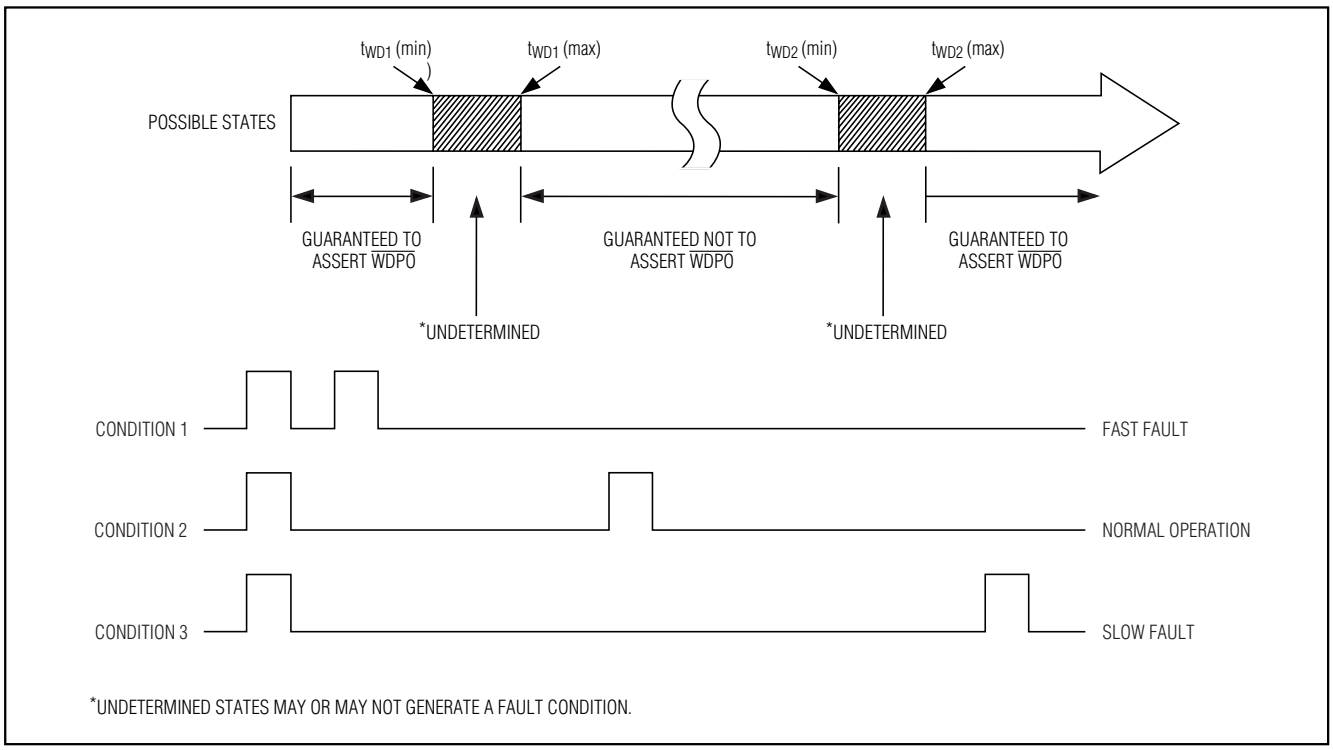


Figure 1. Detailed Watchdog Input Timing Relationship

Detailed Description

The MAX6323/MAX6324 µP supervisory circuits maintain system integrity by alerting the µP to fault conditions. In addition to a standard V_{CC} monitor (for power-on reset, brownout detect, and power-down reset), the devices include a sophisticated watchdog timer that detects when the processor is running outside an expected window of operation for a specific application. The watchdog signals a fault when the input pulses arrive too early (faster than the selected t_{WD1} timeout period) or too late (slower than the selected t_{WD2} timeout period) (Figure 1). Incorrect timing can lead to poor or dangerous system performance in tightly controlled operating environments. Incorrect timing could be the result of improper µP clocking or code execution errors. If a timing error occurs, the MAX6323/MAX6324 issue a watchdog pulse output, independent from the reset output, indicating that system maintenance may be required.

Watchdog Function

A pulse on the watchdog output $\overline{WDPO}$ can be triggered by a fast fault or a slow fault. If the watchdog input (WDI) has two falling edges too close to each other (faster than t_{WD1}) (Figure 2) or falling edges that are too far apart (slower than t_{WD2}) (Figure 3), $\overline{WDPO}$ is pulsed low. Normal watchdog operation is displayed in Figure 4 ($\overline{WDPO}$ is not asserted). The internal watchdog timer is cleared when a WDI falling edge is detected within the valid watchdog window or when the device's $\overline{RESET}$ or $\overline{WDPO}$ outputs are deasserted. All WDI input pulses are ignored while either $\overline{RESET}$ or $\overline{WDPO}$ is asserted. Figure 1 identifies the input timing regions where $\overline{WDPO}$ fault outputs will be observed with respect to t_{WD1} and t_{WD2}. After $\overline{RESET}$ or $\overline{WDPO}$ deasserts, the first WDI falling edge is ignored for the fast fault condition (Figure 2).

Upon detecting a watchdog fault, the $\overline{WDPO}$ output will pulse low for 1ms. $\overline{WDPO}$ is an open-drain output. Connect a pullup resistor on $\overline{WDPO}$ to any supply up to +6V.

V_{CC} Reset

The MAX6323/MAX6324 also include a standard V_{CC} reset monitor to ensure that the µP is started in a known state and to prevent code execution errors during power-up, power-down, or brownout conditions. $\overline{RESET}$ is asserted whenever the V_{CC} supply voltage

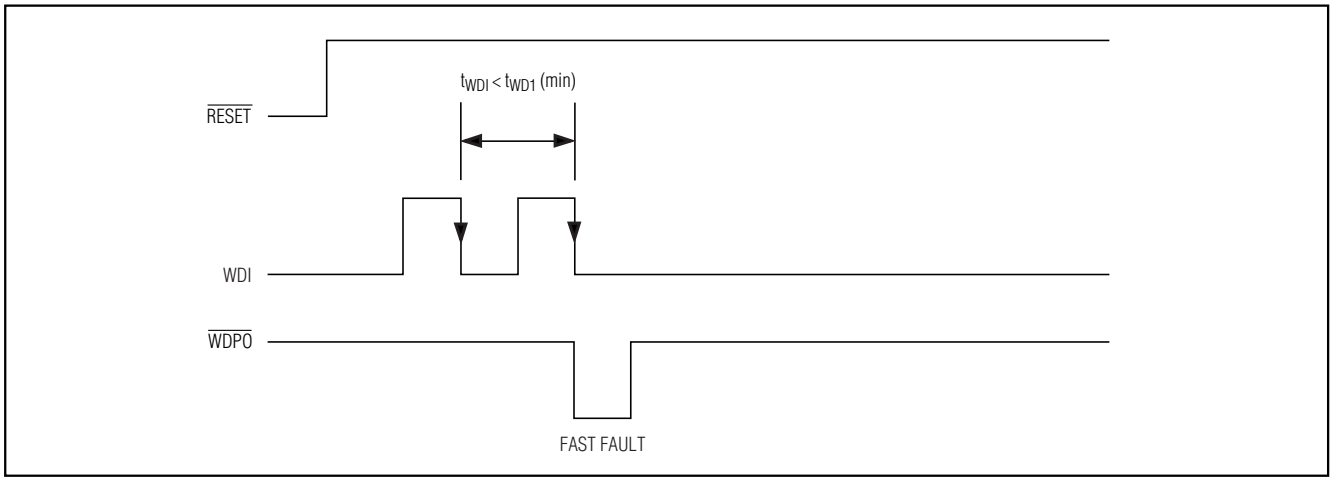


Figure 2. Fast Fault Timing

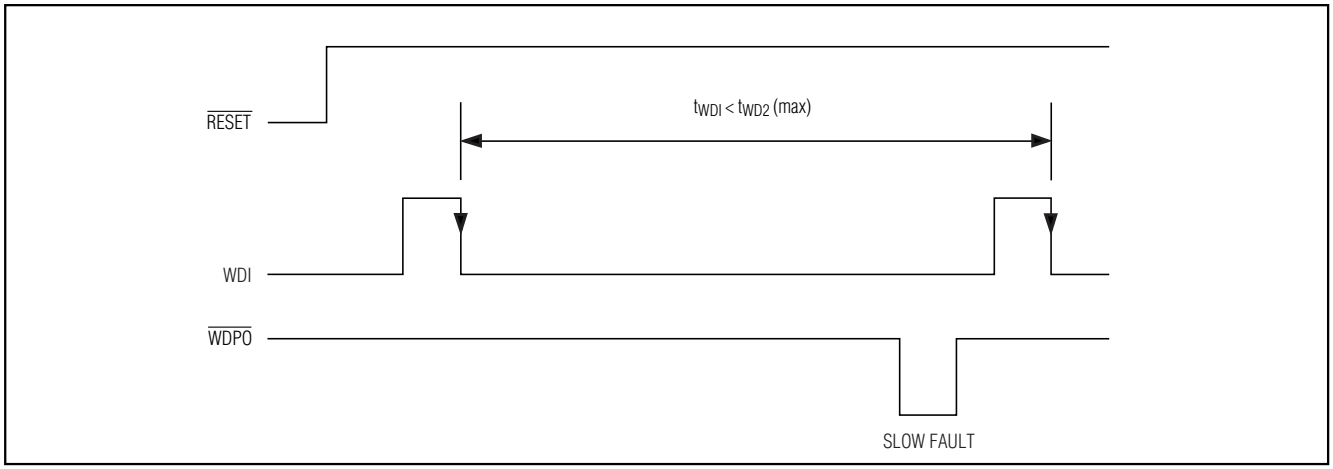


Figure 3. Slow Fault Timing

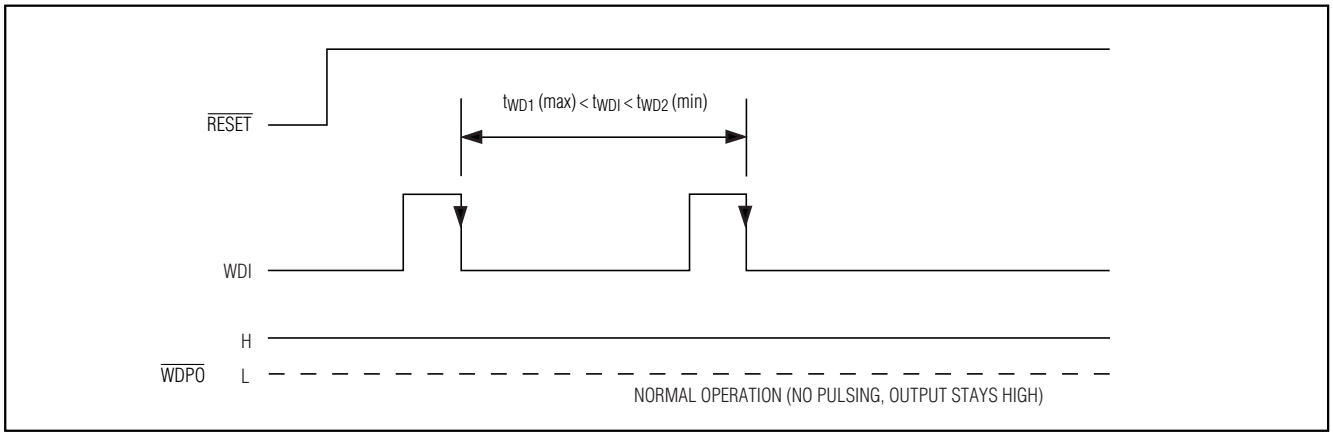


Figure 4. Normal Operation, $\overline{WDPO}$ Not Asserted

µP Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset

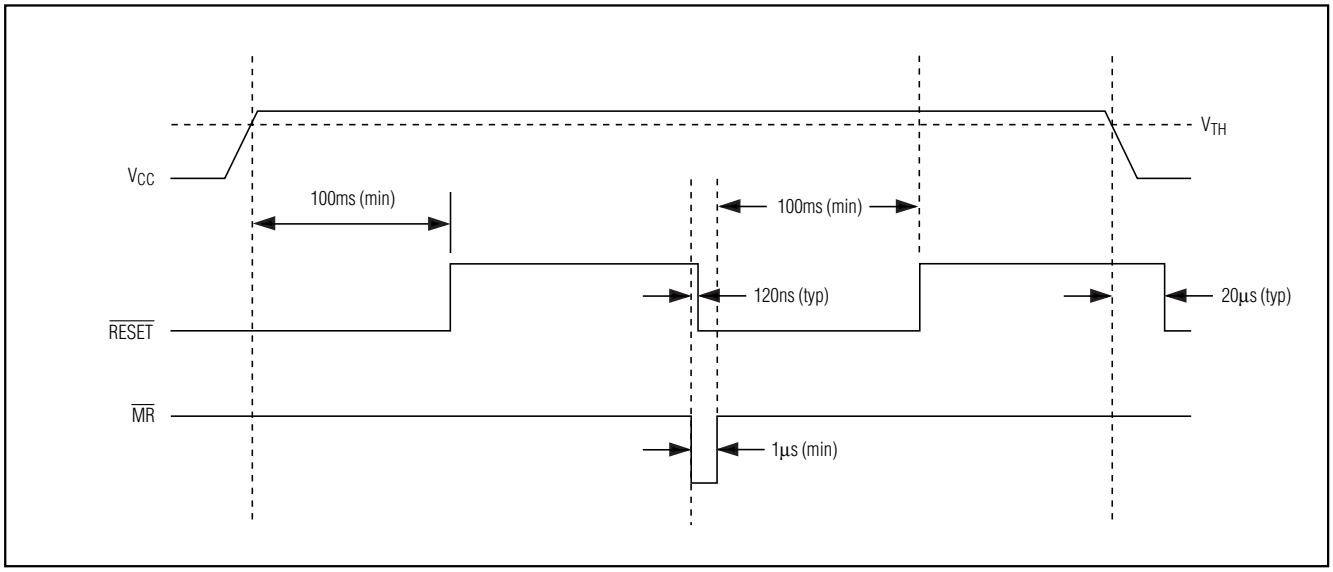


Figure 5. $\overline{RESET}$ Timing Relationship

falls below the preset threshold or when the manual reset input ($\overline{MR}$) is asserted. The $\overline{RESET}$ output remains asserted for at least 100ms after V_{CC} has risen above the reset threshold and $\overline{MR}$ is deasserted (Figure 5). For noisy environments, bybass V_{CC} with a 500pF (min) capacitor to ensure correct operation.

The MAX6323 has a push-pull output stage, and the MAX6324 utilizes an open-drain output. Connect a pull-up resistor on the $\overline{RESET}$ output of the MAX6324 to any supply up to +6V. Select a resistor value large enough to register a logic low (see *Electrical Characteristics*) and small enough to register a logic high while supplying all input leakage currents and leakage paths connected to the $\overline{RESET}$ line. A 10kΩ pullup is sufficient in most applications.

Manual Reset Input

Many µP-based products require manual reset capability to allow an operator or external logic circuitry to initiate a reset. The manual reset input ($\overline{MR}$) can connect directly to a switch without an external pullup resistor or debouncing network. $\overline{MR}$ is internally pulled up to V_{CC} and, therefore, can be left unconnected if unused. $\overline{MR}$ is designed to reject fast, negative-going transients (typically 100ns pulses), and it must be held low for a minimum of 1µs to assert the reset output (Figure 5). A 0.1µF capacitor from $\overline{MR}$ to ground provides additional noise immunity. After $\overline{MR}$ transitions from low to high, reset will remain asserted for the duration of the reset timeout period, at least 100ms.

Applications Information

Negative-Going V_{CC} Transients

The MAX6323/MAX6324 are relatively immune to short-duration negative-going V_{CC} transients (glitches), which usually do not require the entire system to shut down. Typically, 200ns large-amplitude pulses (from ground to V_{CC}) on the supply will not cause a reset. Lower amplitude pulses result in greater immunity. Typically, a V_{CC} transient that falls 100mV below the reset threshold and lasts less than 20µs will not trigger a reset (see *Typical Operating Characteristics*). An optional 0.1µF bypass capacitor mounted close to V_{CC} provides additional transient immunity.

Ensuring a Valid Reset Output Down to V_{CC} = 0

When V_{CC} falls below +1.2V, the MAX6323 $\overline{RESET}$ output no longer sinks current; it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to $\overline{RESET}$ can drift to undetermined voltages. This does not present a problem in most applications, since most µPs and other circuitry are inoperative with V_{CC} below +1.2V. However, in applications where $\overline{RESET}$ must be valid down to 0, adding a pulldown resistor to $\overline{RESET}$ causes any stray leakage currents to flow to ground, holding $\overline{RESET}$ low (Figure 6). R1's value is not critical; 100kΩ is large enough not to load $\overline{RESET}$ and small enough to pull $\overline{RESET}$ to ground. This scheme does not work with the open-drain output of the MAX6324.

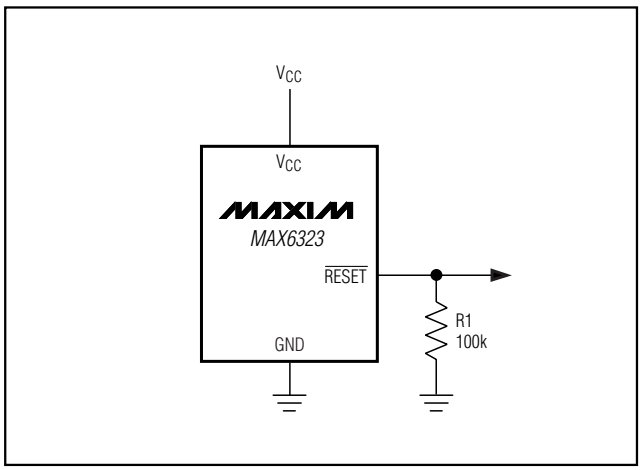


Figure 6. $\overline{RESET}$ Valid to V_{CC} = Ground Circuit

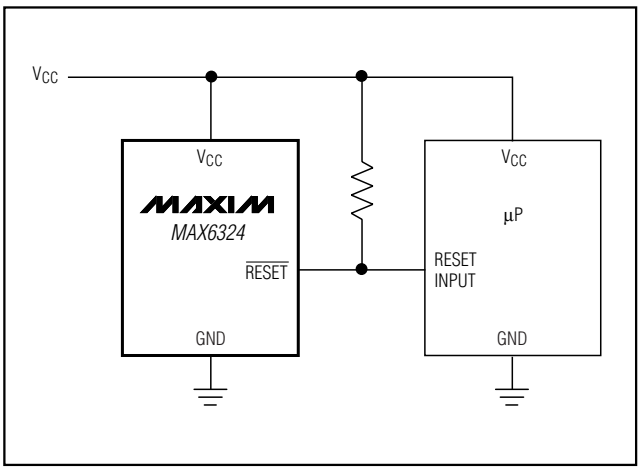


Figure 7. Interfacing to µPs with Bidirectional Reset Pins

Interfacing to µPs with Bidirectional Reset Pins

Since the $\overline{RESET}$ output on the MAX6324 is open-drain, this device easily interfaces with µPs that have bidirectional reset pins, such as the Motorola 68HC11. Connecting the µP supervisor's $\overline{RESET}$ output directly to the microcontroller's (µC's) $\overline{RESET}$ pin with a single pullup resistor allows either device to assert reset (Figure 7).

MAX6324 Open-Drain $\overline{RESET}$ Output Allows Use with Multiple Supplies

Generally, the pullup resistor connected to the MAX6324 will connect to the supply voltage that is being monitored at the IC's V_{CC} pin. However, some systems may use the open-drain output to level-shift from the monitored supply to reset circuitry powered by some other supply (Figure 8). Keep in mind that as the MAX6324's V_{CC} decreases below +1.2V, so does the IC's ability to sink current at $\overline{RESET}$. Also, with any pullup resistor, $\overline{RESET}$ will be pulled high as V_{CC} decays toward 0. The voltage where this occurs depends on the pullup resistor value and the voltage to which it is connected.

Watchdog Software Considerations

To help the watchdog timer monitor software execution more closely, set and reset the watchdog input at different points in the program, rather than "pulsing" the watchdog input high-low-high or low-high-low. This technique avoids a "stuck" loop in which the watchdog time would continue to be reset within the loop, keeping the watchdog from timing out.

Figure 9 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should "hang" in any subroutine, the problem would be quickly corrected, since the I/O is continually set low and the watchdog time is allowed to time out, causing a reset or interrupt to be issued.

$\overline{WDPO}$ to $\overline{MR}$ Loopback

An error detected by the watchdog often indicates that a problem has occurred in the µP code execution. This could be a stalled instruction or a loop from which the processor cannot free itself. If the µP will still respond to a nonmaskable input (NMI), the processor can be redirected to the proper code sequence by connecting the $\overline{WDPO}$ output to an NMI input. Internal RAM data should not be lost, but it may have been contaminated by the same error that caused the watchdog to time out.

If the processor will not recognize NMI inputs, or if the internal data is considered potentially corrupted when a watchdog error occurs, the processor should be restarted with a reset function. To obtain proper reset timing characteristics, the $\overline{WDPO}$ output should be connected to the $\overline{MR}$ input, and the $\overline{RESET}$ output should

µP Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset

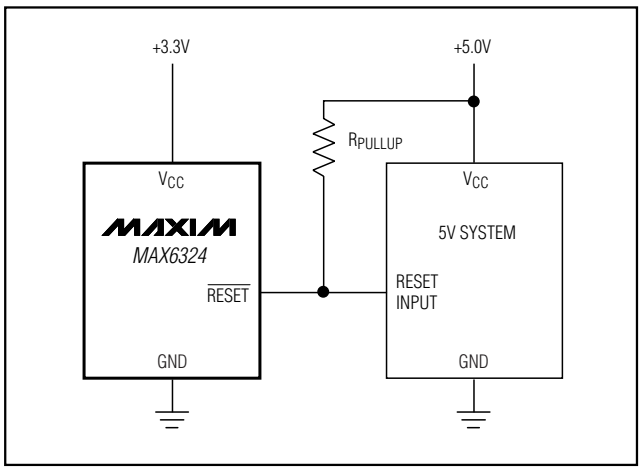


Figure 8. MAX6324 Open-Drain $\overline{RESET}$ Output Allows Use with Multiple Supplies

drive the µP $\overline{RESET}$ input (Figure 10). The short 1ms $\overline{WDPO}$ pulse output will assert the manual reset input and force the $\overline{RESET}$ output to assert for the full reset timeout period (100ms min). All internal RAM data is lost during the reset period, but the processor is guaranteed to begin in the proper operating state.

Standard Versions

MAX6323AUT29	MAX6324AUT29
MAX6323AUT46	MAX6324AUT46
MAX6323CUT29	MAX6324BUT29
MAX6323CUT46	MAX6324BUT46
MAX6323DUT29	MAX6324EUT29
MAX6323DUT46	MAX6324EUT46
MAX6323HUT29	MAX6324HUT29
MAX6323HUT46	MAX6324HUT46

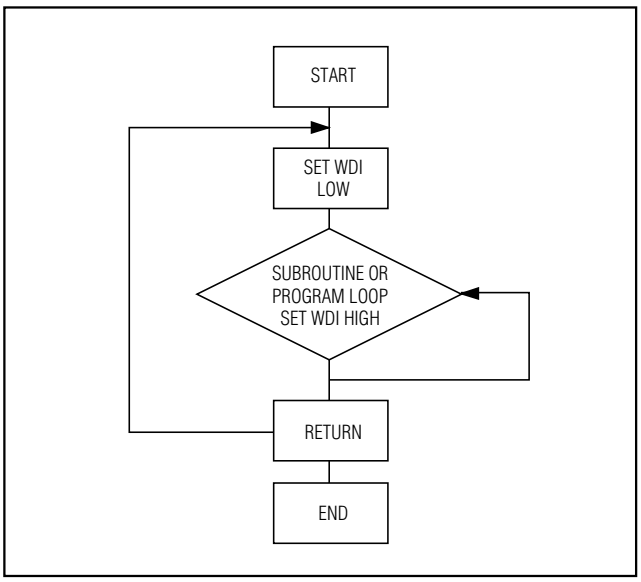


Figure 9. Watchdog Flow Diagram

Reset Threshold Range (-40°C to +125°C)

SUFFIX	MIN	TYP	MAX	UNITS
46	4.50	4.63	4.75	V
44	4.25	4.38	4.50	
31	3.00	3.08	3.15	
29	2.85	2.93	3.00	
26	2.55	2.63	2.70	
23	2.25	2.32	2.38	

Chip Information

TRANSISTOR COUNT: 1371

PROCESS: BiCMOS

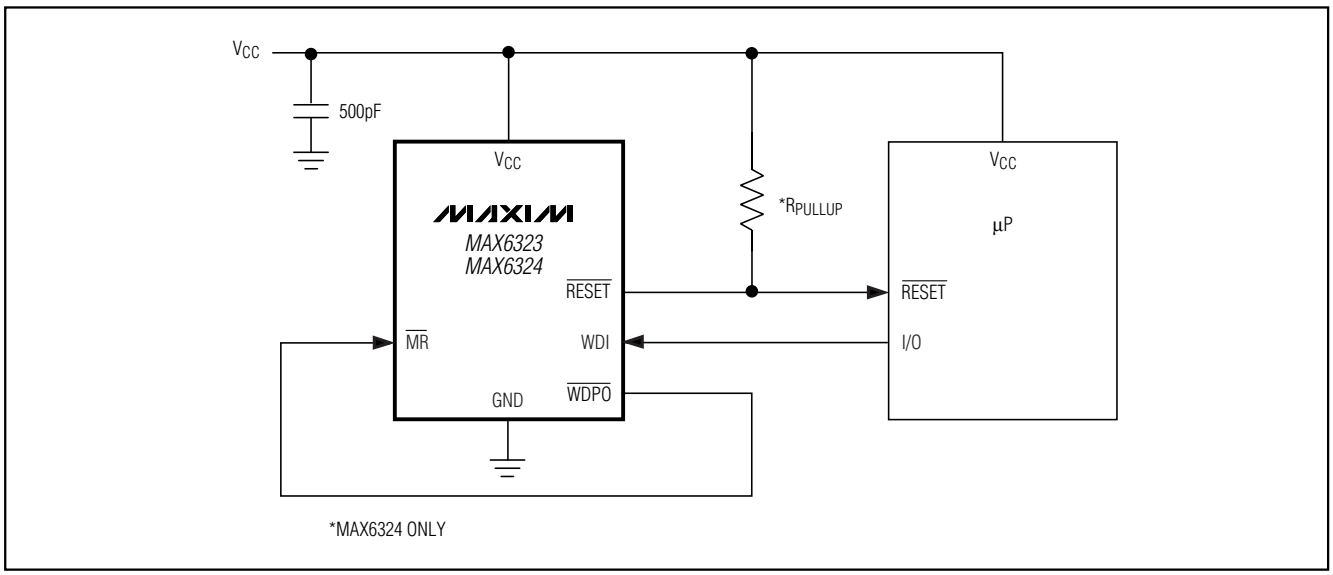
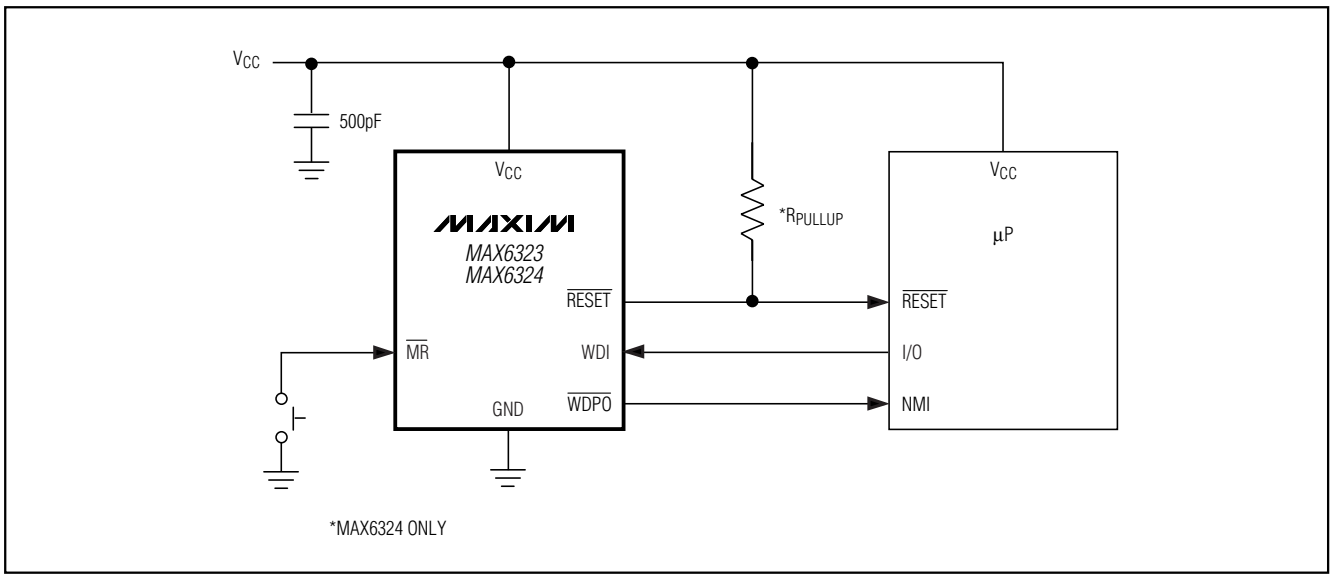


Figure 10. $\overline{WDPO}$ to $\overline{MR}$ Loopback Circuit

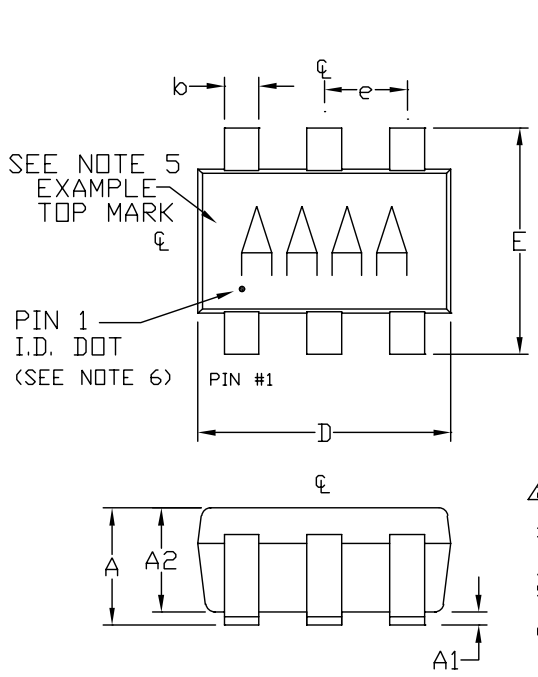
Typical Operating Circuit

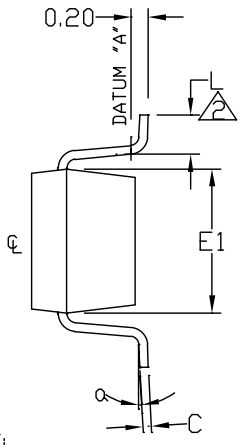


µP Supervisory Circuits with Windowed (Min/Max) Watchdog and Manual Reset

Package Information

6LSOT.EPS





SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
α	0°	10°

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.

MAXIM
PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, SOT23, 6L

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0058	D	1/1