

RELIABILITY REPORT
FOR
MAX6220ASA50
PLASTIC ENCAPSULATED DEVICES

January 27, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

A handwritten signature in black ink, appearing to read "J Pedicord".

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

A handwritten signature in black ink, appearing to read "Bryan J. Preeshl".

Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX6220 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX6220 is a low-noise, precision voltage reference with extremely low 20ppm/°C temperature coefficient over the automotive temperature range (-40°C to +125°C) and excellent ±0.1% initial accuracy. This device features buried-zener technology for low noise performance. The load-regulation specification is guaranteed for source and sink currents up to 15mA. Excellent line and load regulation and low output impedance at high frequency make the MAX6220 ideal for high-resolution data-conversion systems up to 16 bits. The MAX6220 is set for 2.5V, 4.096V, and 5.0V outputs.

B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
IN to Gnd	-0.3V to +42V
OUT, TRIM to Gnd	-0.3V to +12V
NR to GND	-0.3V to +6V
OUT Short Circuit to GND Duration (VIN ≤ 12V)	Continuous
OUT Short Circuit to GND Duration (VIN ≤ 42V)	5s
OUT Short Circuit to IN Duration (VIN ≤ 12V)	Continuous
Operating Temp Range	-40°C to +125°C
Storage Temp Range	-65°C to +150°C
Lead Temp Range (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
8-Lead NSO	471mW
Derates above +70°C	
8-Lead NSO	5.9mW/°C

II. Manufacturing Information

A. Description/Function:	Low Noise, Precision, +2.5V/+4.096V/+5V Voltage Reference
B. Process:	S3
C. Number of Device Transistors:	435
D. Fabrication Location:	California or Oregon, USA
E. Assembly Location:	Thailand or Malaysia
F. Date of Initial Production:	May, 2001

III. Packaging Information

A. Package Type:	8-Lead NSO
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Non-Conductive
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-0901-0148
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	85 x 145 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/Si (Aluminum/ Silicon)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliability Lab Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 720 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

└─ Thermal acceleration factor assuming a 0.8eV activation energy

$$\lambda = 1.51 \times 10^{-9} \quad \lambda = 1.51 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #06-5394) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The RF20 die type has been found to have all pins able to withstand a transient pulse of $\pm 2000\text{V}$, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of $\pm 250\text{mA}$ and/or $\pm 20\text{V}$.

Table 1
Reliability Evaluation Test Results

MAX6220ASA50

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	720	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	2299	18
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the uMax package.

Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

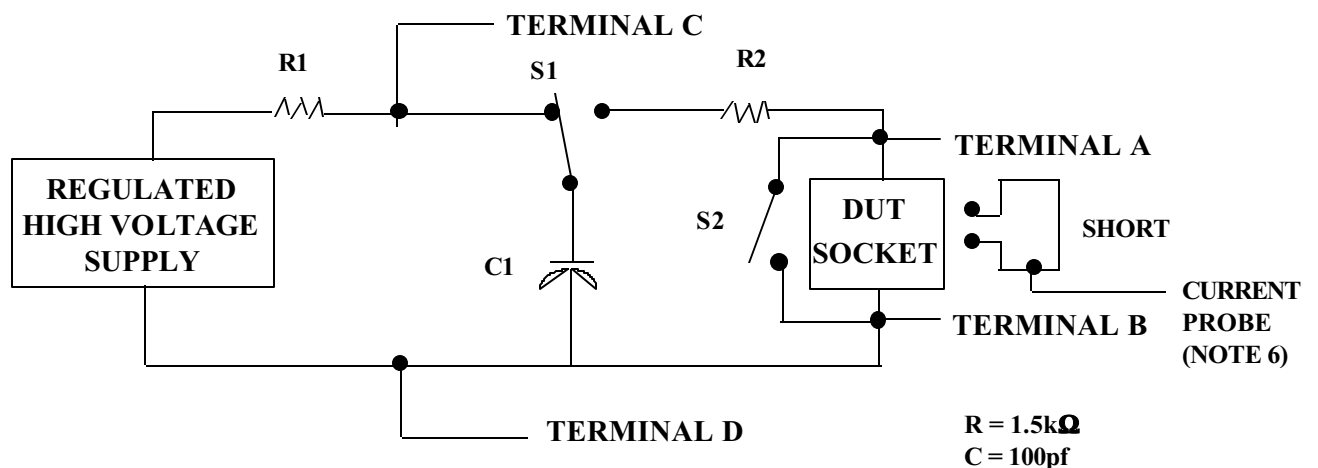
1/ Table II is restated in narrative form in 3.4 below.

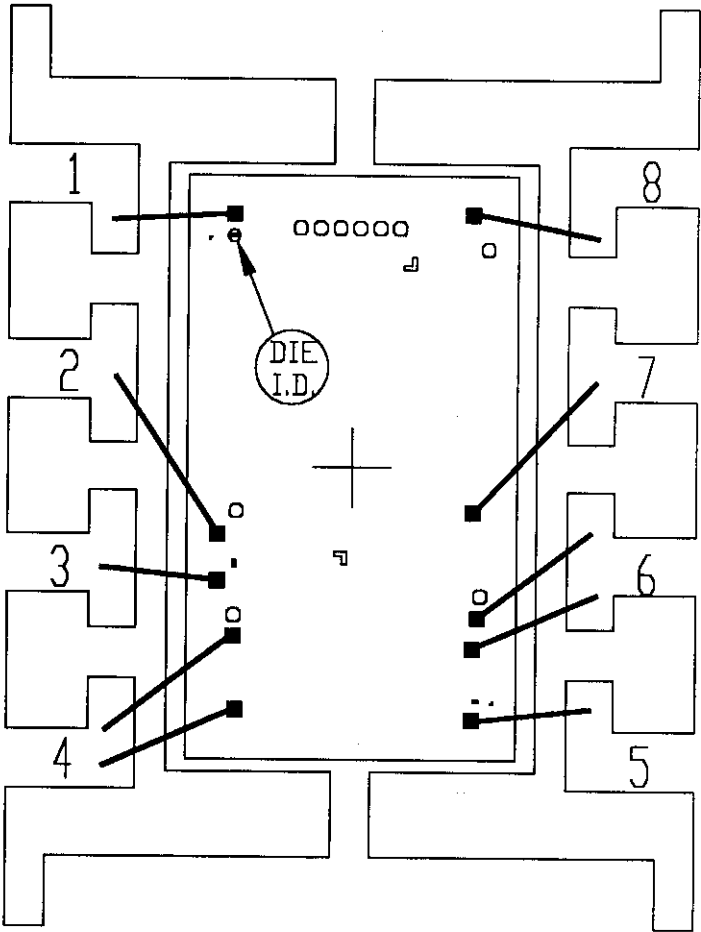
2/ No connects are not to be tested.

3/ Repeat pin combination I for each named Power supply and for ground
(e.g., where V_{PS1} is V_{DD} , V_{CC} , V_{SS} , V_{BB} , GND, $+V_S$, $-V_S$, V_{REF} , etc).

3.4 Pin combinations to be tested.

- Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1} , or V_{SS2} or V_{SS3} or V_{CC1} , or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





PKG.CODE: S8-5		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 95 X 155	PKG.	<i>SVC</i> AUG 29 1997		BUILDSHEET NUMBER:	REV:
	DESIGN	<i>Gabriel Tamm</i>	<i>8/28/97</i>	05-0901-0148	A

W.D. Williams
6/25/99

c/s base
boards

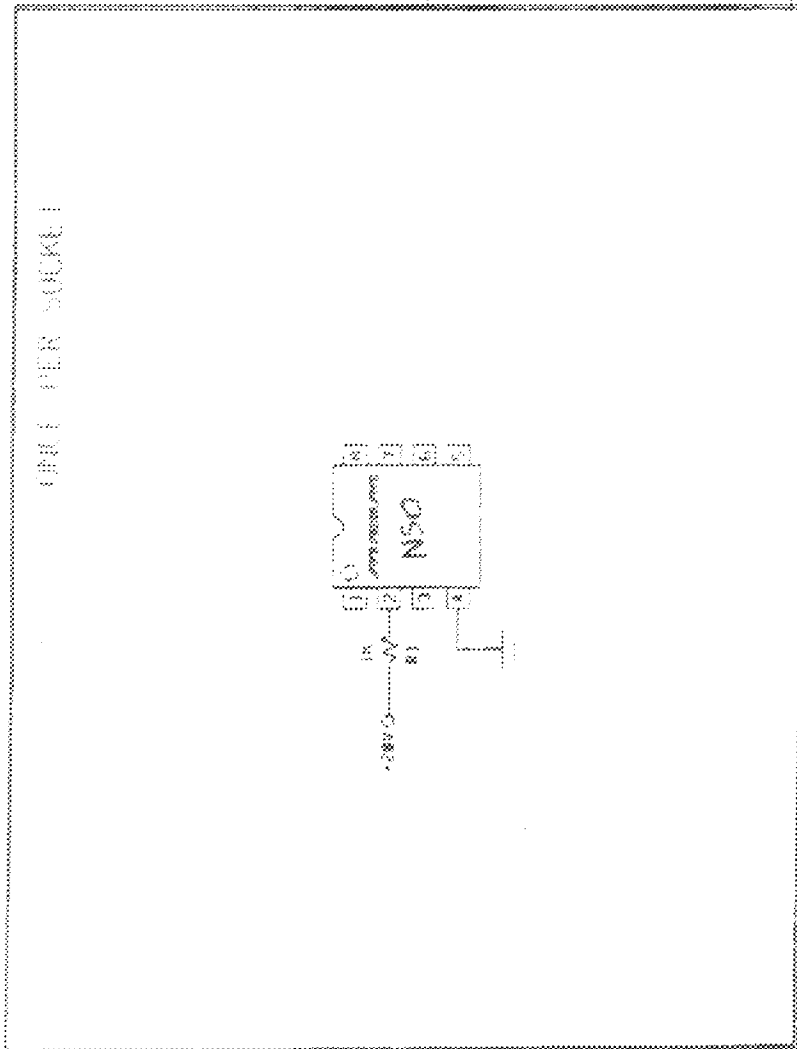
Old boards need

OTS-8(16)-1,2,7-03 to be

modified
again
now
8 columns

ONCE PER BOARD

ONCE PER SOCKET



NOTES:
1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 100 HOURS MIN. OR EQUIVALENT
3. ALL DIMENSIONS AND MATERIAL MUST STAND
4. APPROVED FOR (S) 10/10/83

SPEC NO. 06-5314 REV A

DATE: 12/14/98

DRAWN BY: C. JONES

DEVICE TYPE
PAC80124

DATE: 06/24/98