19-2244; Rev 0; 10/01

MAXIM

+48V Quad Hot-Swap Controllers For Power-Over-LAN

General Description

The MAX5913/MAX5914 are quadruple hot-swap controllers. The MAX5913/MAX5914 independently control four external N-channel switches to hot-swap system loads from a single V_{CC} supply line. The devices allow the safe insertion and removal of power devices from live network ports. Operating supply voltage range is between +35V and +57V. The devices are intended for applications in Power-Over-Media-Dependent Interface (MDI), but are not limited to such usage.

The MAX5913/MAX5914 feature an internal undervoltage lockout (UVLO) function that prevents the FET from turning on, if V_{CC} does not exceed the default value of +32V. The devices also feature a +12V relay driver with 100mA current drive capable of driving low-voltage +3.3V relays. The MAX5913 features an active-low relay driver that sinks current when the relay output is enabled. The MAX5914 features an active-high relay driver output that sources 1mA to drive an external FET relay driver when the relay output is enabled. Control circuitry ensures the relays and the FETs are off until V_{CC} reaches the UVLO threshold. The MAX5913/MAX5914 use an external sense resistor to enable all the internal current-sense functions.

The MAX5913/MAX5914 feature a programmable analog current-limit circuit. If the switch remains in current limit for more than a programmable time, the N-channel FET latches off and the supply can be restarted either by autoretry or by an external command after the preset off-time has elapsed.

The MAX5913/MAX5914 are available in a 44-pin MQFP package and are specified for the extended -40°C to +85°C operating temperature range.

Applications

Power-Over-LAN

Power-Over-MDI

IP Phone Switches/Routers

Telecom Line Cards

Network Switches/Routers

Mid-Span Power-Over-MDI

Typical Operating Circiut appears at end of data sheet.

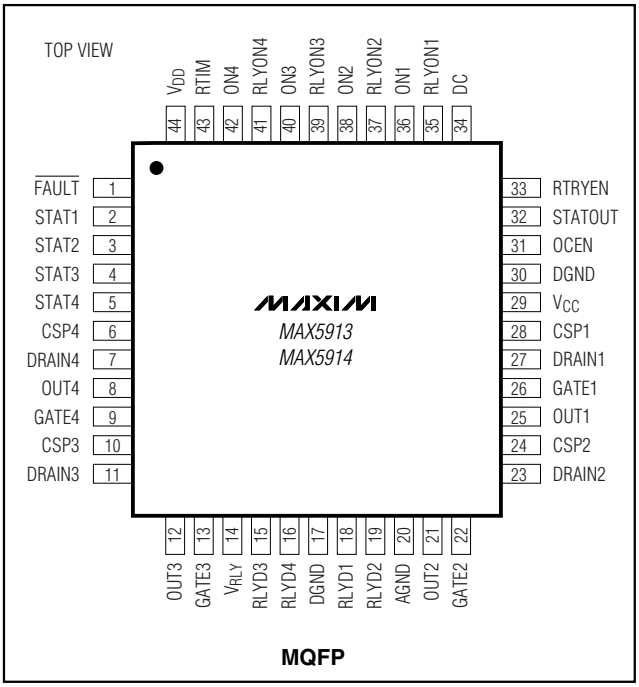
Features

- **Wide Operating Input Voltage Range: +35V to +57V**
- **IEEE 802.3AF Compatible**
- **Four Independent Power Switch Controllers**
- **Open-Circuit Detector**
- **On-Board Charge Pumps to Drive External N-Channel FETs**
- **Current Sense with External Resistor**
- **Foldback Current Limiting**
- **+32V Input Undervoltage Lockout**
- **On-Chip +12V, 100mA Voltage Relay Drivers**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX5913EMH	-40°C to +85°C	44 MQFP
MAX5914EMH	-40°C to +85°C	44 MQFP

Pin Configuration



MQFP

+48V Quad Hot-Swap Controllers For Power-Over-LAN

ABSOLUTE MAXIMUM RATINGS

V_{CC} to AGND or DGND .....-0.6V to +65V
DRAIN_, OUT_ to AGND or DGND .....-0.6V to V_{CC} +0.3V
CSP_ to V_{CC} .....-0.3V to +0.3V
GATE_ to OUT_ .....-0.3V to +13V
V_{RLY} to DGND .....-0.3V to +18V
RLYD_ to DGND .....-0.3V to (V_{RLY} + 0.3V)
ON_, RLYON_, OCEN, RTRYEN, STATOUT, $\overline{DC}$ to DGND .....-0.3V to +12V
$\overline{FAULT}$ to DGND .....-0.3V to +12V
STAT_, RTIM to DGND .....-0.3V to (V_{DD} + 0.3V)
V_{DD} to DGND .....-0.3V to +7V
DGND to AGND .....-5V to +5V
Current into RLYD_ .....-50mA to +150mA
Current into Any Other Pin .....±50mA
Continuous Power Dissipation (T_A = +70°C)
44-Pin MQFP (derate 12.7mW/°C above +70°C) 1.013W
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = $V_{CSP\_}$ = +48V, AGND = DGND = 0, V_{DD} = +3.3V, V_{RLY} = +12V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = $V_{CSP\_}$ = +48V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Analog Supply Voltage	V_{CC}	Measured with respect to AGND	35		57	V
Analog Supply Current	I_S	V_{CC} = $V_{CSP\_}$, I_S = I_{CC} + $I_{CSP\_}$		2.2	3	mA
Digital Supply Voltage	V_{DD}	Measured with respect to DGND	1.8	3.3	3.7	V
Digital Supply Current	I_{DD}	All logic outputs high, RTIM floating		1	3	mA
Analog Supply Undervoltage Lockout	V_{UVLO}	V_{CC} rising, circuits enabled	29.5	32	35	V
UVLO Hysteresis	$V_{UVLO,H}$			3		V
UVLO Deglitch Delay	$t_{D,UVLO}$	V_{ON} = 3.3V, V_{RLYON} = 3.3V (Figure 1)	16	27.5	39	ms
Relay Driver Supply	V_{RLY}	Measured with respect to DGND			14	V
Ground Potential Difference	V_{GG}	Voltage difference between DGND and AGND	-4		4	V
FEEDBACK INPUT AND CURRENT SENSE						
OUT Sense Bias Current	I_{FP}	$V_{OUT\_}$ = V_{CC}			2	µA
Initial Feedback Voltage	V_{FB_S}	Voltage under which the foldback circuit starts reducing the current-limit value (Note 1)		18		V
Current-Limit Threshold Voltage	V_{SC}	Maximum ΔV across R_{SENSE} at V_{OUT} > V_{FB_S}	120	140	160	mV
Foldback Voltage	V_{FLBK}	Maximum ΔV across R_{SENSE} at V_{OUT} = 0	40	48	56	mV
Fast Discharge Threshold	V_{FC}		360	420	480	mV
Switch-On Threshold	V_{SWON}	Maximum V_{CC} - V_{OUT} at which the switch is defined as fully on, V_{OUT} increasing	1	1.5	2	V
Switch-On Comparator Hysteresis	V_{SWON_H}			80		mV
MOSFET DRIVERS						
Gate Overdrive Voltage	V_{GS}	V_{GATE} - V_{CC} when switch is fully on 0°C to +85°C	7	9	11	V
		-40°C to 0°C	7	9	12	
Gate Charge Current	I_{GATE}	V_{GATE} = 0	7	10	13	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = $V_{CSP\_}$ = +48V, AGND = DGND = 0, V_{DD} = +3.3V, V_{RLY} = +12V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = $V_{CSP\_}$ +48V and T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gate Discharge Current	$I_{GATE,DIS}$	During current regulation		8		µA
		V_{ON} = 0		1		mA
		($V_{CSP\_}$ - $V_{DRAIN\_}$) > V_{FC}		15		mA
Source-Gate Clamp Voltage	V_{SGZ}	$V_{OUT\_}$ = 0, force 30mA into GATE_, measure V_{GATE} - V_{OUT}	14	16.5	18	V
OPEN-CIRCUIT DETECTOR						
Open-Circuit Current-Threshold Voltage	V_{OC}	Minimum ΔV across R_{SENSE} to detect an open circuit	1.5	3	4.5	mV
Delay to Open-Circuit Detect	t_{OC}	(Figure 2)	560	960	1370	ms
Deglitch Delay	t_{LPFD}	($V_{CSP\_}$ - $V_{DRAIN\_}$) < V_{OC} (Figure 2)	16	27.5	39	ms
RELAY DRIVERS						
Maximum Low Voltage (MAX5913)	V_{RLOW}	RLYON = high, $I_{RLYD\_}$ = 100mA			0.5	V
Relay Pullup Current (MAX5914)	I_{RPLUP}	RLYON = high, $V_{RLYD\_}$ = 0	0.3	0.55	0.8	mA
Clamp Diode Voltage	V_{RCLAMP}	Force 100mA into RLYD, measure V_{RLYD} - V_{RLY}			2	V
Relay Output Leakage		RLYON_ = low, $V_{RLYD\_}$ = V_{RLY}		1		µA
TIMING						
Short-Circuit and Startup Timer (Note 2)	t_O	On time for continuous overcurrent conditions, R_{RTIM} = 2kΩ	4.8	6.4	8.0	ms
		On time for continuous overcurrent conditions, R_{RTIM} = 40kΩ	60	128	196	ms
		On time for continuous overcurrent conditions, R_{RTIM} = ∞	4.2	6.9	9.7	ms
Auto-Retry Duty Cycle		DC = logic low		1		%
		DC = logic high		2		%
		DC = floating		4		%
Port Turn-ON Delay	t_{ON_DEL}	V_{ON} = 3.3V (Figure 3)	16	27.5	39	ms
Relay Turn-OFF Delay	t_{OFF_DEL}	After RLYON_ goes low (Figure 3)	1.64	3.3	5.00	ms
DIGITAL INTERFACE						
DC Pin Input Voltage High	V_{IH_DC}	+1.8V ≤ V_{DD} ≤ +3.7V	0.7 x V_{DD}			V
DC Pin Input Voltage Low	V_{IL_DC}	+1.8V ≤ V_{DD} ≤ +3.7V			0.3 x V_{DD}	V
DC Pin Input Impedance	R_{IN_DC}			1		kΩ
Logic Input High	V_{IH}	+1.8V ≤ V_{DD} ≤ +3.7V	0.8 x V_{DD}			V
Logic Input Low	V_{IL}	+1.8V ≤ V_{DD} ≤ +3.7V			0.3 x V_{DD}	V
Logic Input Leakage					1	µA
$\overline{FAULT}$ Output Voltage Low	V_{FL}	I_{SINK} = 4mA			0.4	V
$\overline{FAULT}$ High Input Leakage					1	µA
Logic Output Voltage High	V_{OH}	STAT_ outputs sourcing 0.5mA	V_{DD} - 0.4			mV
Logic Output Voltage Low	V_{OL}	STAT_ outputs sinking 0.5mA			0.4	V

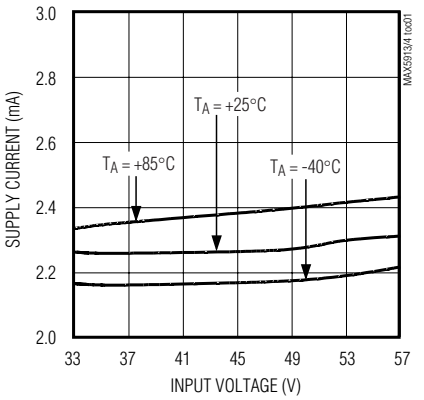
Note 1: See *Typical Operating Characteristics* for Current-Limit Foldback, and refer to *Current Sensing and Regulation* section.
Note 2: The resistor at RTIM can range from 2kΩ to 40kΩ.
Note 3: Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits at -40°C are guaranteed by design and characterization, but are not production tested.

+48V Quad Hot-Swap Controllers For Power-Over-LAN

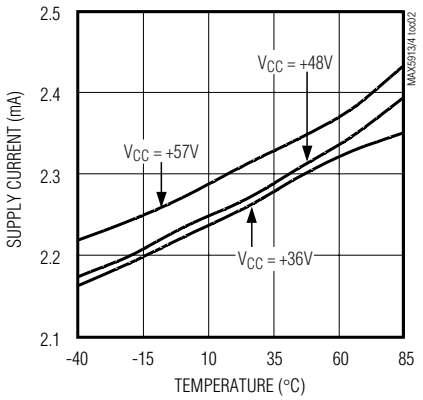
Typical Operating Characteristics

($V_{CSP\_}$ = V_{CC} = +48V, V_{DD} = +3.3V, V_{RLY} = +12V, AGND = DGND = 0, RTIM = open, T_A = +25°C, unless otherwise specified.)

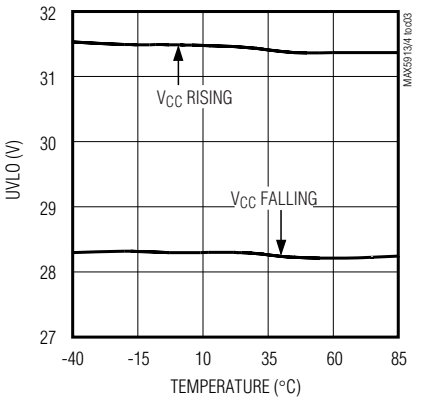
SUPPLY CURRENT vs. INPUT VOLTAGE



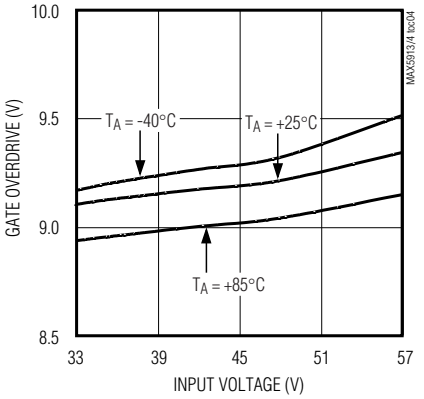
SUPPLY CURRENT vs. TEMPERATURE



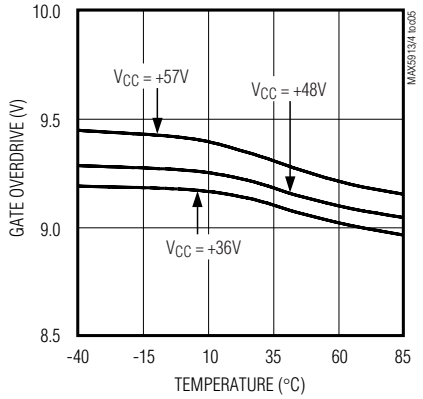
UNDERVOLTAGE LOCKOUT vs. TEMPERATURE



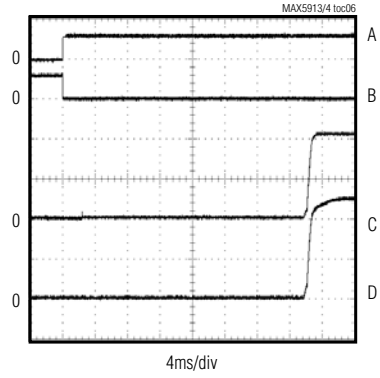
GATE OVERDRIVE VOLTAGE vs. INPUT VOLTAGE



GATE OVERDRIVE VOLTAGE vs. TEMPERATURE

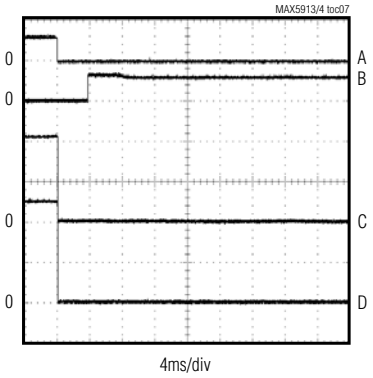


STARTUP WAVEFORMS



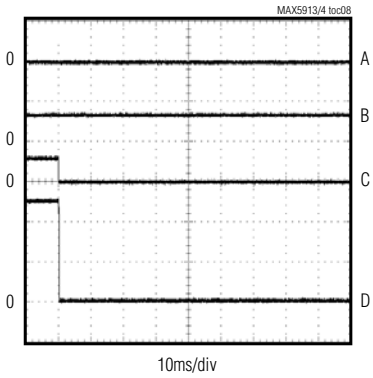
A: V_{ON} = V_{RLYON}, 5V/div
B: V_{RLYD}, 20V/div
C: V_{OUT}, 20V/div
D: V_{GATE}, 20V/div

TURN-OFF WAVEFORMS



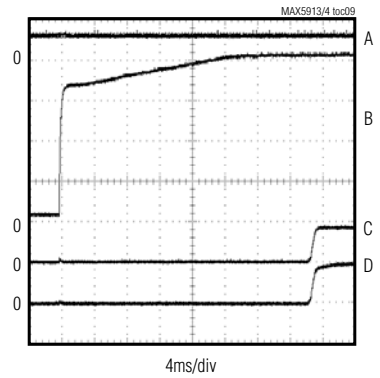
A: V_{ON} = V_{RLYON}, 5V/div
B: V_{RLYD}, 20V/div
C: V_{OUT}, 20V/div
D: V_{GATE}, 20V/div

GATE TURN-OFF WAVEFORM



A: V_{RLYD}, 20V/div
B: V_{RLYON}, 5V/div
C: V_{ON}, 5V/div
D: V_{GATE}, 20V/div

UVLO TURN-ON DELAY



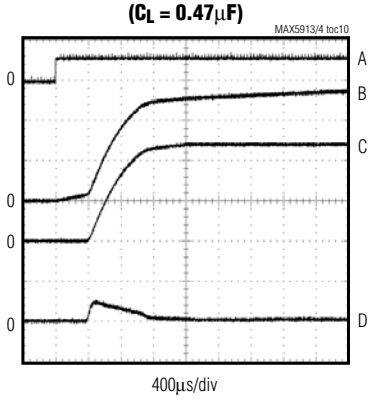
RLYON = V_{DD}
A: V_{ON}, 5V/div
B: V_{CC}, 10V/div
C: V_{OUT}, 50V/div
D: V_{GATE}, 50V/div

MAXIM

Typical Operating Characteristics (continued)

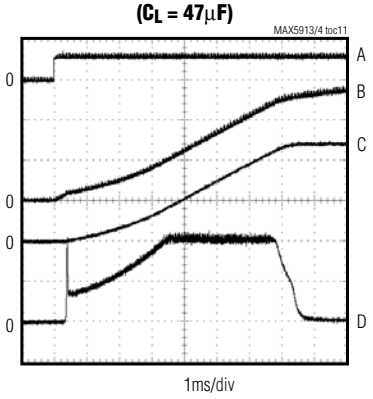
($V_{CSP\_}$ = V_{CC} = +48V, V_{DD} = +3.3V, V_{RLY} = +12V, AGND = DGND = 0, RTIM = open, T_A = +25°C, unless otherwise specified.)

TURN-ON INTO CAPACITIVE LOAD (C_L = 0.47µF)



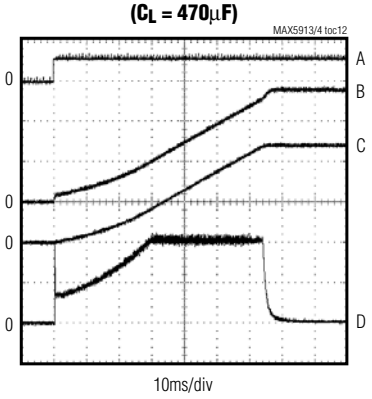
RLYON = V_{DD}
A: V_{ON}, 5V/div
B: V_{GATE}, 20V/div
C: V_{OUT}, 20V/div
D: I_{OUT}, 100mA/div

TURN-ON INTO CAPACITIVE LOAD (C_L = 47µF)



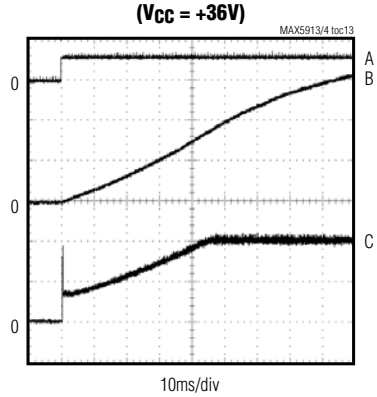
RLYON = V_{DD}, R_{RTIM} = 2kΩ
A: V_{ON}, 5V/div
B: V_{GATE}, 20V/div
C: V_{OUT}, 20V/div
D: I_{OUT}, 200mA/div

TURN-ON INTO CAPACITIVE LOAD (C_L = 470µF)



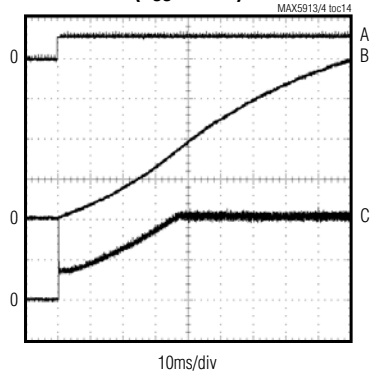
RLYON = V_{DD}, R_{RTIM} = 40kΩ
A: V_{ON}, 5V/div
B: V_{GATE}, 20V/div
C: V_{OUT}, 20V/div
D: I_{OUT}, 200mA/div

CURRENT-LIMIT FOLDBACK (V_{CC} = +36V)



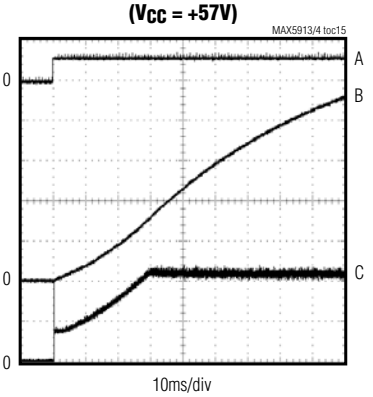
RLYON = V_{DD}, R_L = 100Ω, R_{RTIM} = 40kΩ,
A: V_{ON}, 5V/div
B: V_{OUT}, 10V/div
C: I_{OUT}, 200mA/div

CURRENT-LIMIT FOLDBACK (V_{CC} = +48V)



RLYON = V_{DD}, R_L = 139Ω, R_{RTIM} = 40kΩ,
A: V_{ON}, 5V/div
B: V_{OUT}, 10V/div
C: I_{OUT}, 200mA/div

CURRENT-LIMIT FOLDBACK (V_{CC} = +57V)



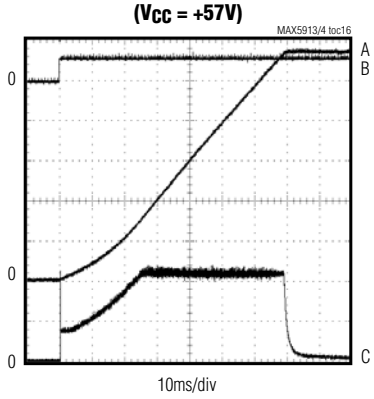
RLYON = V_{DD}, R_L = 162Ω, R_{RTIM} = 40kΩ,
A: V_{ON}, 5V/div
B: V_{OUT}, 10V/div
C: I_{OUT}, 200mA/div

+48V Quad Hot-Swap Controllers For Power-Over-LAN

Typical Operating Characteristics (continued)

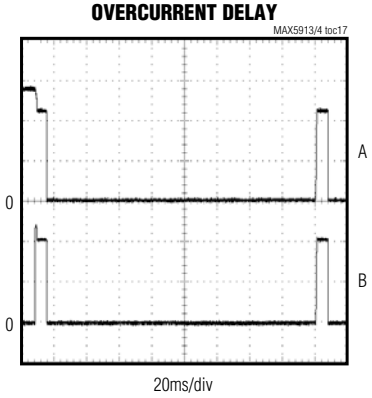
($V_{CSP\_}$ = V_{CC} = +48V, V_{DD} = +3.3V, V_{RLY} = +12V, AGND = DGND = 0, RTIM = open, T_A = +25°C, unless otherwise specified.)

CURRENT-LIMIT FOLDBACK (V_{CC} = +57V)



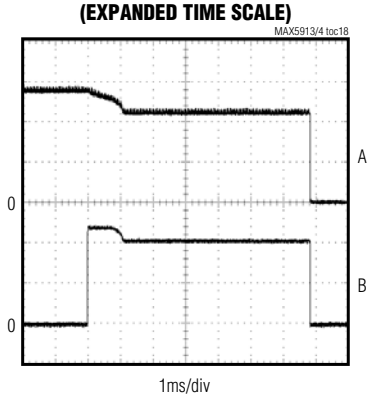
RLYON = V_{DD}, R_L = OPEN, R_{RTIM} = 40kΩ, C_{LOAD} = 470µF
A: V_{ON}, 5V/div
B: V_{OUT}, 10V/div
C: I_{OUT}, 200mA/div

OVERCURRENT DELAY



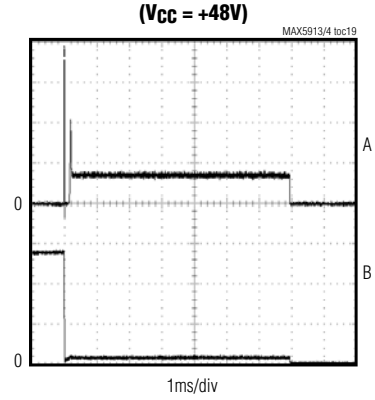
RTRYEN = V_{DD}, RLYON = ON = V_{DD}, DC = 4%, R_{RTIM} = 2kΩ, R_L = 100Ω
A: V_{GATE}, 20V/div
B: I_{OUT}, 200mA/div

OVERCURRENT DELAY (EXPANDED TIME SCALE)



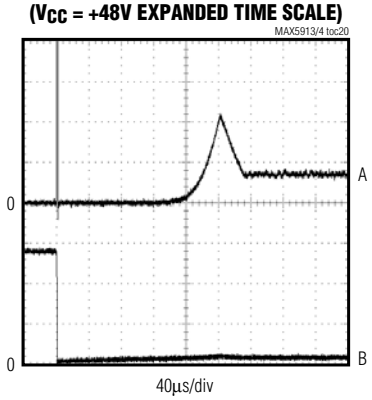
RTRYEN = V_{DD}, RLYON = ON = V_{DD}, DC = DON'T CARE, R_{RTIM} = 2kΩ, R_L = 100Ω
A: V_{GATE}, 20V/div
B: I_{OUT}, 200mA/div

SHORT-CIRCUIT RESPONSE (V_{CC} = +48V)



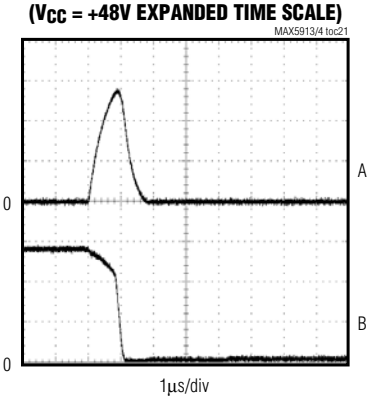
ON = RLYON = V_{DD}, R_L = 1Ω, R_{RTIM} = 2kΩ
A: I_{OUT}, 200mA/div
B: V_{GATE}, 20V/div

SHORT-CIRCUIT RESPONSE (V_{CC} = +48V EXPANDED TIME SCALE)



ON = RLYON = V_{DD}, R_L = 1Ω, R_{RTIM} = 2kΩ
A: I_{OUT}, 200mA/div
B: V_{GATE}, 20V/div

PEAK SHORT-CIRCUIT RESPONSE (V_{CC} = +48V EXPANDED TIME SCALE)

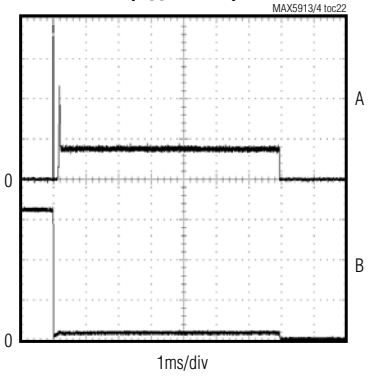


ON = RLYON = V_{DD}, R_L = 1Ω, R_{RTIM} = 2kΩ
A: I_{OUT}, 5A/div
B: V_{GATE}, 20V/div

Typical Operating Characteristics (continued)

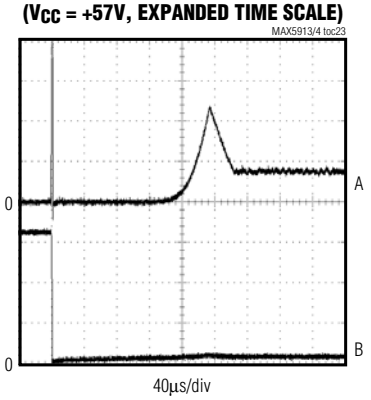
($V_{CSP\_}$ = V_{CC} = +48V, V_{DD} = +3.3V, V_{RLY} = +12V, AGND = DGND = 0, RTIM = open, T_A = +25°C, unless otherwise specified.)

SHORT-CIRCUIT RESPONSE (V_{CC} = +57V)



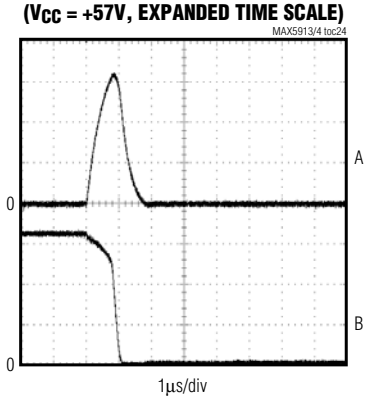
ON = RLYON = V_{DD}
A: I_{OUT}, 200mA/div
B: V_{GATE}, 20V/div

SHORT-CIRCUIT RESPONSE (V_{CC} = +57V, EXPANDED TIME SCALE)



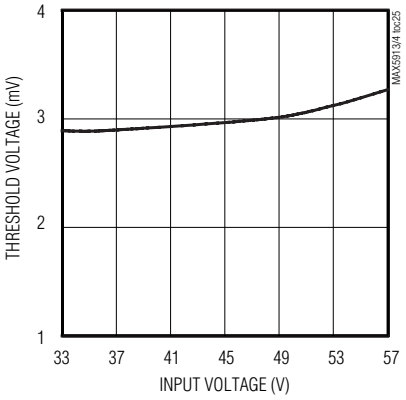
ON = RLYON = V_{DD}, R_L = 1Ω, R_{RTIM} = 2kΩ
A: I_{OUT}, 200mA/div
B: V_{GATE}, 20V/div

PEAK SHORT-CIRCUIT RESPONSE TIME (V_{CC} = +57V, EXPANDED TIME SCALE)

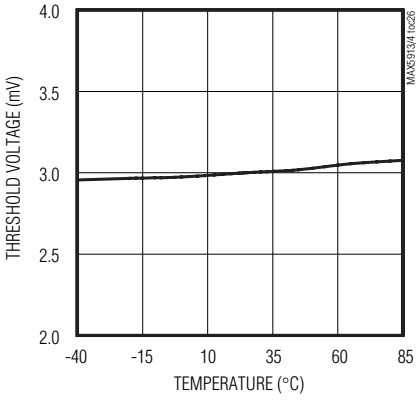


ON = RLYON = V_{DD}, R_L = 1Ω, R_{RTIM} = 2kΩ
A: I_{OUT}, 5A/div
B: V_{GATE}, 20V/div

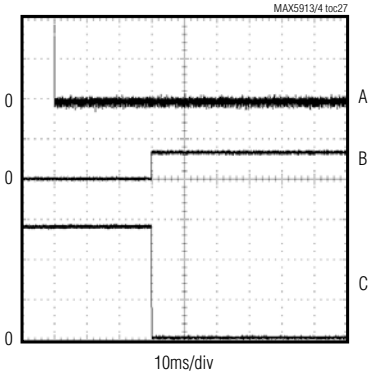
OPEN-CIRCUIT THRESHOLD vs. INPUT VOLTAGE



OPEN-CIRCUIT THRESHOLD vs. TEMPERATURE



OPEN-CIRCUIT GLITCH DELAY



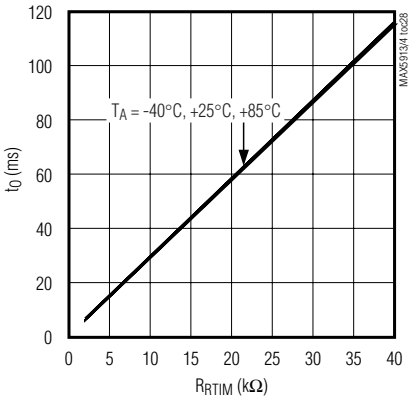
ON = RLYON = V_{DD}, STATOUT = LOW
A: I_{OUT}, 20mA/div
B: V_{STAT}, 5V/div
C: V_{GATE}, 20V/div

+48V Quad Hot-Swap Controllers For Power-Over-LAN

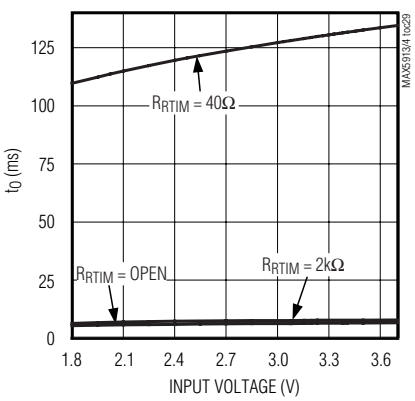
Typical Operating Characteristics (continued)

($V_{CSP\_}$ = V_{CC} = +48V, V_{DD} = +3.3V, V_{RLY} = +12V, AGND = DGND = 0, RTIM = open, T_A = +25°C, unless otherwise specified.)

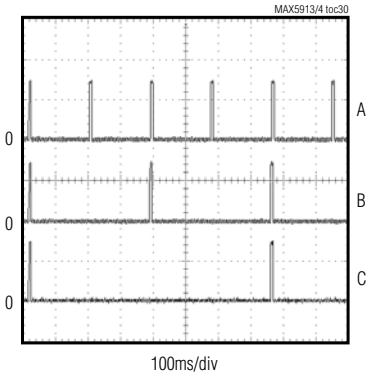
t_O vs. R_{RTIM}



t_O vs. V_{DD}

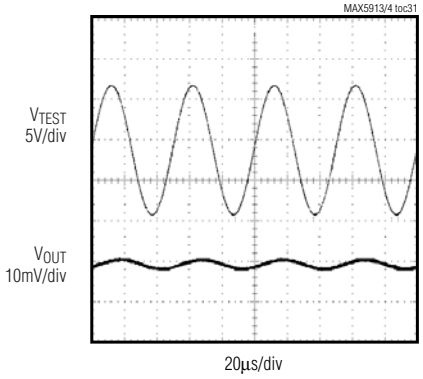


RETRY DUTY CYCLE vs. DC



V_{GATE} = 20V/div, R_{RTIM} = 2kΩ
A: V_{GATE}, 20V/div, DC = FLOATING (4%)
B: V_{GATE}, 20V/div, DC = V_{DD} (2%)
C: V_{GATE}, 20V/div, DC = GND (1%)

CHANNEL-TO-CHANNEL CROSSTALK



SEE FIGURE 4 FOR TEST CIRCUIT

Pin Description

PIN	NAME	FUNCTION
1	$\overline{FAULT}$	Fault Output. $\overline{FAULT}$ is an open-drain output that goes low when a fault is detected on any of the four channels. $\overline{FAULT}$ is low when an OC (open circuit) is detected, or when the MAX5913/MAX5914 is in auto-retry caused by an overcurrent condition. When RTRYEN is low, and the channel switch is latched off due to overcurrent condition, $\overline{FAULT}$ remains low until ON_ is driven low.
2, 3, 4, 5	STAT1, STAT2, STAT3, STAT4	Status Outputs. STAT_ are push-pull outputs. Depending on the STATOUT pin status, STAT_ flags either the Power-OK_ or Port-OC_ status. Power-OK_ high indicates: a) ON_ input is high b) The switch port is fully on and startup is completed ($V_{CSP\_}$ - $V_{OUT\_}$) < V_{SWON} c) Input voltage is above V_{UVLO} d) Switch is not in current limit. Power-OK_ low indicates a fault with any of the above conditions. Port_OC_ output high indicates that the switch is latched off because the switch current is less than the open current threshold Port_OC is low otherwise.
6, 10, 24, 28	CSP4, CSP3, CSP2, CSP1	Current-Sense Positive Input. Connect to V_{CC} and place a current-sense resistor from CSP_ to DRAIN_. Use Kelvin sense trace from current-sense resistor to CSP_ (see Figure 7).
7, 11, 23, 27	DRAIN4, DRAIN3, DRAIN2, DRAIN1	MOSFET Drain Current-Sense Negative Input. Connect to drain of power MOSFET and connect a current-sense resistor from CSP_ to DRAIN_. Use Kelvin sense trace from current-sense resistor to DRAIN_ (see Figure 7).
8, 12, 21, 25	OUT4, OUT3, OUT2, OUT1	MOSFET Source Output Voltage Sense. Connect to power MOSFET source through a 100Ω series resistor.
9, 13, 22, 26	GATE4, GATE3, GATE2, GATE1	MOSFET Gate Driver Output. The MAX5913/MAX5914 regulate the gate-drive voltage to (V_{CC} + 9V) to fully turn on the power N-channel MOSFET. GATE_ sources 10µA during startup to slowly turn-on the MOSFET switch. GATE_ sinks 1mA to turn-off the MOSFET switch.
14	V_{RLY}	Relay Supply Voltage Input. Referenced to DGND.
15, 16, 18, 19	RLYD3, RLYD4, RLYD1, RLYD2	Relay-Drive Output. For the MAX5913, RLYD_ sinks 100mA when the relay driver is enabled. For the MAX5914, RLYD_ sources 1mA when the relay driver is enabled.
17, 30	DGND	Digital Ground. All logic voltages are referred to DGND. The voltage difference between DGND and AGND can be up to ±4V.
20	AGND	Analog Ground. All analog voltages are referred to AGND.
29	V_{CC}	Analog Power Supply. Connect V_{CC} to +35V to +57V power supply. UVLO circutry turns off MOSFET switch and relay for V_{CC} < V_{UVLO}. Bypass V_{CC} to AGND with a 1µF capacitor.
31	OCEN	Open-Circuit Detector Enable Input. Drive OCEN high to enable open-circuit detector, or drive low to disable. When enabled, the open-circuit detector waits for a 900ms delay after Power-OK conditions are met before enabling the open-circuit detector function.
32	STATOUT	Status Output Multiplexer (MUX) Control Input. Controls the signal MUX into the STAT_ outputs. Drive STATOUT high to route Power-OK_ status to STAT_ outputs, or drive STATOUT low to route Port-OC_ status to STAT_ outputs.

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Pin Description (continued)

PIN	NAME	FUNCTION
33	RTRYEN	Auto-Retry Enable Input. Drive RTRYEN high to enable auto-retry. Drive RTRYEN low to enable switch latch-off mode. When switch is latched off, a high-to-low transition on the ON_ control input clears the latch.
34	DC	Duty-Cycle Programming Input. DC sets the minimum off-time after an overcurrent condition latches off the switch. When RTRYEN is high, DC sets the auto-retry duty cycle. Drive DC low for 1% duty cycle, drive DC high for 2%, or leave DC floating for 4% duty cycle.
35, 37, 39, 41	RLYON1, RLYON2, RLYON3, RLYON4	Relay-Driver Control Input. Drive RLYON_ high to enable RLYD_, drive RLYON_ low to turn off MOSFET switch for the channel and disable RLYD_.
36, 38, 40, 42	ON1, ON2, ON3, ON4	MOSFET Switch Control Input. Drive ON_ high to enable GATE_ to turn on MOSFET switch. RLYON_ must be high to enable the switch. Drive ON_ low to disable the switch. Pulling ON_ low also resets the latch when RTRYEN is low or if the switch is latched off due to open-circuit detection.
43	RTIM	Timing Oscillator Frequency Set Input. Connect a 2kΩ to 40kΩ resistor from RTIM to DGND to set the maximum continuous overcurrent time, t_O. Leave RTIM unconnected to set default 6.4ms t_O.
44	V_{DD}	Digital Power Supply. Bypass V_{DD} to DGND with a 1µF capacitor.

Detailed Description

The MAX5913/MAX5914 quadruple hot-swap controllers provide Power-Over-MDI, also known as Power-Over-LAN systems (Figure 5). The MAX5913/MAX5914 enable control of four external N-channel MOSFET switches from a single V_{CC} ranging from +35V to +57V, with timing control and current-limiting functions built in.

Features include undervoltage lockout (UVLO), 100mA relay drivers, dual-level current sense, foldback current limit, programmable overcurrent time and auto-retry periods, internal charge pumps to drive external MOSFET and soft-start, port status output indicating Power-OK or open-circuit conditions (Figure 6).

Switch and Relay Control Inputs

The MAX5913/MAX5914 ON_ inputs turn on the corresponding MOSFET switch. Driving ON_ high turns on the switch if the corresponding RLYON is driven high, and $V_{CC} > V_{UVLO}$ for more than 25.6ms. Driving RLYON_ high immediately turns on the corresponding relay, and activates the 25.6ms delay after which the corresponding ON_ input is active. Driving RLYON_ low immediately turns off the switch and activates a 3.2ms delay after which the relay is turned off. These internal delays safely allow driving ON_ and RLYON_ simultaneously. The relay is turned on while the switch is off so that there is no voltage across the relay contacts. The relay is turned off while the switch is off so that there is no current flowing when the relay contacts are opened (see Figure 3).

Input Voltage and UVLO

The MAX5913/MAX5914 operate from +35V to +57V supply voltage. V_{CC} powers the MAX5913/MAX5914 analog circuitry and is monitored continuously during startup and normal operation. The MAX5913/MAX5914 keep all MOSFET switches and relay drivers securely off before V_{CC} rises above V_{UVLO}. The MAX5913/MAX5914 turn off all MOSFET switches and relay drivers after V_{CC} falls below $V_{UVLO} - V_{UVLO,H}$.

Startup

When the turn-on condition is met (see *Input Voltage and UVLO and Switch* and *Relay Control Inputs* sections), the MAX5913/MAX5914 slowly turn on the external MOSFET switch by charging its gate using a constant current source, I_{GATE} (10µA typ). The gate voltage slope is determined by the total gate capacitance C_{GATE} connected to this node. Since the output voltage follows the gate voltage, thus the output rises with a slope determined by:

$$\frac{\Delta V_{OUT}}{\Delta t} = \frac{I_{GATE}}{C_{GATE}}$$

Test Circuits and Timing Diagrams

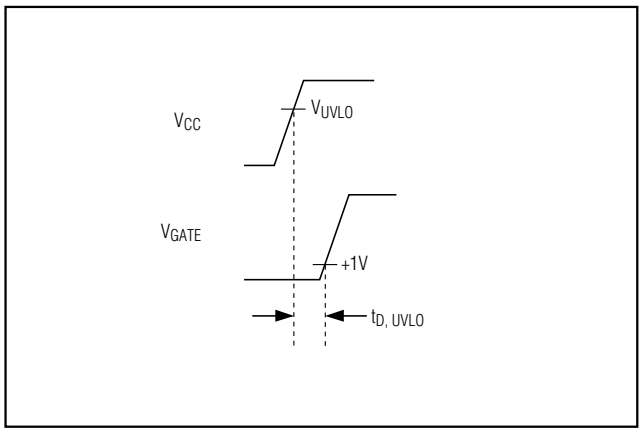

Figure 1. UVLO Deglitch Delay

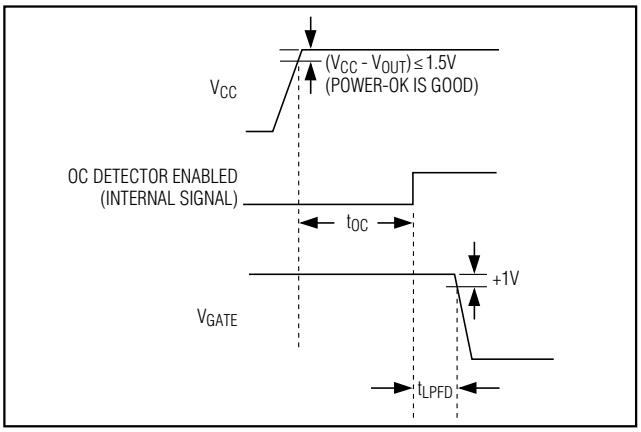

Figure 2. Open-Circuit Detector Deglitch Delay

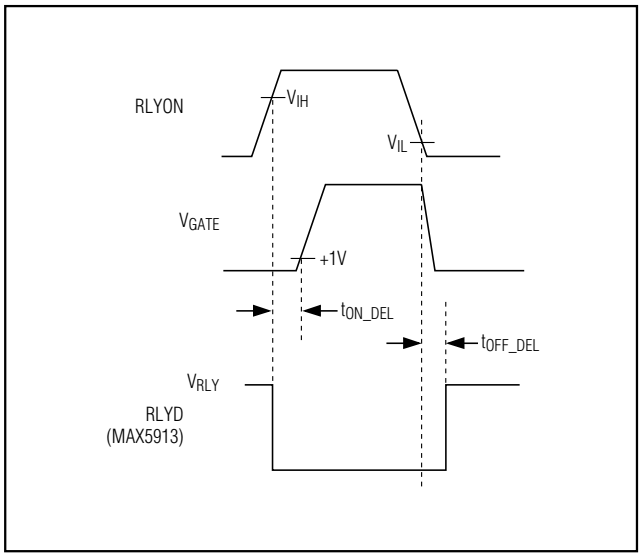

Figure 3. Port Turn-On Delay, Relay Turn-Off Delay

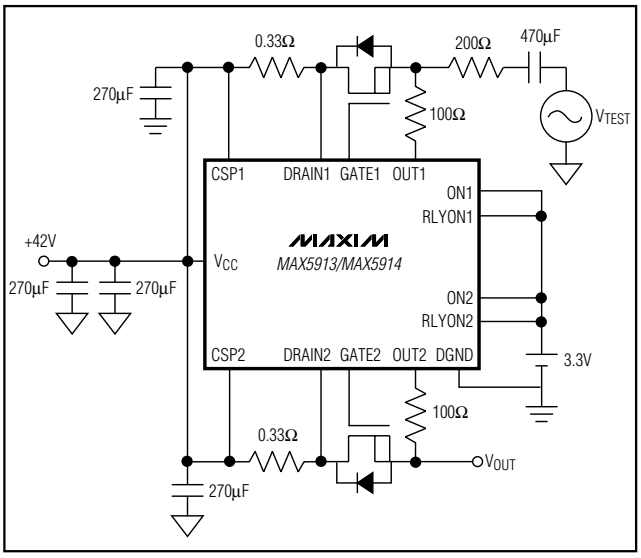

Figure 4. Channel-to-Channel Crosstalk Test Circuit

If a capacitor load is connected to the output the total current through the FET is:

$$I = I_{GATE}\frac{C_L}{C_{GATE}} + I_L$$

where C_L is the load capacitance and I_L is the current required by any load connected to the output during the startup phase.

If the current through the FET reaches the programmed current-limit value:

$$I_{MAX} = \frac{V_{SC}}{R_{SENSE}}$$

the internal current-limit circuitry activates and regulates this FET current to be a value, I_{LIM}, that depends on V_{OUT} (I_{FLBK}) (Figure 8). See the *Current Sensing*

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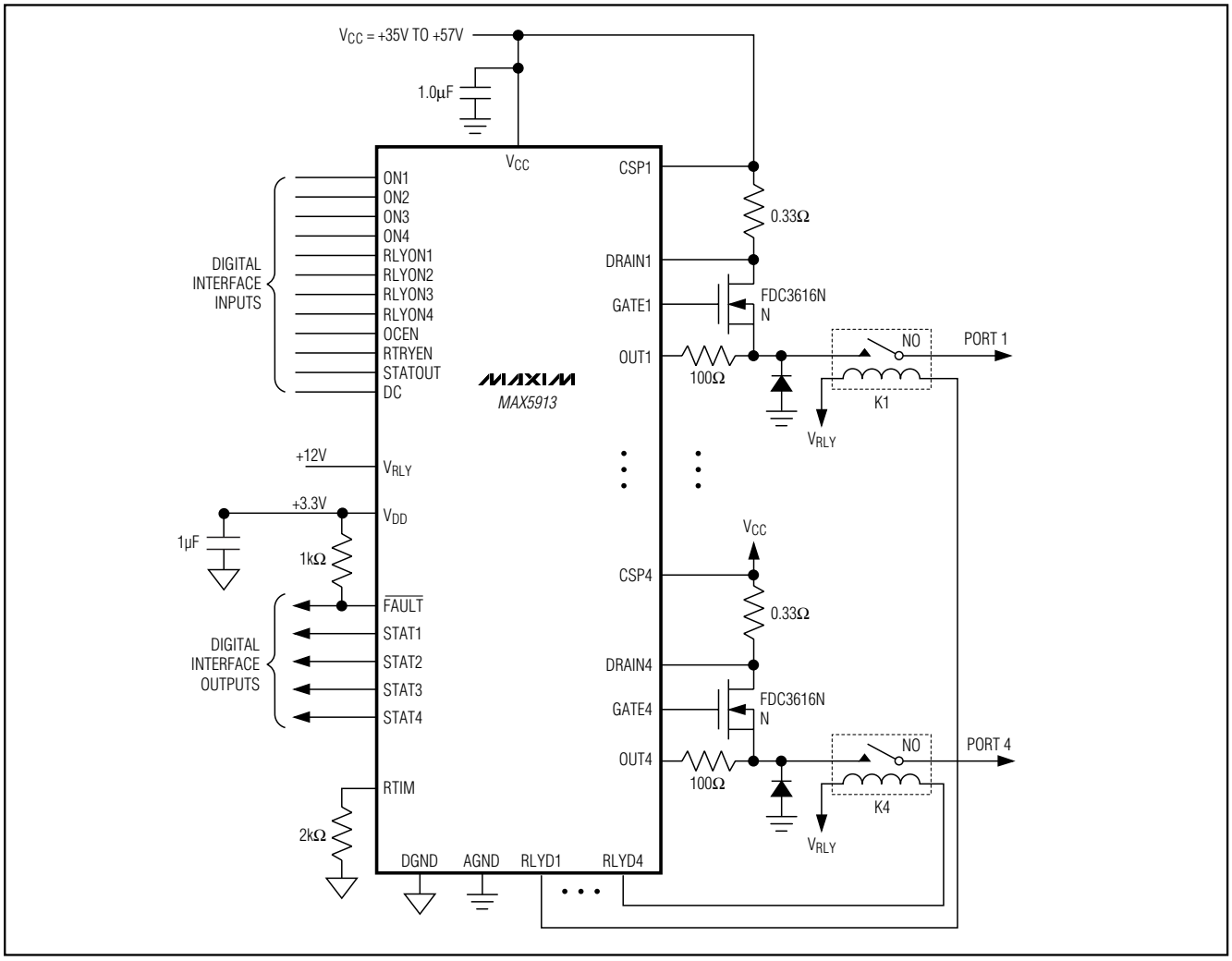

Figure 5. Typical Application Circuit

and Regulation section for more information. In this case the maximum rate of change of the output is determined by:

$$\frac{\Delta V_{OUT}}{\Delta t} = \frac{I_{LIM} - I_L}{C_L}$$

The formula shows the necessity for I_{LIM} to be larger than I_L in order to allow the output voltage to rise. The foldback function is active as long as the circuit is in overcurrent condition. Should the overcurrent condition persist for a period longer than the maximum time t_O, the switch is latched off and GATE_ is discharged to ground with a 1mA pulldown current.

If auto-retry is enabled, the switch turns on again after a waiting period, t_{OFF}, which is determined by the programmed duty cycle.

After the startup, the internal charge pumps provide (V_{CC} + 9V) typical gate overdrive to fully turn on the switch. When the switch is fully on (voltage drop across the switch is ≤ 1.5V), and the switch is not in current limit, the Power-OK signal is asserted.

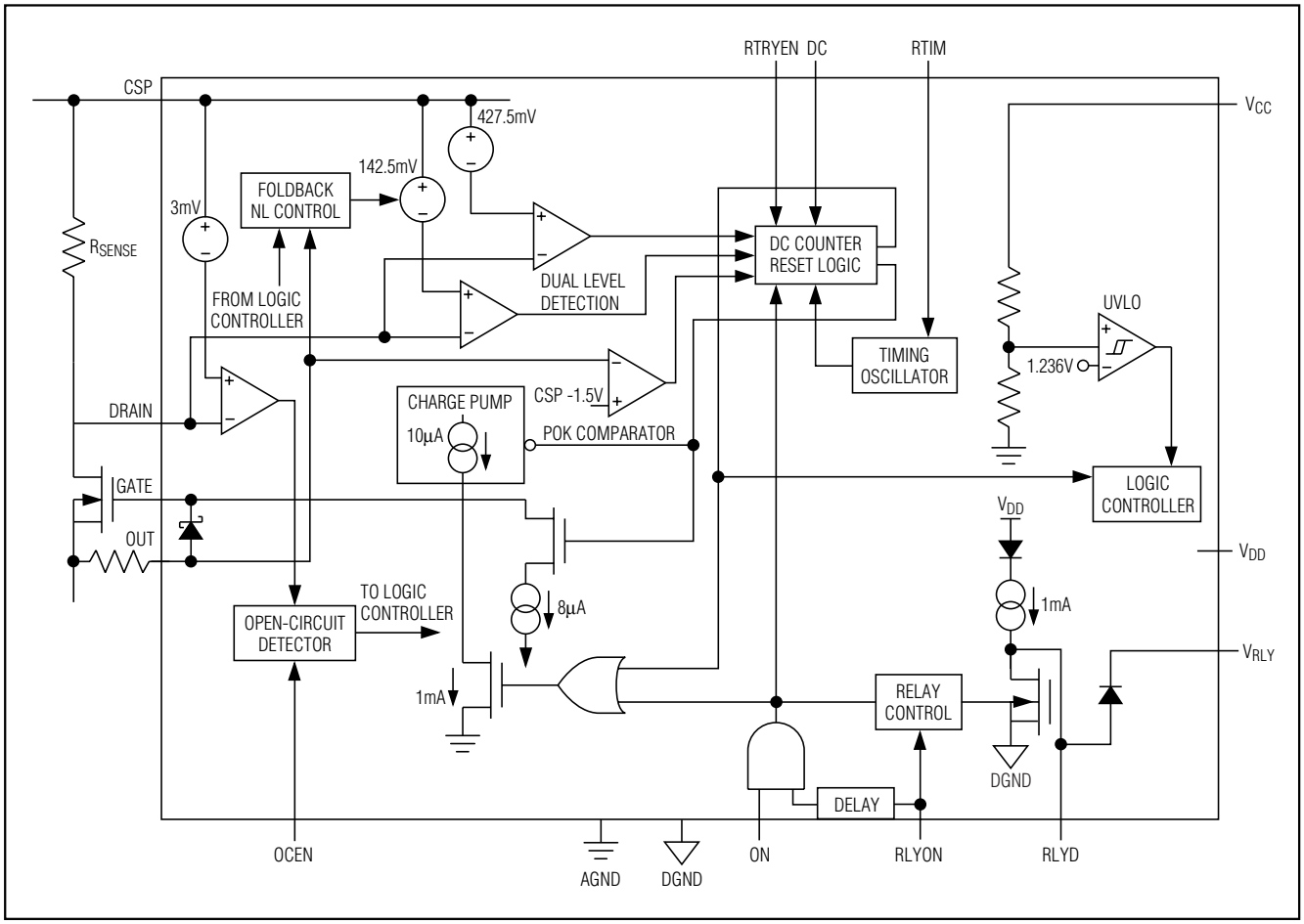

Figure 6. Functional Diagram

Current Sensing and Regulation

The MAX5913/MAX5914 control port current with using two voltage comparators (dual-level detection) that sense the voltage drop across an external current-sense resistor. Connect CSP_ to V_{CC} and connect a current-sense resistor between CSP_ and DRAIN_. Kelvin sensing should be used as shown in Figure 7. The first comparator compares the sensed voltage against VSC threshold (typically 142.5mV). Choose a sense as follows:

$$R_{SENSE} = V_{SC} / I_{MAX}$$

where IMAX is the maximum current allowed through the switch.

When I_{MAX} is reached, foldback current-limit circuitry regulates the current limit as a function of V_{OUT} (Figure 8). As V_{OUT} approaches zero the maximum voltage drop across the sense resistor is lowered to a minimum value of 47.5mV. This foldback feature helps reduce the power dissipation in the external power FET during output overload and output short-circuit conditions. If a load with very low activation voltage is permanently connected to the output, make the minimum limit current sufficiently larger than the load current. If the load current indeed exceeds the foldback-limit value the MAX5913/MAX5914 are not able to power-up the switch.

A second comparator with a detection threshold of $3V_{SC}$ activates a fast 15mA pulldown of the gate. The purpose of this comparator is to rapidly discharge the gate when a momentary current peak overstresses the external FET helping the regulation to act more rapidly.

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The sense resistor is also used to detect an open-circuit or low-current condition with a typical threshold of 3mV.

Open-Circuit Detection

The MAX5913/MAX5914 detect when a port has low current or is open circuit, and turn off the switch to that port. After the switch is turned on and the Power-OK conditions are met, the open-circuit detector is enabled after a 900ms delay. The open-circuit voltage threshold is set at 3mV across the current-sense resistor. Drive OCEN high to enable open-circuit detectors for all four ports. Drive OCEN low to disable the detectors. Each port has an open-circuit flag that can be read from STAT_ outputs when the STATOUT is low. STAT_ output high indicates that the switch is latched off due to an open-circuit condition on that port. To reset the latch pull ON_ low and then high to restart (Table 1).

Output Voltage Sense and Power-OK

The MAX5913/MAX5914 sense the output voltage of the port at the source of the external MOSFET switch. Internally the circuit compares the output voltage with V_{CC} to determine when the FET is completely on. A "Power-OK" condition is met when:

$$(V_{CC} - V_{OUT}) \le 1.5V$$

The internal circuit monitors V_{OUT} to determine the value of the foldback current when the circuit goes into current-limit conditions. The value of the current limit decreases as the output voltage decreases in order to limit the power dissipation of the FET. The nonlinear relationship between V_{OUT} and I_{LIM} is depicted in Figure 8.

The foldback circuit is active whenever the MAX5913/MAX5914 is in current-limit mode after an overcurrent condition has been detected.

Connect a catch diode to analog ground and a 100Ω resistor in series with OUT_ to limit the current during negative inductive kicks that can bring OUT_ below the ground potential (Figure 5).

Relay Drivers

The MAX5913/MAX5914 include on-chip relay drivers, RYLD_, capable of sinking 100mA. When RLYON_ goes high the MAX5913/MAX5914 immediately enable the relay driver, and the corresponding ON_ switch control input is delayed 25.6ms to allow the relay to close under a zero-voltage condition. When RLYON_ goes low, the MAX5913/MAX5914 immediately turn off the corresponding switch, and then turn off the relay driver after a 3.2ms delay, ensuring the relay contacts open under a zero-current condition. The polarity of the MAX5913 RLYD_ is opposite to that of the MAX5914. For the MAX5913, upon the assertion of the RLYON_ input RLYD_ sinks 100mA to DGND. For the MAX5914 when RLYON_ is high, an internal 1mA current source pulls up RLYD_ to V_{DD}. A 100mA catch diode is internally connected between RYLD_ and V_{RLY} to protect the MAX5913/MAX5914 from inductive kicks from the relay coil. V_{RLY} must be connected to the high-side relay supply voltage.

Programmable Timing, RTIM

An external resistor from RTIM to DGND sets the frequency of the internal oscillator upon which t_O and the auto-retry times are based.

Use 2kΩ to 40kΩ resistors for R_{RTIM}.

$$t_O = (R_{RTIM} / 2k\Omega)\ (6.4ms)$$

If RTIM is unconnected (floating), an internal resistor sets t_O to a nominal 6.4ms.

Table 1. Status Output

PORT_ CONDITION	OCEN	STATOUT	STAT_
Enabled. Switch fully on and not in current limit	x	H	H (Power-OK_ is good)
Enabled. Switch in current limit, or V_{DS} > 1.5V	x	H	L (Power-OK_ is not good)
Enabled. Switch current is less than OC threshold, port is latched off	H	L	H (Port-OC_, Port current is low or zero)
Enabled. Switch fully on and output current is greater than OC threshold	H	L	L (Port-OC_, Port current is good)
Disabled	L	L	L

Auto-Retry and Programmable Duty Cycle

The MAX5913/MAX5914 feature auto-retry with adjustable duty cycle. Driving RTRYEN high enables the auto-retry function. When the switch encounters an overcurrent for a period greater than t_O the switch is turned off, and remains off for a t_{OFF} programmed by DC, a three-level input. After the t_{OFF} period, the switch is automatically turned on again. When the port encounters a continuous overload or short-circuit condition, the switch turns on and off repeatedly with the on duty cycle of 1%, 2%, or 4% depending on the DC input state (Table 2). When RTRYEN is low, the auto-retry is disabled, and a fault condition at the switch turns the switch off and the switch remains latched off. Driving the corresponding ON control input low resets the latch. Pulling ON high to turn on the switch. However, the MAX5913/MAX5914 always waits a minimum time t_{OFF}, before restarting the switch.

Logic Interface and Status Outputs

The MAX5913/MAX5914 logic interface controls the device functionality. All the basic control functions for the four switches are separated. ON_ enables individual on/off control of each MOSFET (the corresponding relay must be on to turn on the switch). RLYON_ enables individual on/off control of each relay. STAT_ indicates Power-OK or Port-OC (open circuit) status of each switch. The other logic pins are common to all four switches. A single $\overline{FAULT}$ output goes low when any of the four channels is latched off. Driving OCEN high enables the open-circuit detectors. Driving RTRYEN high enables the auto-retry function, RTRYEN low enables the switch latch-off function. DC, a three-level logic input, programs the duty cycle. The STATOUT input selects the signal multiplexed at STAT_ outputs (Table 1.). Driving STATOUT high routes Power-OK status to the STAT_ outputs. Driving STATOUT low routes Port-OC status to the STAT_ outputs.

Fault Management

UVLO and Power-OK

The MAX5913/MAX5914 monitor the V_{CC} input voltage and each switch's current and voltage to determine Power-OK, overcurrent, or Port-OC status. When V_{CC} falls below the UVLO threshold, $\overline{FAULT}$ goes low and all four switches and relays are turned off. When the volage across the switch is less than 1.5V, the switch is fully on, and if the switch is not in current limit or open circuit, Power-OK status is good (high).

Open-Circuit Faults

With the open circuit detector enabled, when any switch current falls below the open-circuit detector threshold current, the open-circuit detector turns off the switch after a 25.6ms delay, $\overline{FAULT}$ goes low and the Port-OC flag is set for that switch. To clear the switch latched-off condition, $\overline{FAULT}$ and Port-OC flags drive the corresponding ON input low.

Overcurrent Faults

When an on switch current exceeds the current-limit threshold, foldback circuitry activates and regulates the switch current. When current limit lasts for longer than t_O, the switch latches off. The Power-OK status flag is set low, and the $\overline{FAULT}$ flag is set. If auto-retry is enabled, the switch remains off for a period t_{OFF}. If auto-retry is disabled, the switch remains latched off, and $\overline{FAULT}$ is low. Reset the latch and $\overline{FAULT}$ by driving corresponding ON_ low.

Applications Information

Considerations for circuit design include output capacitor requirements, current-limit requirements, setting the maximum on-time in current limit, and choosing a suitable MOSFET and on-time duty cycle in auto-retry.

Output Capacitor Requirements

The load capacitor requirements should be determined first, as this affects the required startup.

Current-Limit Requirements (Choosing R_{SENSE})

The current limit should be set to at least 20% higher than the expected full load current. If current limit is also used to control startup current, then set this limit high enough so that the output voltage can rise and settle before t_O elapses (see *Setting t_O* section below).

Setting t_O (Choosing R_{RTIM})

Choose the t_O time by connecting a 2kΩ to 40kΩ resistor from RTIM to DGND. The minimum 6.4ms t_O is set with R_{RTIM} = 2kΩ. The maximum 128ms t_O is set with R_{RTIM} = 40kΩ set according to the following equation:

$$t_O = (R_{RTIM} / 2k\Omega)\ (6.4ms).$$

t_O should be chosen appropriately, depending on the startup condition. There are two cases:

1) For startup without current limit, when

$$I = I_{GATE}\frac{C_L}{C_{GATE}} + I_L < \frac{V_{SC}}{R_{SENSE}}$$

the startup current does not reach the maximum current-limit threshold and t_O will not activate during startup condition. In this case, set t_O to a small value, but large enough to allow the switch to remain

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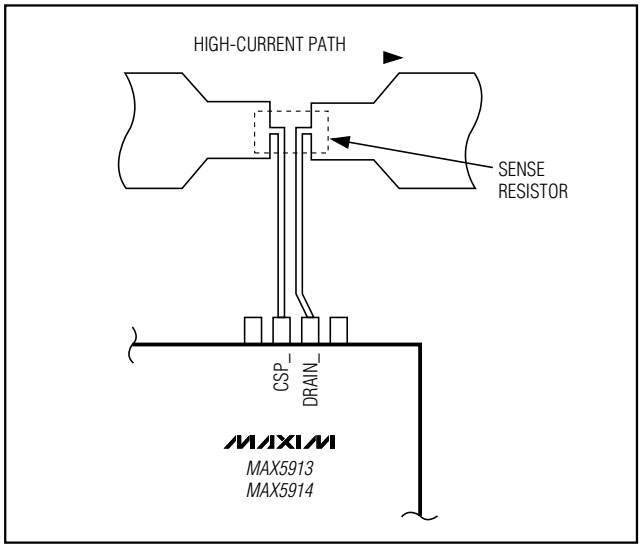


Figure 7. Recommended Layout for Kelvin-Sensing Current Through Sense Resistor

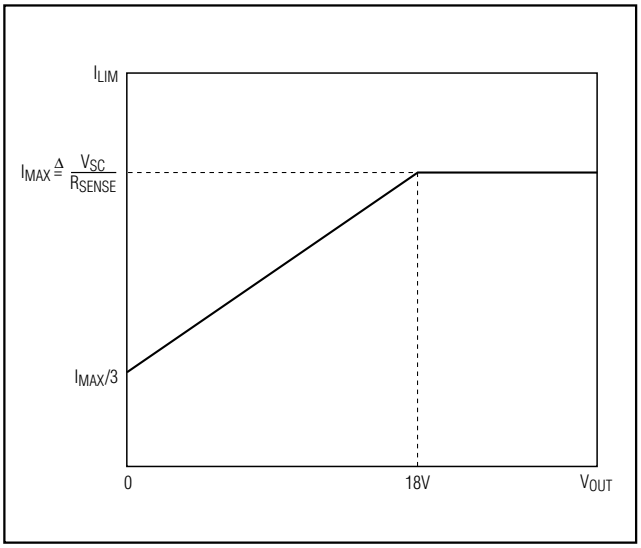


Figure 8. Foldback Current-Limit Response

on during large output load-current transients. The smaller the t_O, the faster the MAX5913/MAX5914 turn off the external FET in case of output overload or short-circuit condition.

2) For startup with current limit, when

$$I = I_{GATE}\left(\frac{C_L}{C_{GATE}} + I_L\right) \geq \frac{V_{SC}}{R_{SENSE}}$$

which is expected when

$$\frac{C_L}{C_{GATE}}$$

is large, t_O must be set to be long enough to allow the output voltage to rise and settle before t_O elapses. In this case, t_O must satisfy the following equation:

$$t_O = C_L \frac{18}{\frac{2}{3} I_{MAX} - I_L} + C_L \frac{V_{CC} - 18V}{I_{MAX} - I_L}$$

where V_{CC} is the input voltage and given that $I_L < I_{LIM}$.

Choosing Power MOSFET

The FET must withstand a short-circuit condition where its power dissipation is $P_{DISS} = V_{CC} \times I_{LIM}$. The FET must have sufficient thermal capacitance to prevent thermal heating damage during the t_O time.

Table 2. Duty Programming Cycle

DC	t_{OFF}	DUTY CYCLE
0	$99 \times t_O$	1%
1	$49 \times t_O$	2%
Open	$24 \times t_O$	4%

Choose Duty Cycle (setting DC)

The duty cycle can be adjusted to allow time for heat to dissipate between t_O cycles, allowing use of smaller MOSFETs with lower thermal capacitance. For smaller duty cycle, a smaller FET is sufficient. See Table 2 for setting the duty cycle.

The auto-retry off-time should not be too long to keep system wait time during retry period to a reasonable value. For example, when t_O is set to 128ms and duty cycle is set to 1%, the retry time is 99 × 128ms = 12.7s.

Application Circuits

In a typical LAN system there are two ways to deliver power over the LAN cable. Power can be supplied to the unused cable pairs, or power can be supplied over the signal pairs (Figures 9 and 10).

Chip Information

TRANSISTOR COUNT: 14,622

PROCESS: BiCMOS

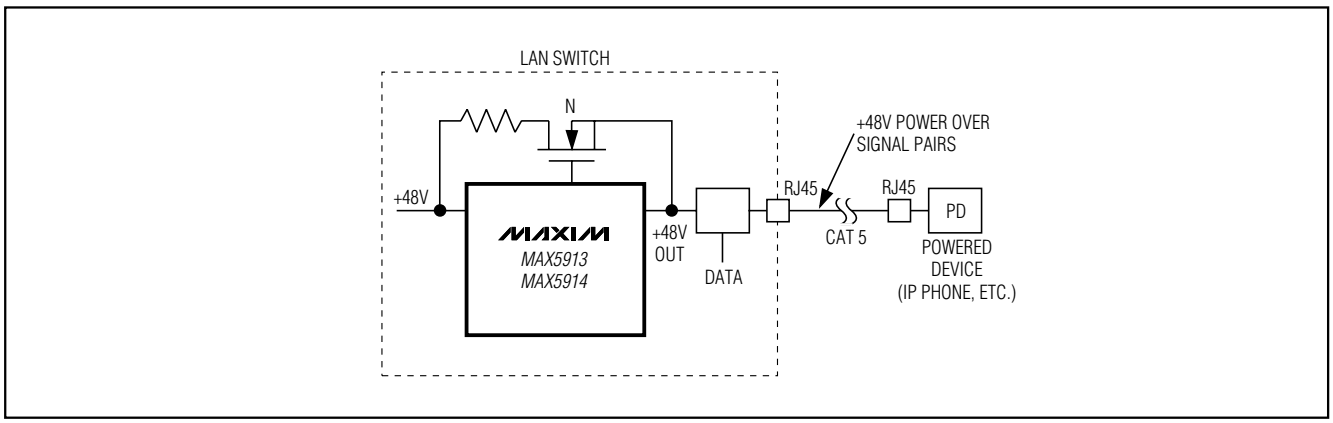


Figure 9. Power Sent Over Signal Pairs

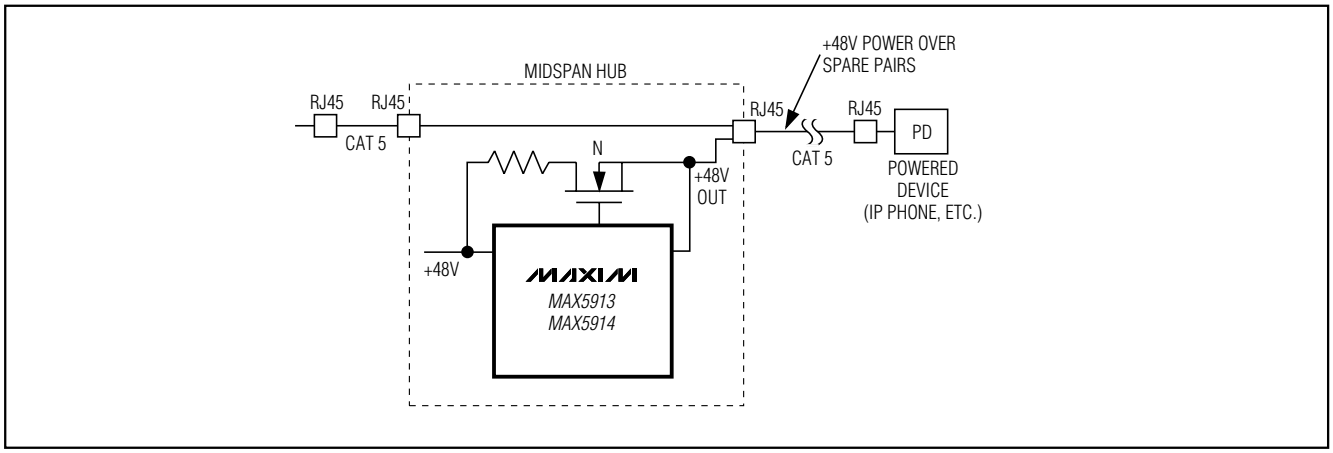
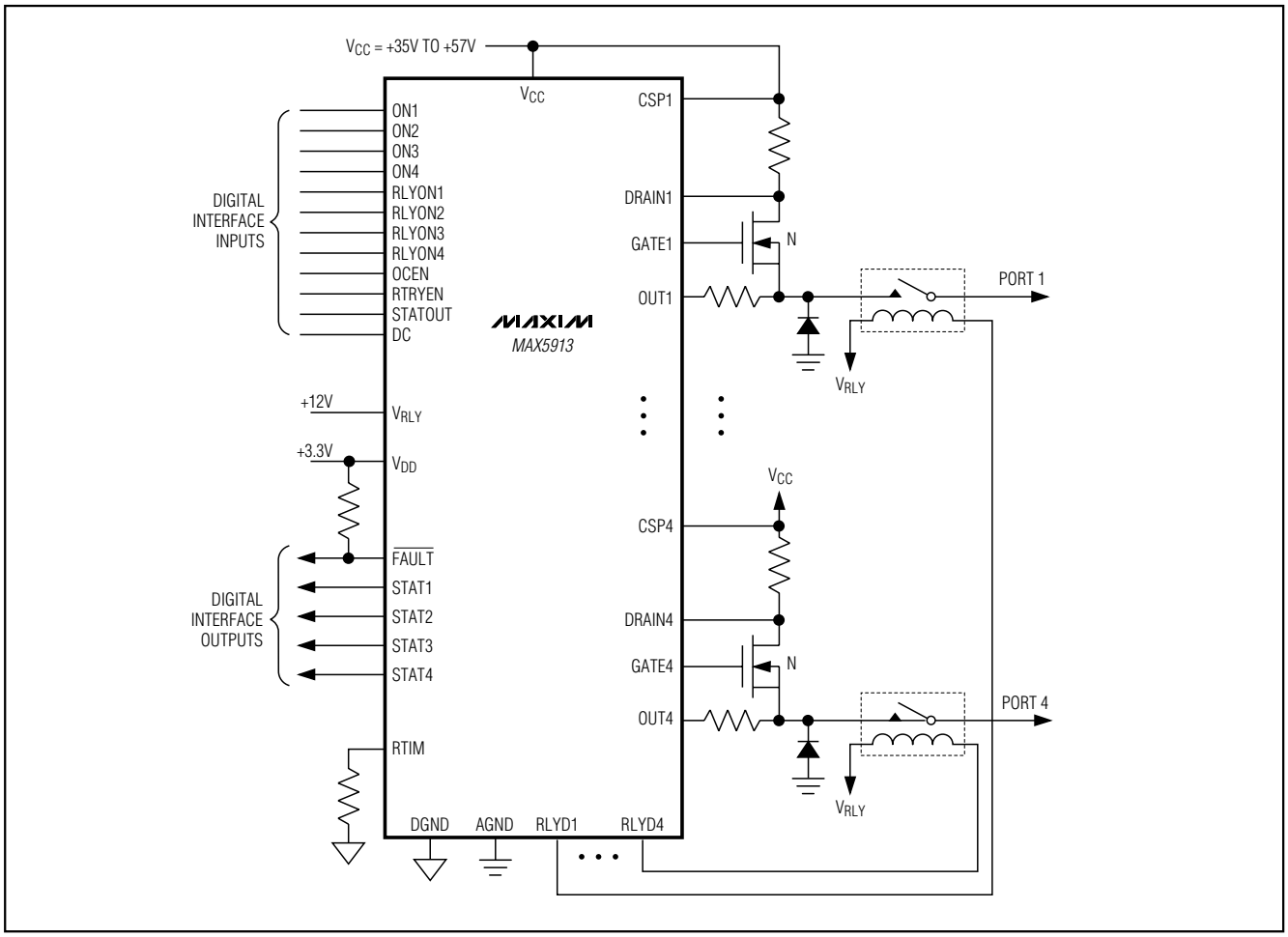


Figure 10. Power Sent Over Spare Pairs

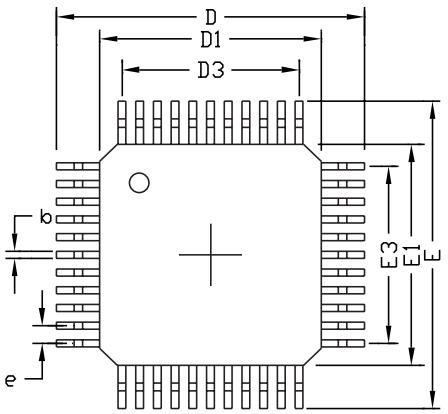
+48V Quad Hot-Swap Controllers For Power-Over-LAN

Typical Operating Circuit

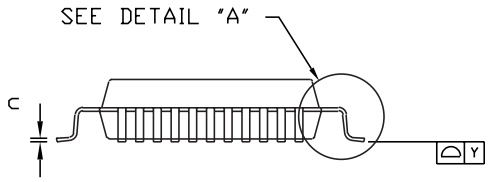


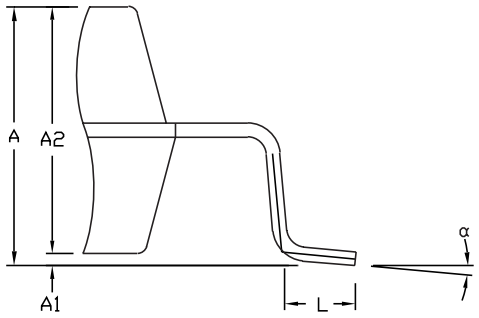
Package Information

MQFP44.EPS



	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.032	2.388	0.080	0.094
A1	0.102	0.254	0.004	0.010
A2	1.930	2.134	0.076	0.084
b	0.305	0.457	0.012	0.018
c	0.102	0.254	0.004	0.010
D	12.954	13.462	0.510	0.530
D1	9.906	10.109	0.390	0.398
D3	8.000 REF		0.315 REF	
E	12.954	13.462	0.510	0.530
E1	9.906	10.109	0.390	0.398
E3	8.000 REF		0.315 REF	
e	0.800 REF		0.0315 REF	
L	0.635	0.940	0.025	0.037
α	°0	°10	°0	°10





DETAIL "A"

NOTES:

1. D1&E1 DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .254mm(.010").
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC MO-108-AA-2.

MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, MQFP, 44L

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0826	C	1/1