RELIABILITY REPORT

FOR

MAX521xxxx

PLASTIC ENCAPSULATED DEVICES

November 28, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX521 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX521 is a octal, 8-bit voltage-output digital-to-analog converter (DAC) with simple a 2-wire serial interface that allows communication between multiple devices. This device operates from a single +5V supply and its reference input range includes both supply rails.

The MAX521 includes rail-to-rail output buffer amplifiers for reduced system size and component count when driving loads.

The MAX521 features a serial interface and internal software protocol, allowing communication at data rates up to 400kbps. The interface, combined with the double-buffered input configuration, allows the DAC registers to be updated individually or simultaneously. In addition, the device can be put into a low-power shutdown mode that reduces supply current to 4µA. Power-on reset ensures the DAC outputs are at 0V when power is initially applied.

B. Absolute Maximum Ratings

Item	Rating
V_{DD} to DGND	-0.3V to +6V
V_{DD} to AGND	-0.3V to +6V
OUT_	-0.3V to (V_{DD} + 0.3V)
REF_	-0.3V to (V_{DD} + 0.3V)
AD0, AD1, AD2	-0.3V to (V_{DD} + 0.3V)
SCL, SDA to DGND	-0.3V to +6V
AGND to DGND	-0.3V to +0.3V
Maximum Current to Any Pin	50mA
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
24-Pin WSO	941mW
20-Pin PDIP	889mW
24-Pin SSOP	640mW
Derates above +70°C	
24-PIN WSO	11.76mW/°C
20-Pin PDIP	11.11W/°C
24-Pin SSOP	8.0mW/°C

II. Manufacturing Information

A. Description/Function:	Octal, 2-Wire Serial 8-Bit DAC with Rail-to-Rail Outputs
B. Process:	S3 -Standard 3 micron silicon gate CMOS
C. Number of Device Transistors:	4518
D. Fabrication Location:	California or Oregon, USA
E. Assembly Location:	Philippines, Malaysia, or Korea
F. Date of Initial Production:	April, 1995

III. Packaging Information

A. Package Type:	24-Lead SSOP	24-Lead WSO	20-Pin PDIP
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	#05-0401-0424	#05-0401-0423	#05-0401-0422
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0

IV. Die Information

A. Dimensions:	125 x 212 mils
B. Passivation:	SiN/SiO (nitride/oxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 179 \times 2}$$

(Chi square value for MTTF upper limit)

↳ Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 6.07 \times 10^{-9}$

λ = 6.07 F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5104) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The DA55 die type has been found to have all pins able to withstand a transient pulse of ± 1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±100mA and/or ±20V.

Table 1
Reliability Evaluation Test Results
MAX521xxxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		179	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	PDIP SSOP WS	260 200 220	0 2 2
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality (generic test vehicle)		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters (generic test vehicle)		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Shrink Small Outline package.
Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

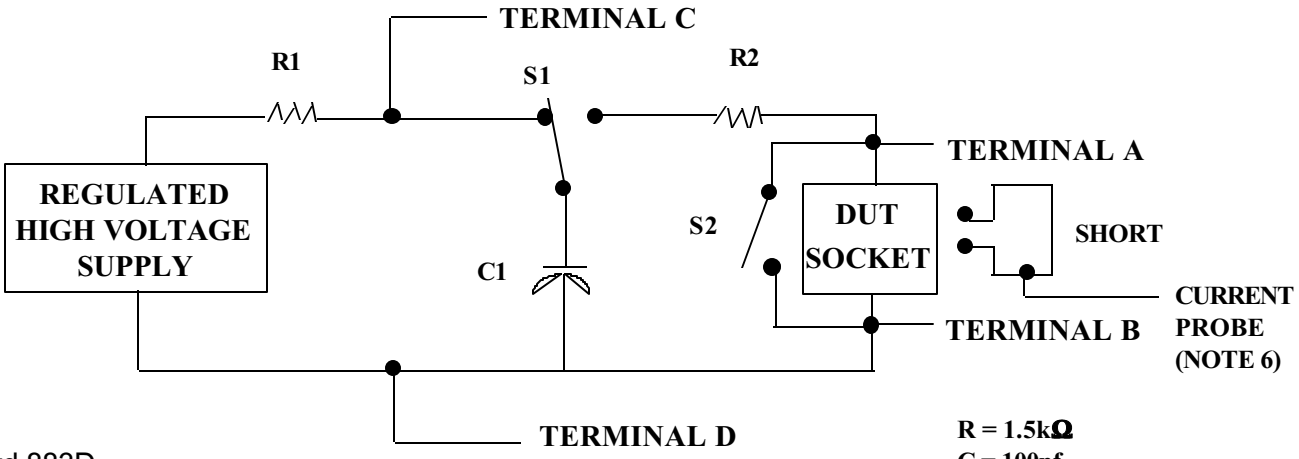
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

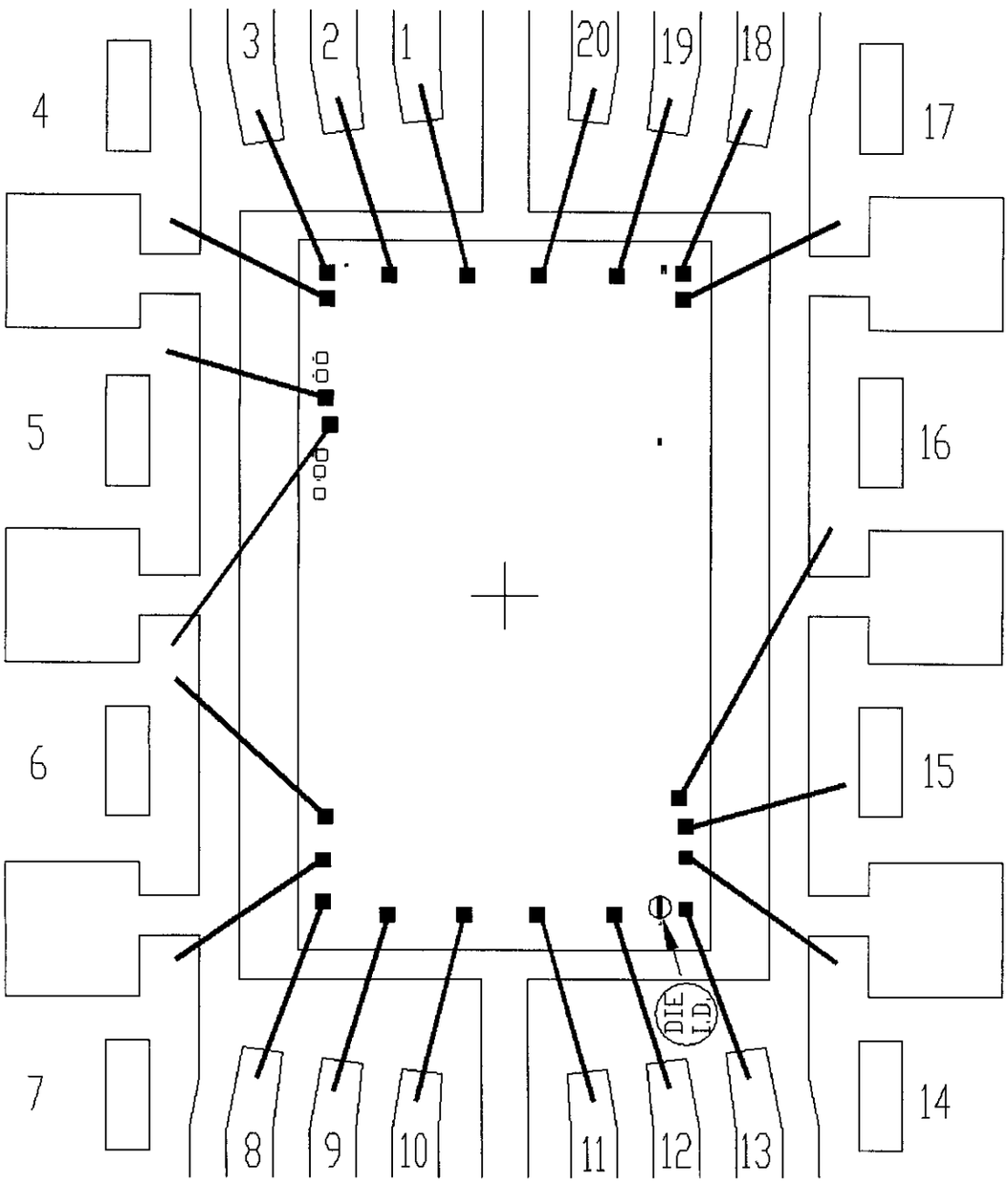
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

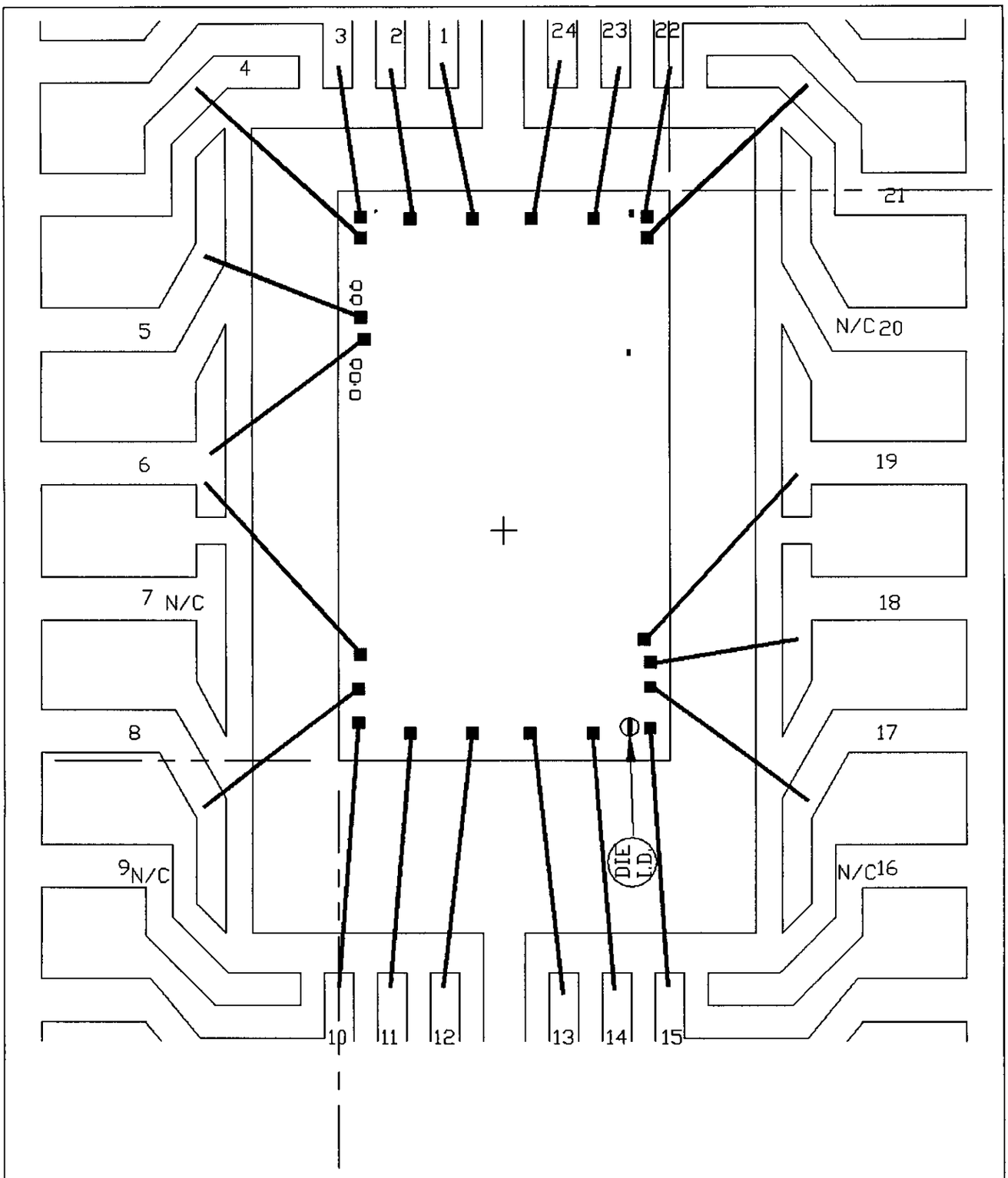
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



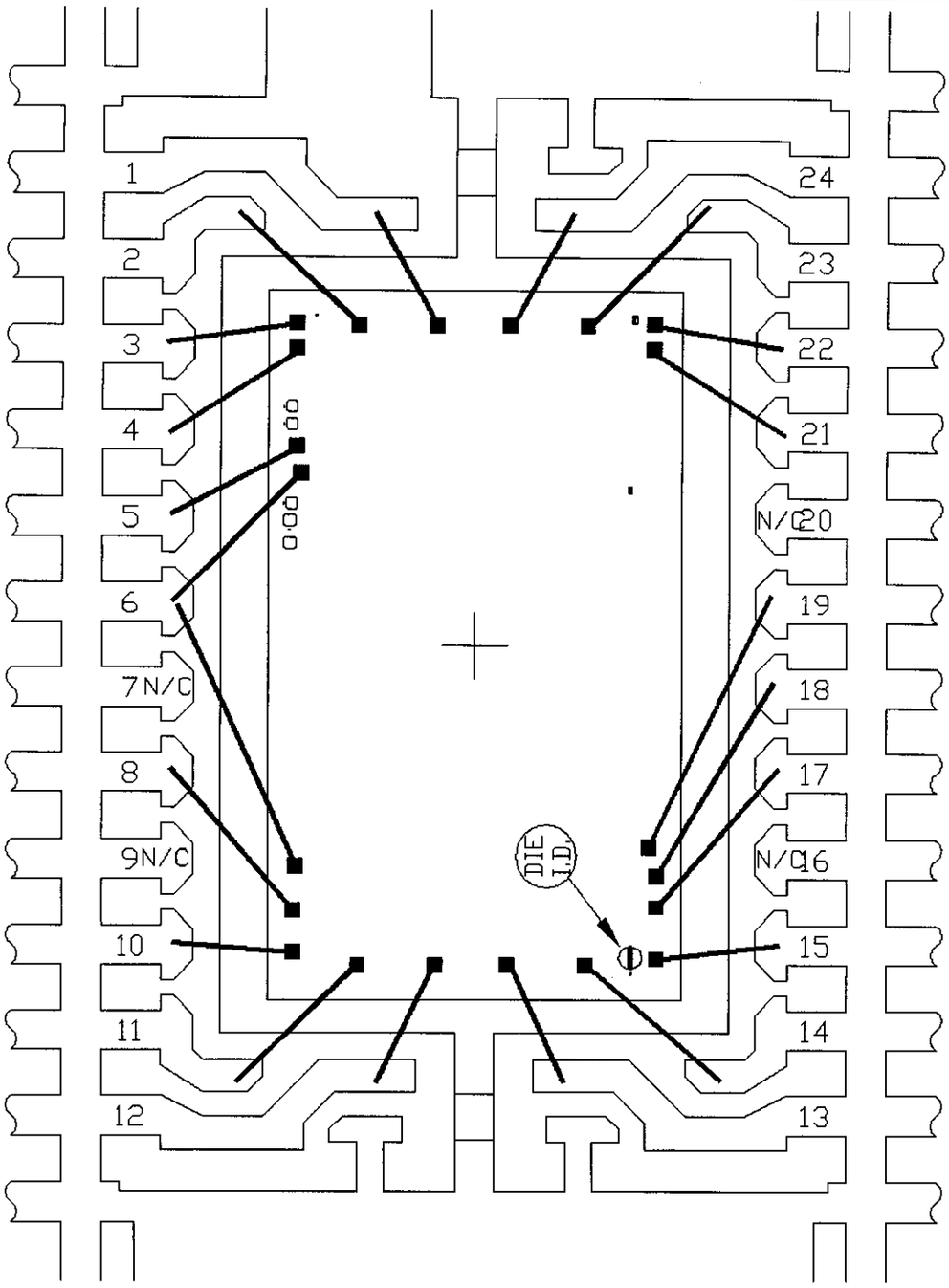
Mil Std 883D
Method 3015.7
Notice 8



PKG.CODE: P20-2		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 160 X 230	PKG.	AKhai	12/6/94	BUILDSHEET NUMBER: 05-0401-0422	REV.: A
	DESIGN		12/19/94		



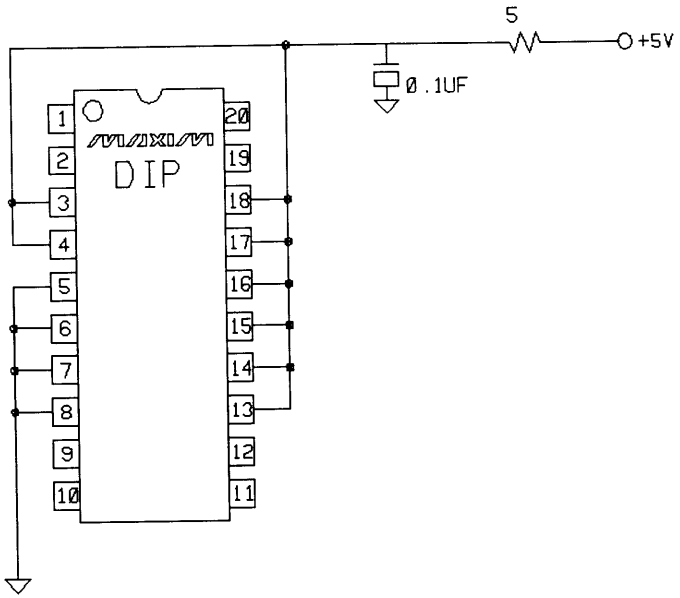
PKG.CODE: W24-3		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 190X300	PKG.	A Shai	12/13/94	BUILDSHEET NUMBER: 05-0401-0423	REV.: A
	DESIGN		12/19/94		



PKG.CODE: A24-3		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 154X232	PKG.		12/6/94	BUILDSHEET NUMBER: 05-0401-0424	REV.: A
	DESIGN		12/19/94		

ONCE PER BOARD

ONCE PER DEVICE



+5V I = 20mA

100UF

PS2 I=

PS3 I =

PS4 I=

PS5 I =

PS6 I =

CLKØ FREQ= AMP=

CLK1 FREQ= AMP=

CLK2 FREQ= AMP=

CLK3 FREQ= AMP=

CLK4 FREQ= AMP=

GND

- STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
- BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL
   [X] HR/883

SPEC. NO. Ø6-5104 REV: A

DATE: 1/17/95

DRAWN BY: C. JONES

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE(S):

MAX521