RELIABILITY REPORT

FOR

MAX4685Exx

CHIP SCALE & PLASTIC ENCAPSULATED DEVICES

January 12, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX4685 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4685 low on-resistance (R_{ON}), low-voltage, dual single-pole/double-throw (SPDT) analog switche operates from a single +1.8V to +5.5V supply. The MAX4685 features a 0.8 max on-resistance for both NO and NC switches at a +2.7V supply.

The part features break-before-make switching action (2ns) with t_{ON} = 50ns and t_{OFF} = 40ns at +3V. The digital logic inputs are 1.8V logic-compatible with a +2.7V to +3.3V supply.

The MAX4685 is packaged in the chipscale package (UCSP)™, significantly reducing the required PC board area. The chip occupies only a 2.13mm x 1.50mm area. The 4 x 3 array of solder bumps are spaced with a 0.5mm bump pitch.

B. Absolute Maximum Ratings

Item	Rating
V+, IN_ to GND	-0.3V to +6V
COM_, NO_, NC_ to GND (Note 1)	-0.3V to (V+ + 0.3V)
Continuous Current NO_, NC_, COM_	+/-150mA
Peak Current NO_,NC_,COM_	
(pulsed at 1ms, 10% Duty Cycle)	+/-300mA
Storage Temp. Range	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Bump Temperature (Soldering)	
Infrared (15s)	+220°C
Vapor Phase (60s)	+215°C
Power Dissipation	
12-Bump UCSP	909mW
10-Pin uMax	444mW
Derates above +70°C	
12-Bump UCSP	11.4mW/°C
10-Pin uMax	5.6mW/°C

II. Manufacturing Information

A. Description/Function:	0.8 Ohm Low-Voltage, Dual SPDT Analog Switches
B. Process:	TM50 (.5 micron Poly Gate)
C. Number of Device Transistors:	198
D. Fabrication Location:	Taiwan
E. Assembly Location:	Philippines, Malaysia, Arizona
F. Date of Initial Production:	January, 2001

III. Packaging Information

A. Package Type:	10-Lead uMax	12-Bump UCSB
B. Lead Frame:	Copper	N/A
C. Lead Finish:	Solder Plate	N/A
D. Die Attach:	Silver-filled Epoxy	N/A
E. Bondwire/Solder Bump:	Gold (1.3 mil dia.)	14 mil dia Solder Ball
F. Mold Material:	Epoxy with silica filler	N/A
G. Assembly Diagram:	# 05-1201-0202	#05-1201-0200
H. Flammability Rating:	Class UL94-V0	N/A
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions:	82 x 60 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/Cu/Si/Ti
D. Backside Metallization:	None
E. Minimum Metal Width:	.5 microns (as drawn)
F. Minimum Metal Spacing:	.5 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 79 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 13.57 \times 10^{-8}$ $\lambda = 13.57$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (#06-5629) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AH71-1 die type has been found to have all pins able to withstand a transient pulse of ± 200V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX4685Exx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	79	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic process/package data.

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

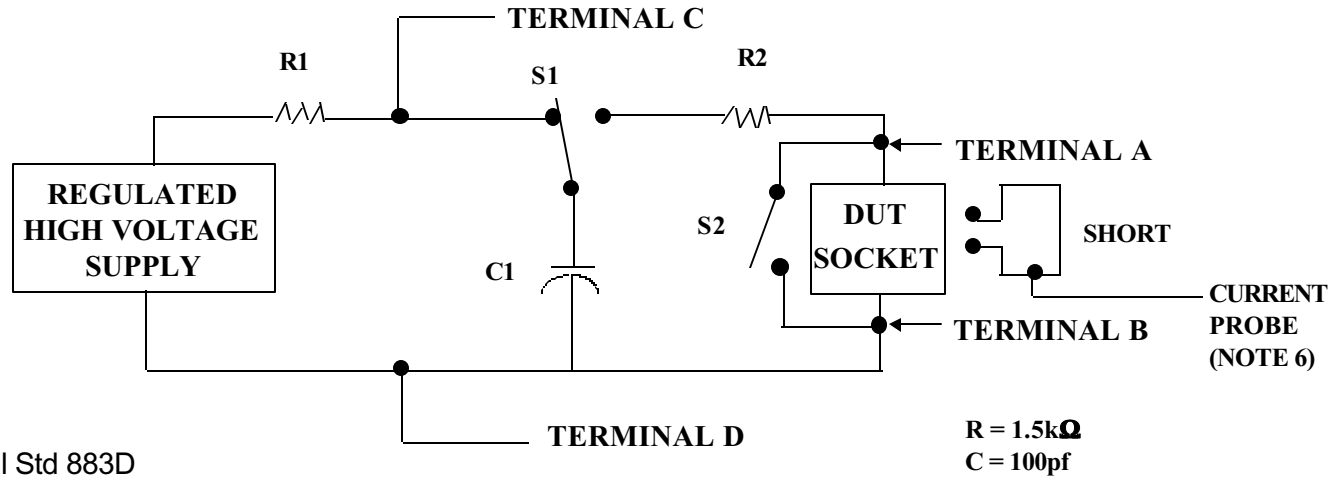
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

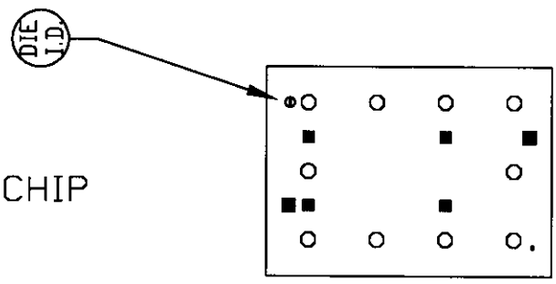
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

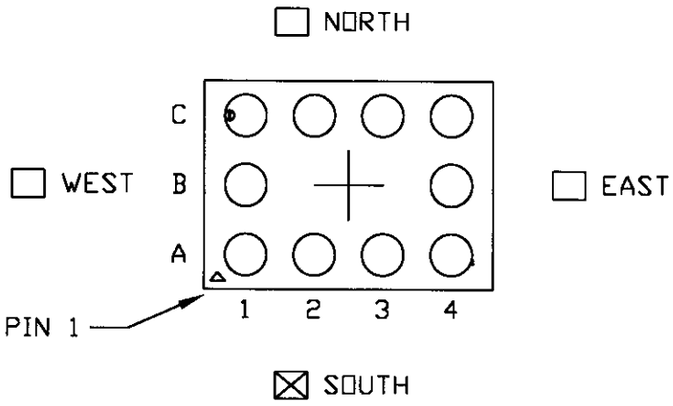
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8

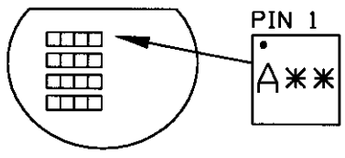


ORIGINAL CHIP



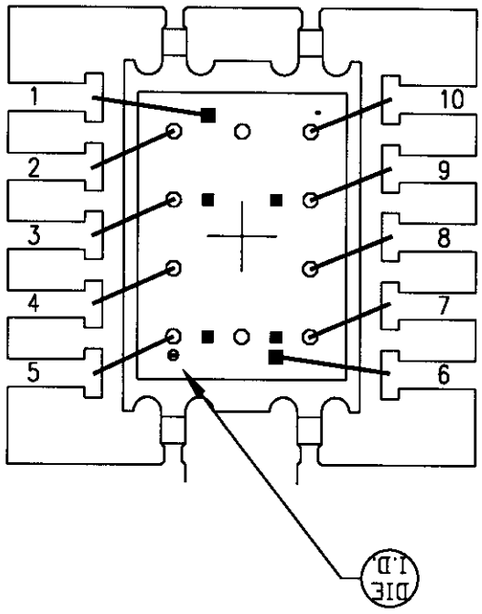
AFTER BUMP

SELECT THE BOX INDICATING THE WAFER FLAT SIDE
WITH RESPECT TO PIN 1.



PART MARKING ORIENTATION
IN REFERENCE TO WAFER FLAT
(MARK IS ON WAFER BACKSIDE)

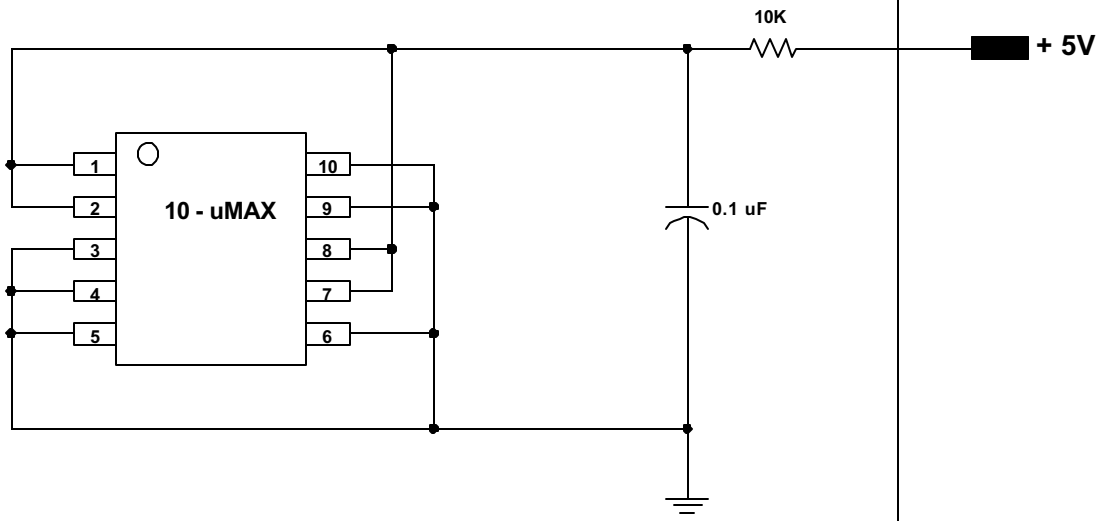
PKG. CODE: B12-4		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: N/A	PKG.		6/14/00	BOND DIAGRAM #: 05-1201-0202	REV: A
	DESIGN		6/14/00		



PKG. CODE: U10-2		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 68x94	PKG.		6/14/00	BOND DIAGRAM #: 05-1201-0200	REV: A
	DESIGN		6/15/00		

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX4684/4685

MAX. EXPECTED CURRENT = 100 uA

DRAWN BY: HAK TAN

NOTES: