RELIABILITY REPORT

FOR

MAX4642EUA

PLASTIC ENCAPSULATED DEVICES

September 4, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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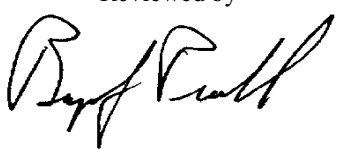
Reviewed by



Bryan J. Preeshl
Quality Assurance
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Conclusion

The MAX4642 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

The MAX4642 is a monolithic, dual, single-pole/single-throw (SPST) switch that can operate from a single supply ranging from +1.8V to +5.5V. The MAX4642 provides low 4-ohm on-resistance (R_{ON}), 0.6-ohm R_{ON} matching between channels, and 1-ohm R_{ON} flatness over the entire analog signal range. This device offers fast switching times of less than 20ns while consuming less than 0.01µW of quiescent power.

The MAX4642 has two normally closed (NC) switches. This device has low 0.35nA leakage current over the entire temperature range. The MAX4642 is available in small 8-pin µMAX packages.

B. Absolute Maximum Ratings

Item	Rating
V+	-0.3V to +6V
IN_, COM_, NO_, NC_ (Note 1)	-0.3V to (V+ + 0.3V)
Continuous Current (any terminal)	±20mA
Continuous Current (NO_, NC_, COM_)	±50Ma
Peak Current (NO_, NC_, COM_, pulsed at ims, 10% duty cycle)	±100mA
Operating Temp Range	-40^0C to $+85^0$C
Junction Temp	$+150^0$C
Storage Temp Range	-65^0C to $+150^0$C
Lead Temp Range (soldering, 10s)	$+300^0$C
Power Dissipation	
8 Lead uMax	362mW
Derates above +70°C	
8 Lead uMax	4.5mW/°C

II. Manufacturing Information

A. Description/Function:	1Ω, Low-Voltage, Single-Supply SPDT Analog Switch
B. Process:	TSMC50 (0.5 micron TSMC CMOS)
C. Number of Device Transistors:	105
D. Fabrication Location:	Taiwan
E. Assembly Location:	Malaysia or Philippines
F. Date of Initial Production:	January, 2000

III. Packaging Information

A. Package Type:	**8 Lead uMax**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1201-0160
H. Flammability Rating:	Class UL94-V0

IV. Die Information

A. Dimensions:	57 x 35 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al/Si/Cu (Aluminum/ Silicon/ Copper)
D. Backside Metallization:	None
E. Minimum Metal Width:	.5 micron as drawn
F. Minimum Metal Spacing:	.5 micron as drawn
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliablity Lab Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83 \quad \text{(Chi square value for MTTF upper limit)}}{192 \times 4389 \times 240 \times 2}$$

$\rightarrow$ Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 4.52 \times 10^{-9}$ $\lambda = 4.52$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. #5509) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AH42Y-1 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX4642EUA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	240	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the uMax package.
Note 2: Generic package/process data

Attachment #3

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

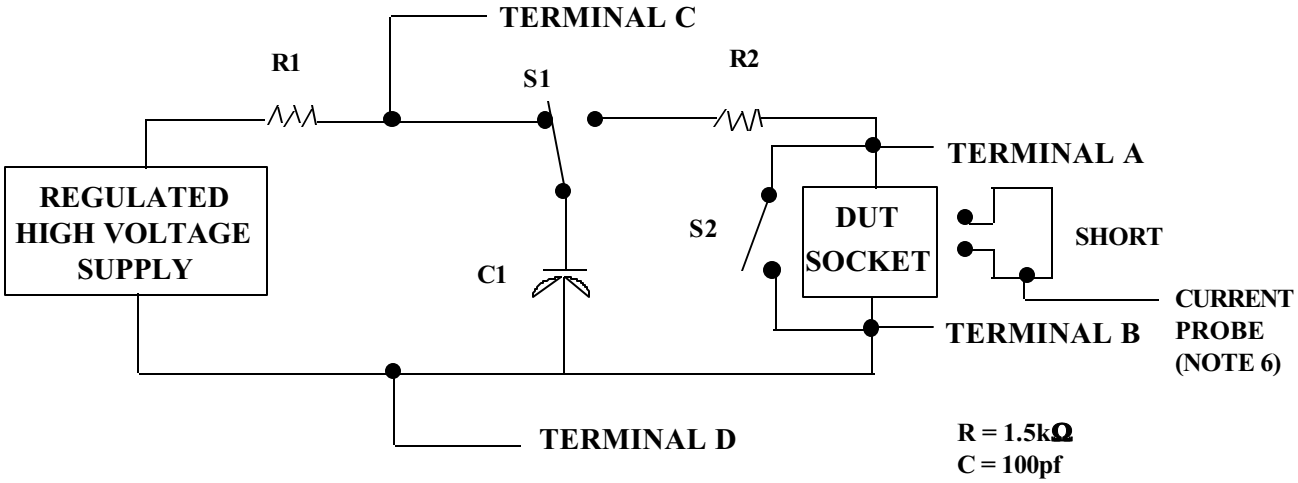
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

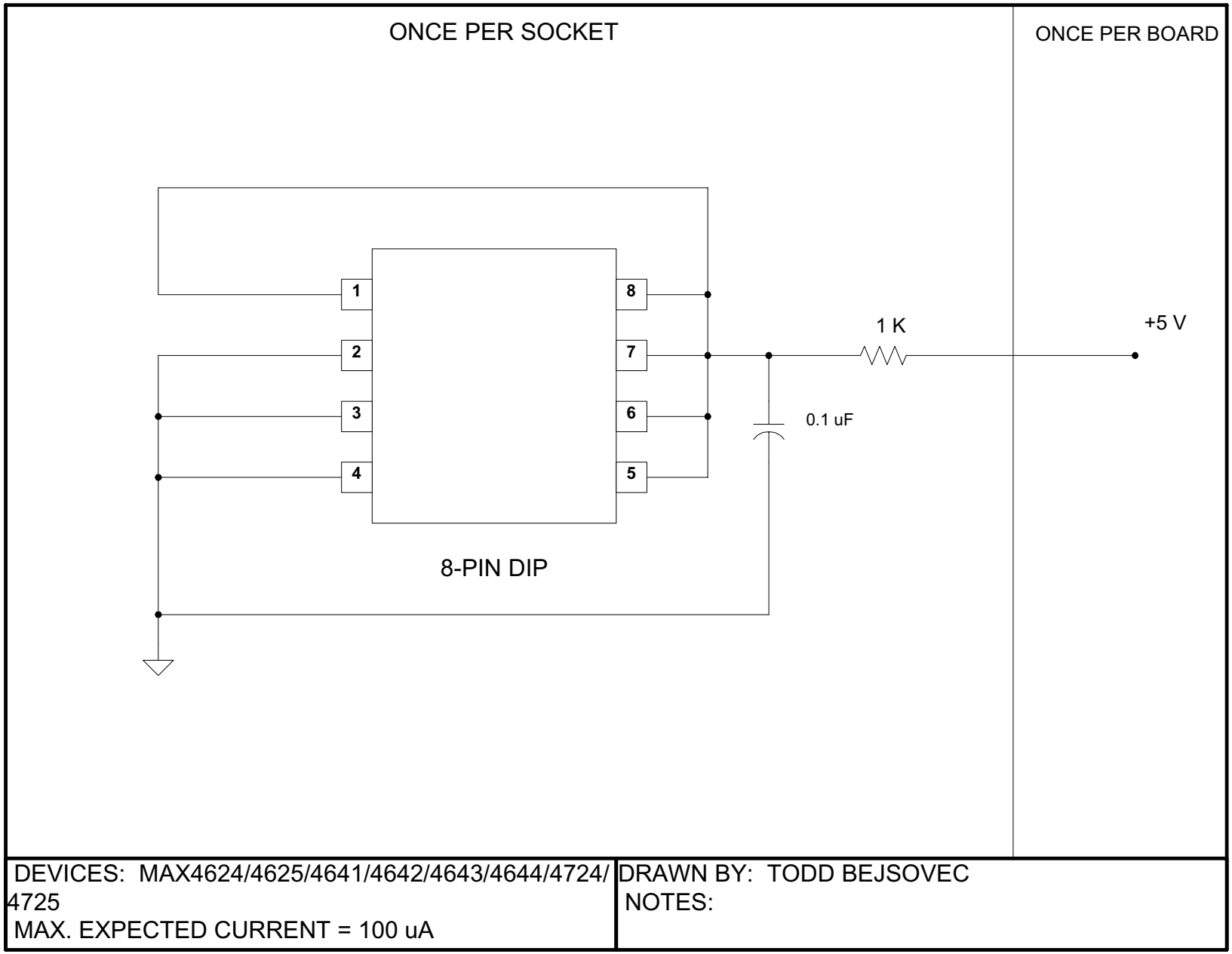
3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.





DEVICES: MAX4624/4625/4641/4642/4643/4644/4724/4725 MAX. EXPECTED CURRENT = 100 uA	DRAWN BY: TODD BEJSOVEC NOTES: