RELIABILITY REPORT

FOR

MAX4561EUT

PLASTIC ENCAPSULATED DEVICES

January 21, 2002

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX4561 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4561 is a low-voltage, ESD-protected analog switch. The normally open (NO) and normally closed (NC) inputs are protected against ±15kV electrostatic discharge (ESD) without latchup or damage, and the COM input is protected against 2.5kV ESD.

This switch operates from a single +1.8V to +12V supply. The 70 ohms at 5V (120 ohms at 3V) on-resistance is matched between channels to 2 ohms max, and is flat (4 ohms max) over the specified signal range. The switch can handle Rail-to-Rail ® analog signals. Off-leakage current is only 0.5nA at +25°C and 5nA at +85°C. The digital input has +0.8V to +2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single +5V supply. The MAX4561 is a single-pole/double-throw (SPDT) switch.

The MAX4561 is available in a 6-pin SOT23 package.

B. Absolute Maximum Ratings

Item	Rating
V+ to GND	-0.3V to 13V
IN, COM, NO, NC to Gnd	-0.3V to (V+ 0.3V)
Continous Current (any terminal)	+/-10mA
Peak Current (NO,NC, COM pulsed at 1ms 10% duty cycle)	+/-30mA
ESD Protection per method IEC 1000-4-2 (NO,NC)	
Air-Gap Discharge	+/-15kV
Contact Discharge	+/-8kV
ESD Protection per Method 3015.7	
V+, GND, IN, COM	+/-2.5kV
NO, NC	+/-15kV
Junction Temperature	+150°C
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Continous Power Dissipation (T_A = +70^{0}C)	
6 Lead SOT	696mW
Derates above +70°C	
6 Lead SOT	8.7mW/°C

II. Manufacturing Information

A. Description/Function:	+15kV ESD-Protected, Low-Voltage, SPDT CMOS Analog Switch
B. Process:	S3 (SG3) Standard 3 micron silicon gate CMOS
C. Number of Device Transistors:	69
D. Fabrication Location:	Oregon or California, USA
E. Assembly Location:	Malaysia
F. Date of Initial Production:	July, 2000

III. Packaging Information

A. Package Type:	**6-Lead SOT34**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-1201-0167
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	61 x 42 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{4.04}{192 \times 4389 \times 80 \times 2}$$ (Chi square value for MTTF upper limit)

↳ Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 29.97 \times 10^{-9}$ $\lambda = 29.97$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. # 06-5560) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The AH52 die type has been found to have all pins able to withstand a transient pulse of ±2500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX4561EUT

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	80	1
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality (generic test vehicle)	99	1
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality (generic test vehicle)	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters (generic test vehicle)	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the uMax package.
Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

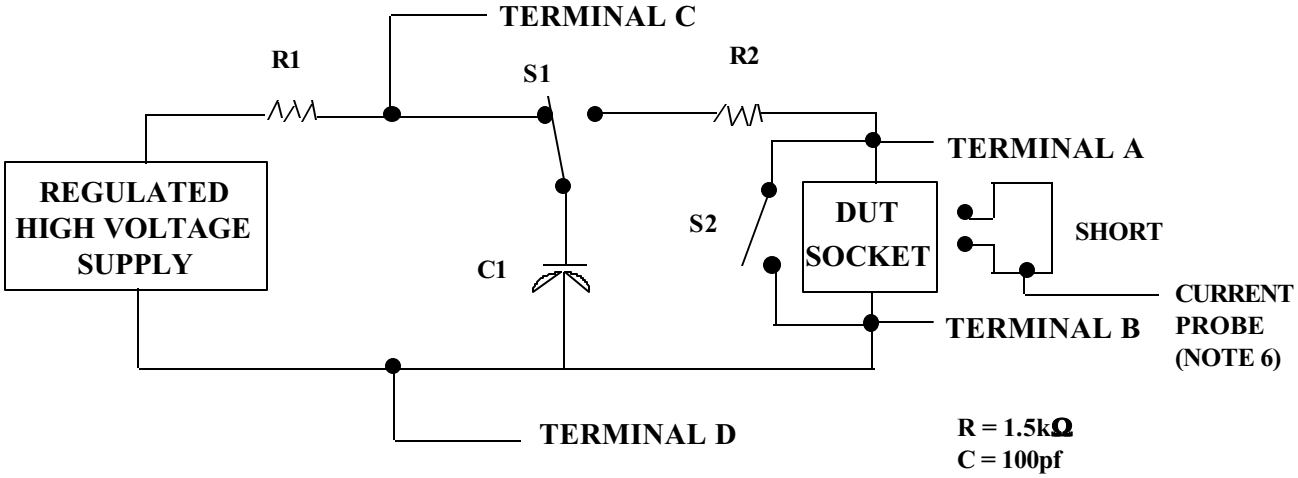
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

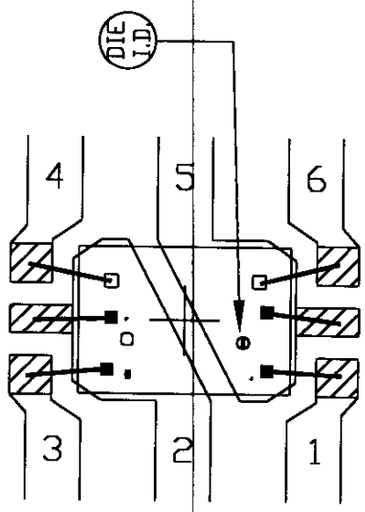
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8

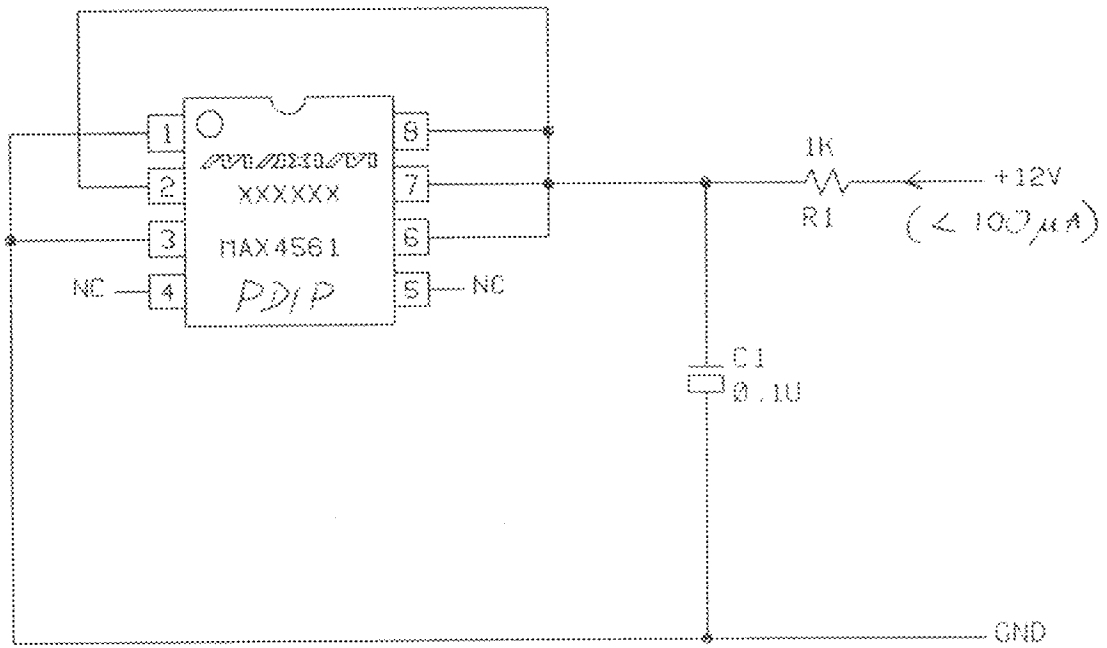


NOTE: USE NON-CONDUCTIVE EPOXY ONLY

BONDABLE AREA

PKG. CODE: U6S-3		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 64x46	PKG.		1/10/00	BOND DIAGRAM #: 05-1201-0167	REV: A
	DESIGN		1/20/00		

BURN-IN BOARD SCHEMATIC



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