RELIABILITY REPORT

FOR

MAX4544xxx

PLASTIC ENCAPSULATED DEVICES

October 10, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by

Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX4544 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX4544 is a precision, dual analog switch designed to operate from a single +2.7V to +12V supply. Low power consumption (5µW) makes this part ideal for battery-powered equipment. This switch offers low leakage currents (100pA max) and fast switching speeds (t_{ON} = 150ns max, t_{OFF} = 100ns max).

When powered from a +5V supply, the MAX4544 offers 2 ohm max matching between channels, 60 ohm max on-resistance (R_{ON}), and 6 ohm max R_{ON} flatness. This switch also offers 5pC max charge injection and a minimum of 2000V ESD protection per Method 3015.7. The MAX4544 is a single-pole/double-throw (SPDT) device.

B. Absolute Maximum Ratings

Item	Rating
Voltage Referenced to GND	
V+	-0.3V to +13V
IN_, COM_, NC_, NO_ (Note 1)	-0.3V to (V+ +0.3V)
Continuous Current (any terminal)	±10mA
Peak Current, COM_, NO_, NC_	
(pulsed at 1ms, 10% duty cycle max)	±20mA
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
8-Lead NSO	471mW
6-Lead SOT-23	571mW
8-Lead uMax	330mW
8-Lead PDIP	727mW
Derates above +70°C	
8-Lead NSO	5.88mW/°C
6 Lead SOT-23	7.1mW/°C
8 Lead uMax	4.10mW/°C
8 Lead PDIP	9.09mW/°C

Note 1: Signals on NC, NO, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maxim current rating.

II. Manufacturing Information

A. Description/Function:	Low-Voltage, Single-Supply Dual SPDT Analog Switch
B. Process:	S3 (Standard 3 micron silicon gate CMOS)
C. Number of Device Transistors:	76
D. Fabrication Location:	Oregon or California, USA
E. Assembly Location:	Philippines, Malaysia, Thailand or Korea
F. Date of Initial Production:	February, 1997

III. Packaging Information

A. Package Type:	**8-Lead NSO**	**6-Lead SOT-23**	**8-Lead uMax**	**8-Lead PDIP**
B. Lead Frame:	Copper	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	# 05-1201-0010	# 05-1201-0008	# 05-1201-0011	# 05-1201-0009
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0	Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions:	57 x 32 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	3 microns (as drawn)
F. Minimum Metal Spacing:	3 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 240 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 4.52 \times 10^{-9}$

$\lambda = 4.52$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80-piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5318) shows the static Burn-In circuit. Maxim also performs quarterly 1000-hour life test monitors. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The AH02-3 die type has been found to have all pins able to withstand a transient pulse of ± 2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results
MAX4544xSA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		80	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 96hrs.	DC Parameters & functionality	NSO PDIP SOT uMAX	2339 600 99 195	17 0 0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality (generic test vehicle)		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters (generic test vehicle)		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Small Outline package.
Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

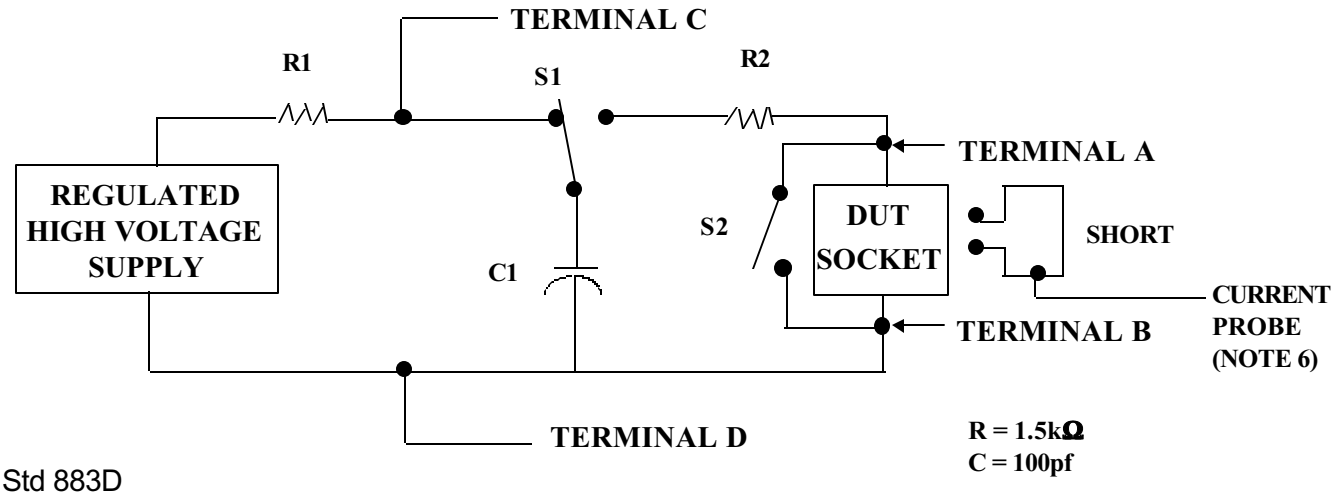
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

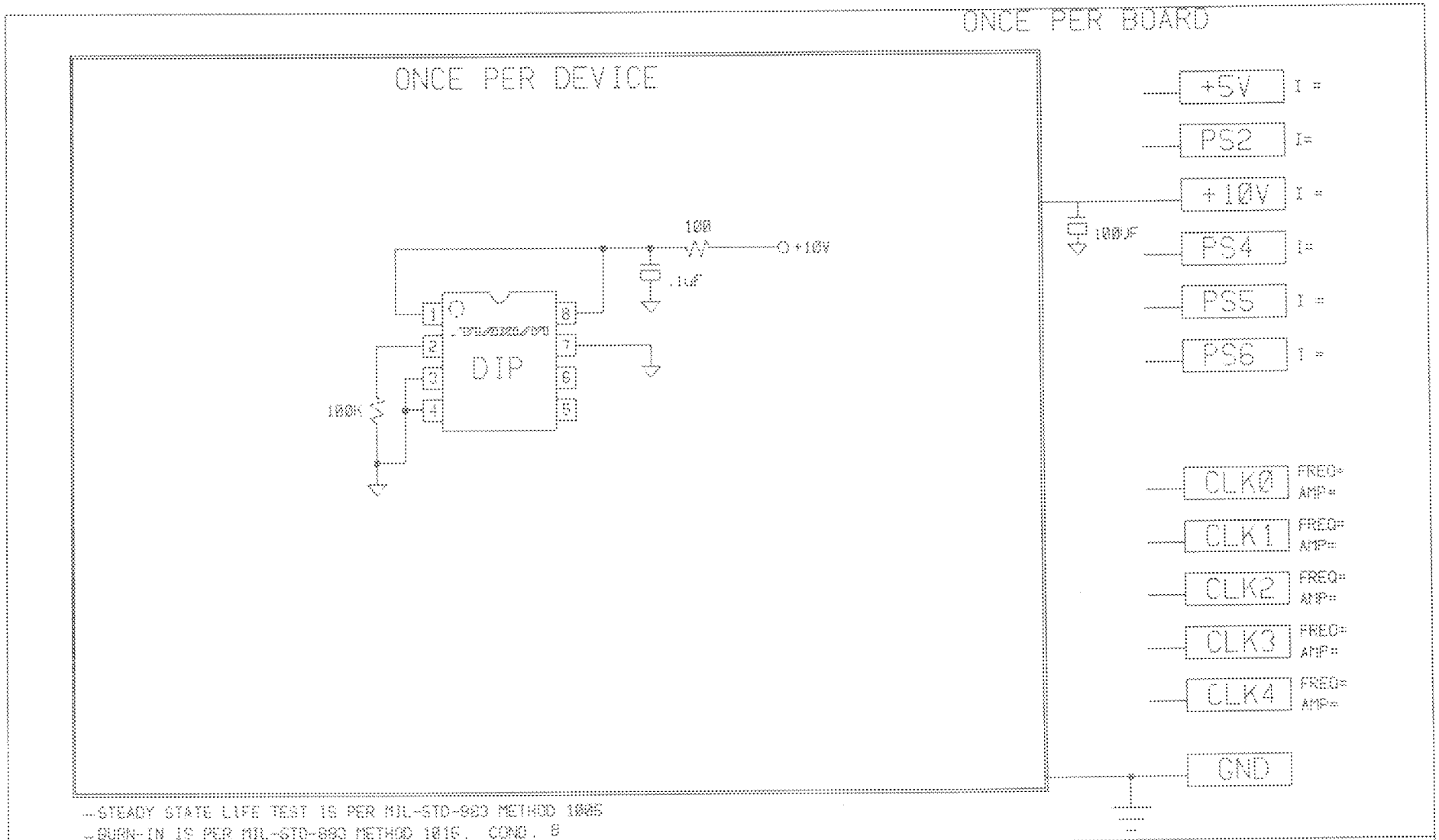
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



-STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005
-BURN-IN IS PER MIL-STD-883 METHOD 1015, COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150K CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL
   [X] MIL/883

SPEC. NO. 06-5318 REV: A

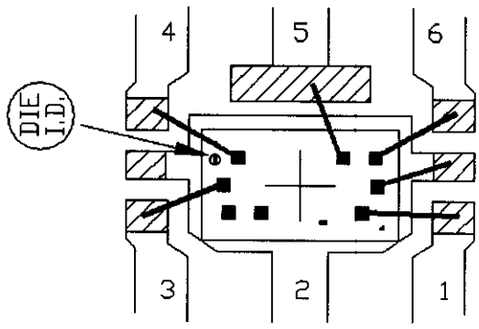
DATE: 10/14/97

DRAWN BY: R. TARIGA

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE(S):

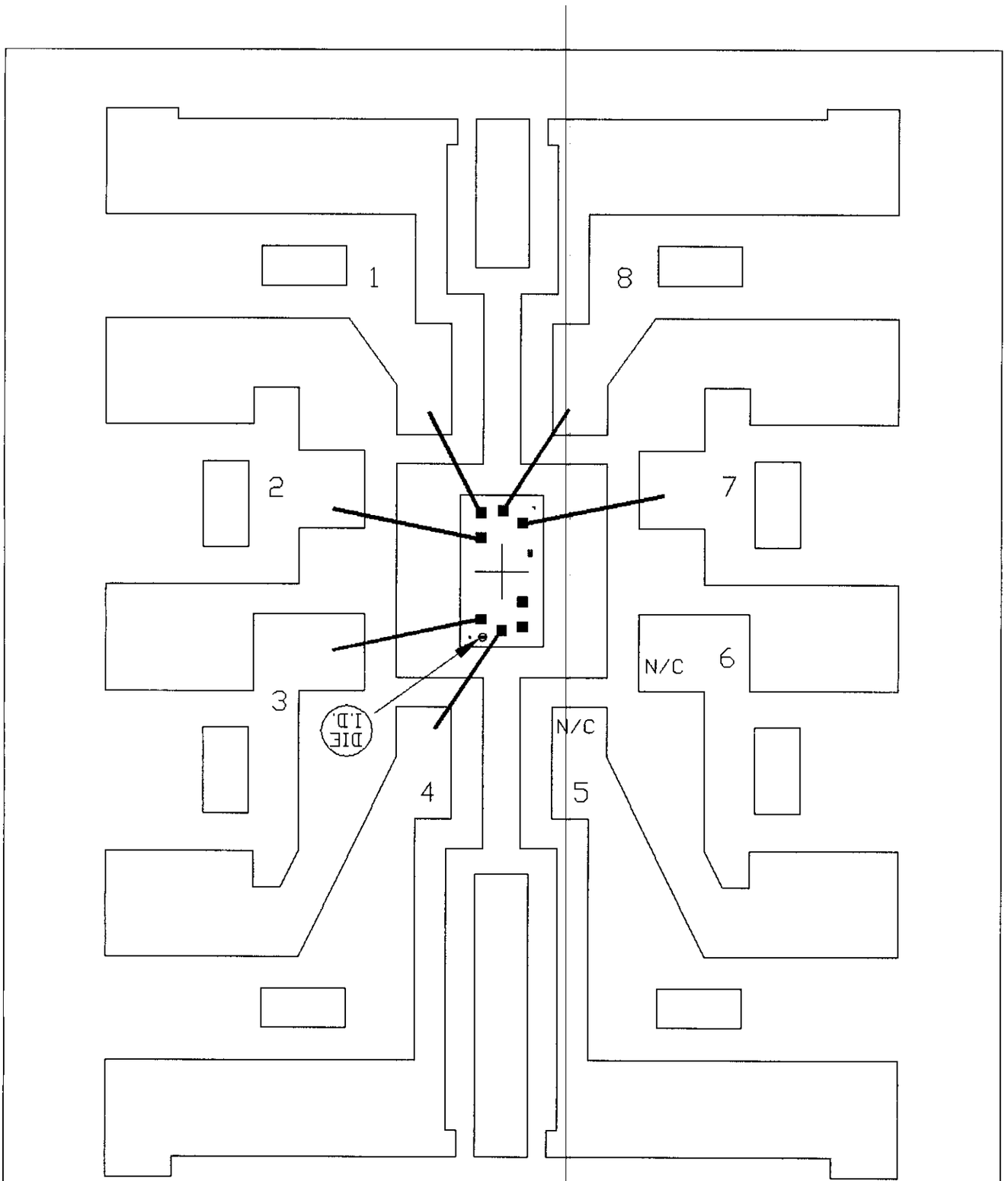
MAX4544



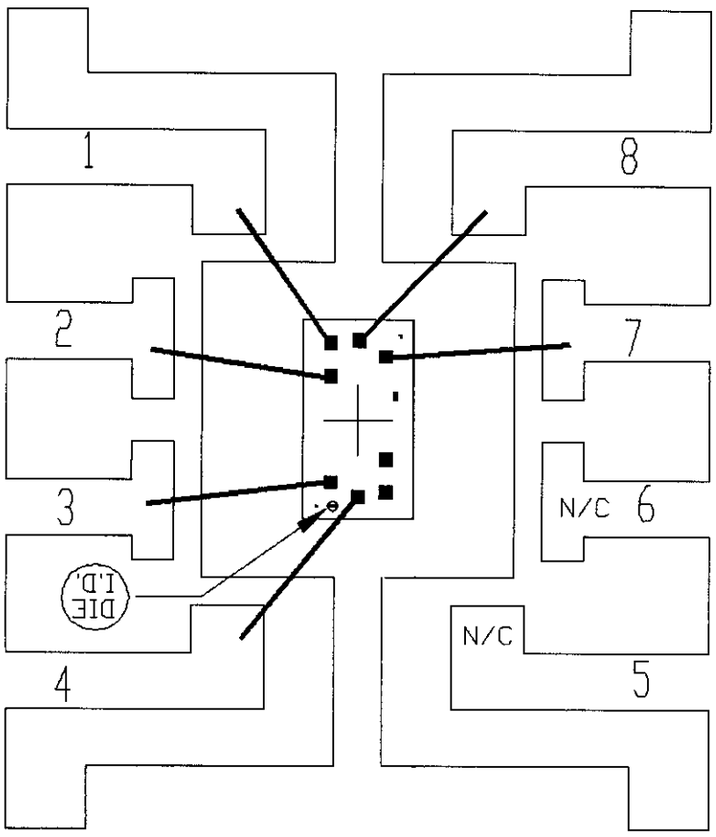
▨ - BONDING AREA

NOTE: CAVITY DOWN

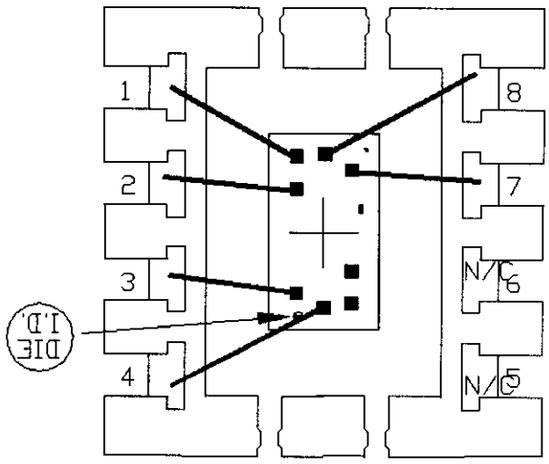
PKG.CODE: U6-1		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 64X39	PKG.	SVC	JAN 0 6 1997	BUILDSHEET NUMBER: 05-1201-0008	REV.: A
	DESIGN	JJ	1-7-97		



PKG.CODE: P8-5		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 80X80	PKG.	SVC	JAN 0 9 1997	BUILDSHEET NUMBER: 05-1201-0009	REV.: A
	DESIGN		1-9-97		



PKG.CODE: S8-2		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 90 X 90	PKG.	JAN 09 1997		BUILDSHEET NUMBER: 05-1201-0010	REV.: A
	DESIGN		1-9-97		



PKG.CODE: U8-1		APPROVALS	DATE	MAXIM
CAV./PAD SIZE: 68X94	PKG.	SVC	JAN 0 9 1997	BUILDSHEET NUMBER: 05-1201-0011
	DESIGN		1-9-97	REV.: A