

RELIABILITY REPORT  
FOR  
**MAX4541xxA**  
PLASTIC ENCAPSULATED DEVICES

September 10, 2001

**MAXIM INTEGRATED PRODUCTS**

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by



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Reviewed by



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Executive Director

## Conclusion

The MAX4541 Successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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### I. Device Description

#### A. General

The MAX4541 is a precision, dual analog switch designed to operate from a single +2.7V to +12V supply. Low power consumption (5 $\mu$ W) makes this part ideal for battery-powered equipment. This switch offers low leakage currents (100pA max) and fast switching speeds (tON = 150ns max, tOFF = 100ns max). When powered from a +5V supply, the MAX4541 offers 2max matching between channels, 60 max on-resistance (RON), and 6max RON flatness. This switch also offers 5pC max charge injection and a minimum of 2000V ESD protection per Method 3015.7. The MAX4541 is a dual single-pole/single-throw (SPST) device. The MAX4541 has two normally open (NO) switches .

#### B. Absolute Maximum Ratings

<u>Item</u>	<u>Rating</u>
Voltage Referenced to GND	
V+	-0.3V to +13V
IN_, COM_, NC_, NO_ (Note 1)	-0.3V to (V+ + 0.3V)
Continuous Current (any terminal)	$\pm$ 10mA
Peak Current, COM_, NO_, NC_ (pulsed at 1ms, 10% duty cycle max)	$\pm$ 20mA
ESD per Method 3015.7	>2000V
Operating Temperature Ranges	
MAX4541C_ _	0°C to +70°C
MAX4541E_ _	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation	
8-Lead $\mu$ MAX	330mW
8-Lead NSO	471mW
8-Lead PDIP	727mW
Derate above +70°C	
8-Lead $\mu$ MAX	4.10mW/°C
8-Lead $\mu$ MAX	5.88mW/°C
8-Lead $\mu$ MAX	9.09mW/°C

## II. Manufacturing Information

- A. Description/Function: Low-Voltage, Single-Supply Dual SPST Analog Switch
- B. Process: S3 (SG3) - Standard 3 micron silicon gate CMOS
- C. Number of Device Transistors: 76
- D. Fabrication Location: California or Oregon, USA
- E. Assembly Location: Philippines, Malaysia or Thailand
- F. Date of Initial Production: April, 1997

## III. Packaging Information

A. Package Type:	<b>8 Lead <math>\mu</math>MAX</b>	<b>8 Lead NSO</b>	<b>8 Lead PDIP</b>
B. Lead Frame:	Copper	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate	Solder Plat
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)	Gold (1 mils dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	05-1201-0007	05-1201-0006	05-1201-0005
H. Flammability Rating:	Class UL94-V0	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1		

## IV. Die Information

- A. Dimensions: 57 X 32 mils
- B. Passivation:  $\text{Si}_3\text{N}_4/\text{SiO}_2$  (Silicon nitride/ Silicon dioxide)
- C. Interconnect: Aluminum/Si (Si = 1%)
- D. Backside Metallization: None
- E. Minimum Metal Width: 3 microns (as drawn)
- F. Minimum Metal Spacing: 3 microns (as drawn)
- G. Bondpad Dimensions: 5 mil. Sq.
- H. Isolation Dielectric:  $\text{SiO}_2$
- I. Die Separation Method: Wafer Saw

## V. Quality Assurance Information


- A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)  
Bryan Preeshl (Executive Director of QA)  
Kenneth Huening (Vice President)
- B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.  
0.1% For all Visual Defects.
- C. Observed Outgoing Defect Rate: < 50 ppm
- D. Sampling Plan: Mil-Std-105D

## VI. Reliability Evaluation

### A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate ( $\lambda$ ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4389 \times 240 \times 2} \quad (\text{Chi square value for MTTF upper limit})$$

 Temperature Acceleration factor assuming an activation energy of 0.8eV

$$\lambda = 4.52 \times 10^{-9} \quad \lambda = 4.52 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic 06-5091 shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1L**) located on the Maxim website at <http://www.maxim-ic.com>.

### B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

### C. E.S.D. and Latch-Up Testing

The AH02 die type has been found to have all pins able to withstand a transient pulse of  $\pm 2000\text{V}$ , per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of  $\pm 250\text{mA}$  and/or  $\pm 20\text{V}$ .

**Table 1**  
Reliability Evaluation Test Results

**MAX4541xxA**

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
<b>Static Life Test</b> (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		240	0
<b>Moisture Testing</b> (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	uMax	197	0
			NSO	2340	15
			PDIP	600	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
<b>Mechanical Stress</b> (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters (generic test vehicle)		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.

Note 2: Generic Process/Package Data

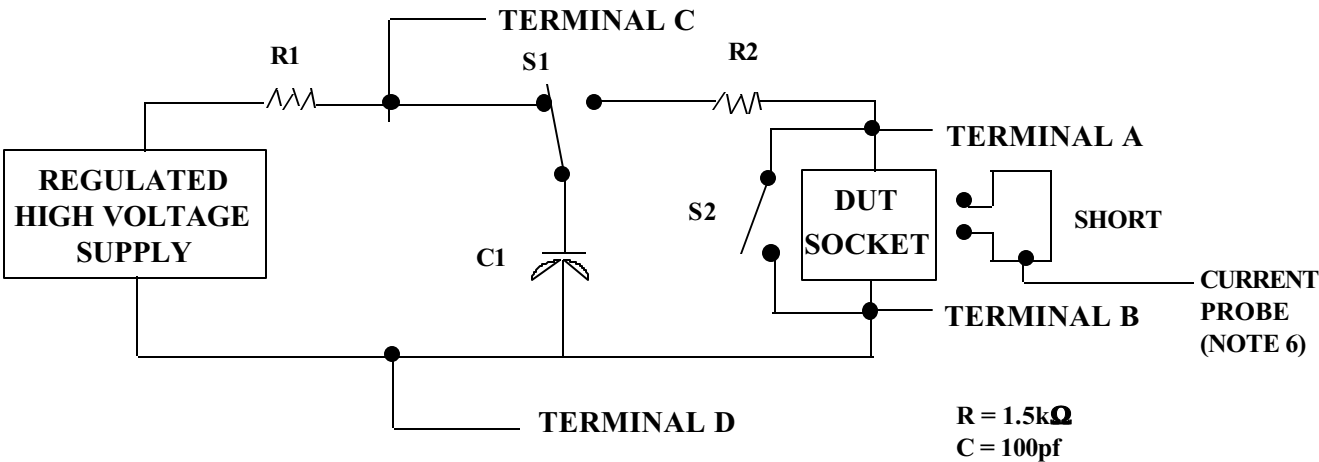
TABLE II. Pin combination to be tested. 1/ 2/

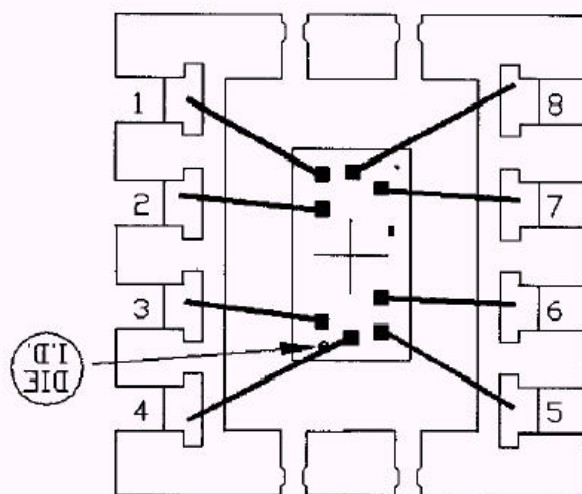
	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except $V_{PS1}$ 3/	All $V_{PS1}$ pins
2.	All input and output pins	All other input-output pins

- 1/ Table II is restated in narrative form in 3.4 below.  
2/ No connects are not to be tested.  
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where  $V_{PS1}$  is  $V_{DD}$ ,  $V_{CC}$ ,  $V_{SS}$ ,  $V_{BB}$ , GND,  $+V_S$ ,  $-V_S$ ,  $V_{REF}$ , etc).

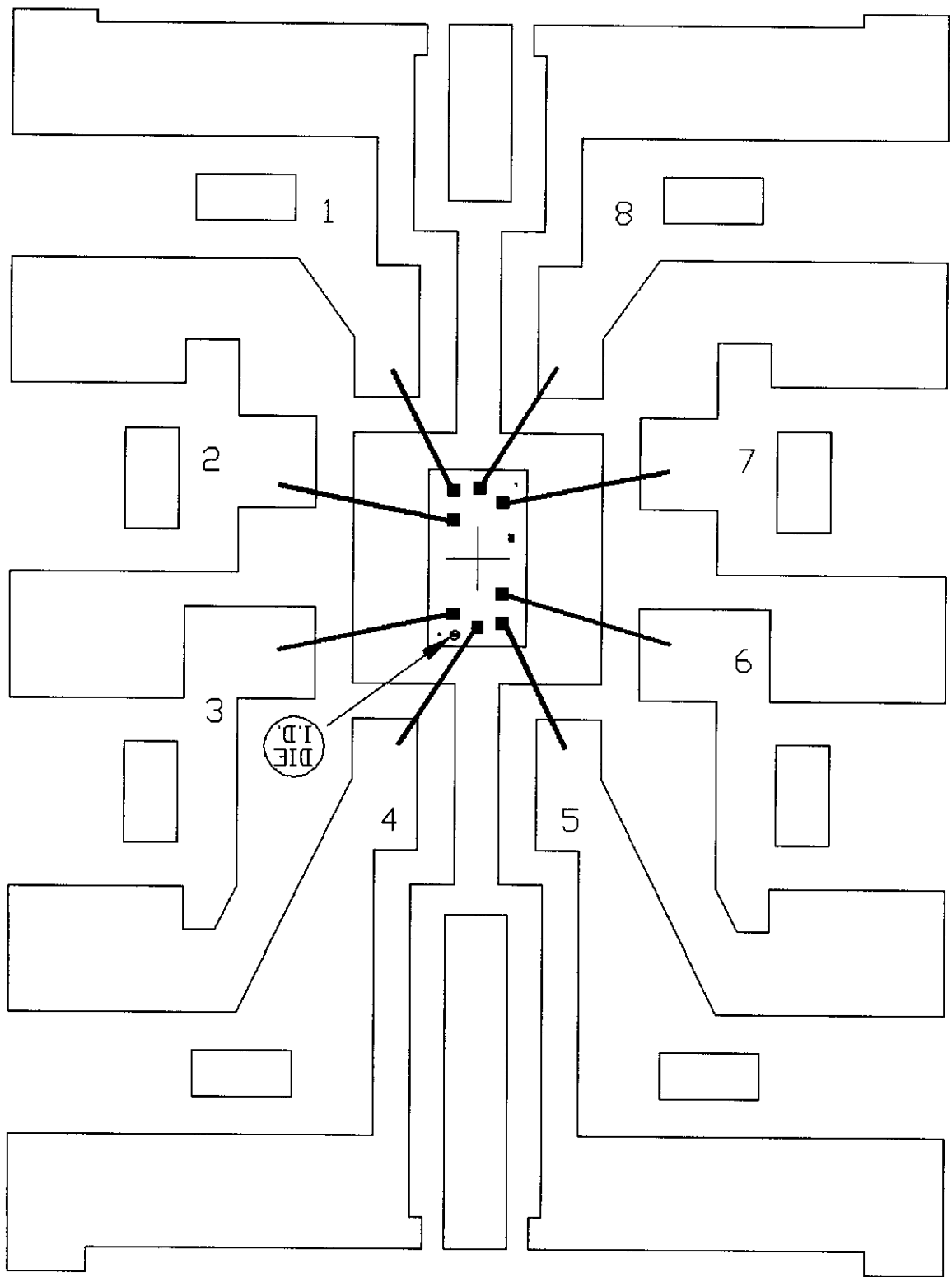
3.4 Pin combinations to be tested.

- Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.
- Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g.,  $V_{SS1}$ , or  $V_{SS2}$  or  $V_{SS3}$  or  $V_{CC1}$ , or  $V_{CC2}$ ) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.
- Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



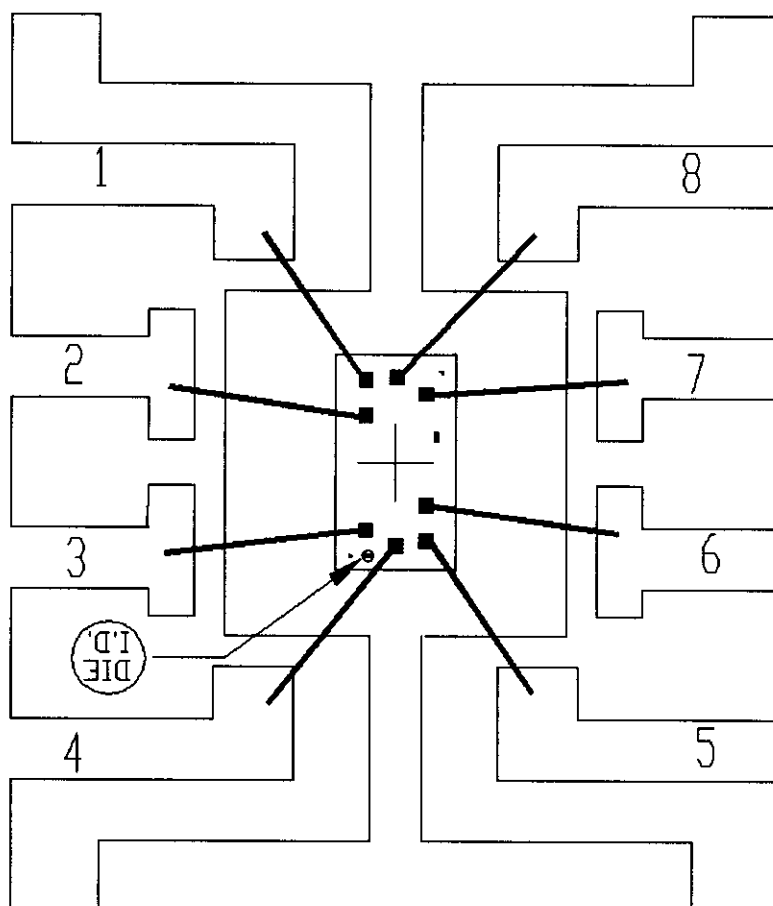


PKG.CODE: U8-1		APPROVALS	DATE	<b>MAXIM</b>	
CAV./PAD SIZE: 68X94	PKG. DESIGN	<i>SVC</i> JAN 06 1997 <i>724</i>	1-797	BUILDSHEET NUMBER: 05-1201-0007	REV: A



PKG.CODE: P8-5		APPROVALS	DATE	<b>MAXIM</b>	
CAV./PAD SIZE: 80X80	PKG. DESIGN	<i>Sve</i> <i>72</i>	JAN 06 1997 1-7-97	BUILDSHEET NUMBER: 05-1201-0005	REV: A

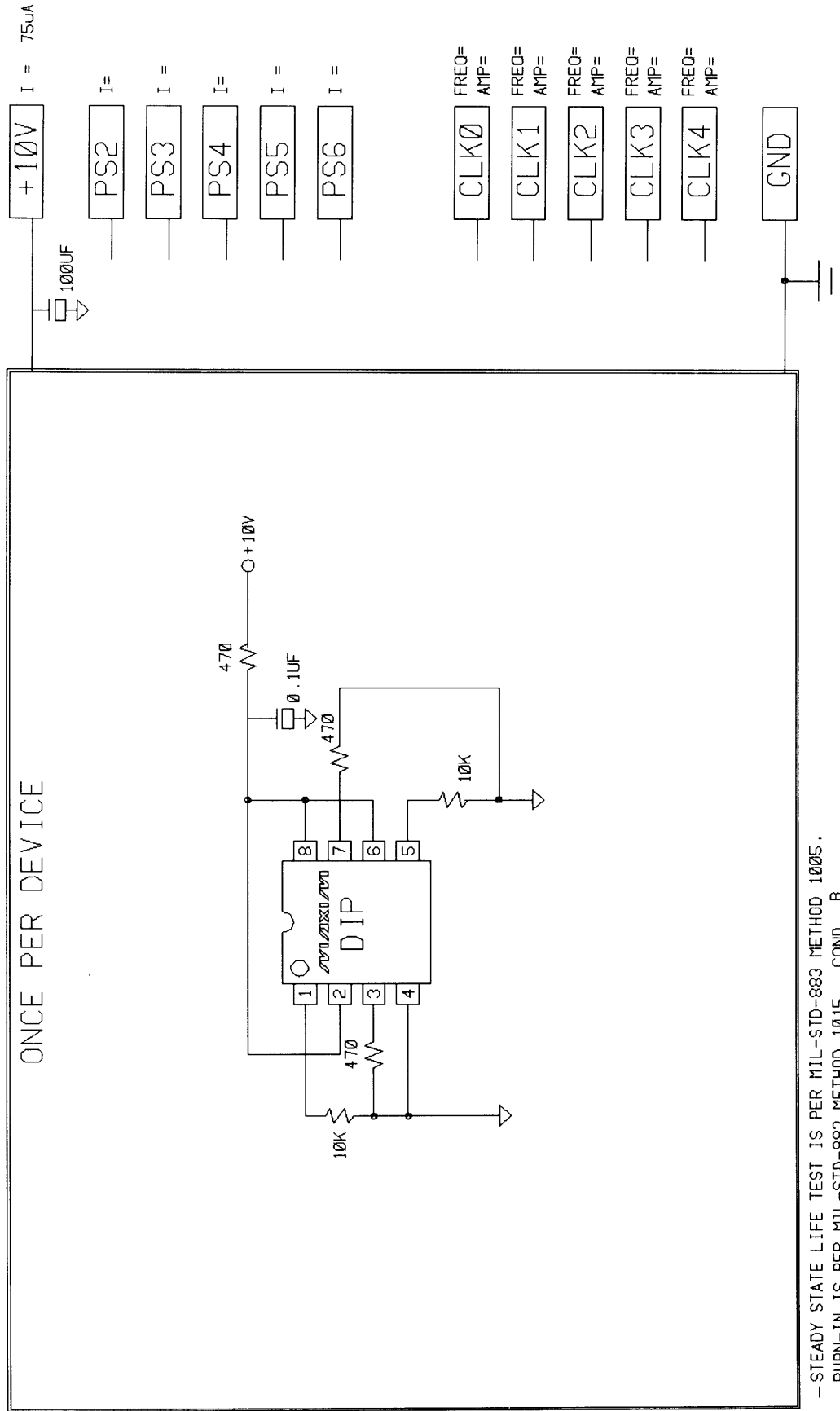




PKG.CODE: S8-2		APPROVALS	DATE	<b>MAXIM</b>	
CAV./PAD SIZE: 90 X 90	PKG. DESIGN	231- Kve	1-7-97 JAN 06 1997	BUILDSHEET NUMBER: 05-1201-0006	REV.: A

ONCE PER BOARD

ONCE PER DEVICE



— STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.  
— BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL [X] HR/883

SPEC. NO. 06-5091 REV: A

DATE: 11/28/94

DRAWN BY: C. JONES

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE(S):

MAX320/323