RELIABILITY REPORT

FOR

MAX4372TExx

PLASTIC ENCAPSULATED DEVICES

December 3, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX4372T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4372T low-cost, precision, high-side current-sense amplifier is available in a tiny, space-saving SOT23-5 package. Offered in three gain versions (T = +20V/V, F = +50V/V, and H = +100V/V), this device operates from a single +2.7V to +28V supply and consumes only 30µA. It features a voltage output that eliminates the need for gain-setting resistors and is ideal for today's notebook computers, cell phones, and other systems where battery/DC current monitoring is critical.

B. Absolute Maximum Ratings

Item	Rating
V_{CC} , RS+, RS- to GND	-0.3V to +30V
OUT to GND	-0.3V to +15V
Differential Input Voltage	-0.3Vto +0.3V
Current into any pin	10mA
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
5-pin SOT	571mW
8-pin SO	471mW
Derates above +70°C	
5-pin SOT	7.1mW/°C
8-pin SO	5.88 mW/°C

II. Manufacturing Information

A. Description/Function: Micropower, High-Side Current Sense Amplifier with Voltage Output

B. Process: S12 – Silicon Gate 1.2 micron CMOS

C. Number of Device Transistors: 225

D. Fabrication Location: Oregon, USA

E. Assembly Location: Malaysia or Thailand

F. Date of Initial Production: June, 1998

III. Packaging Information

A. Package Type:	**5 Lead SOT-23**	**8-Pin SO**
B. Lead Frame:	Alloy 42	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Non-Conductive Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica fill
G. Bonding Diagram	05-3001-0148	05-3001-0147
H. Flammability Rating:	Class UL94-V0	Class UL94-V0

I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112: Level 1

IV. Die Information

A. Dimensions: 57 x 38 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Aluminum

D. Backside Metallization: None

E. Minimum Metal Width: 1.2 microns (as drawn)

F. Minimum Metal Spacing: 1.2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 159 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 6.83 \times 10^{-9}$ $\lambda = 6.83$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic (Spec. # 06-5024) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The OP85Z die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX4372TExx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		159	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	NSO SOT	1480 355	3 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the package.
Note 2: Generic package/process data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

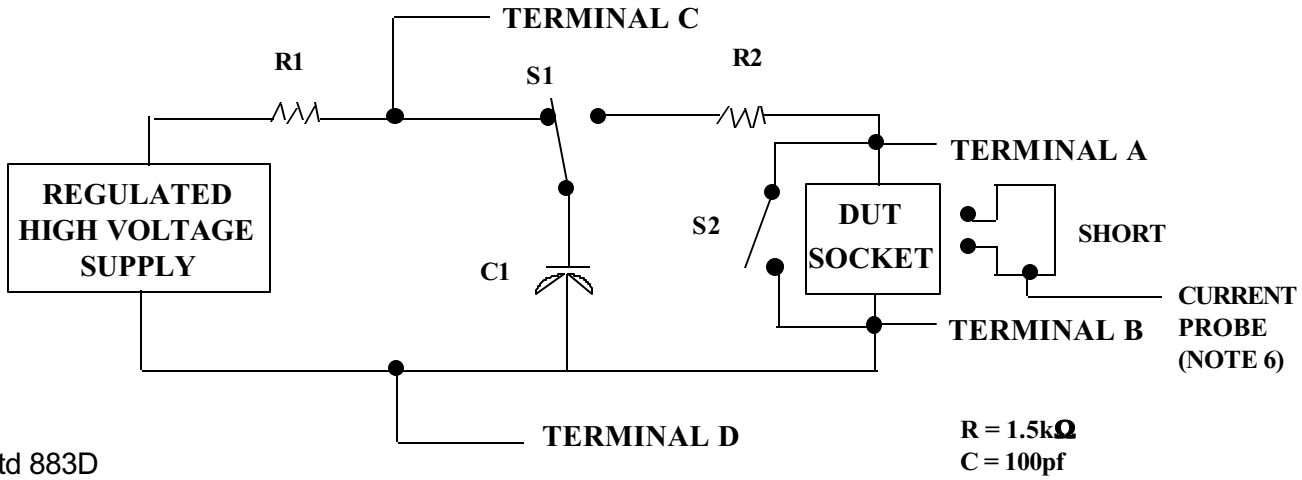
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

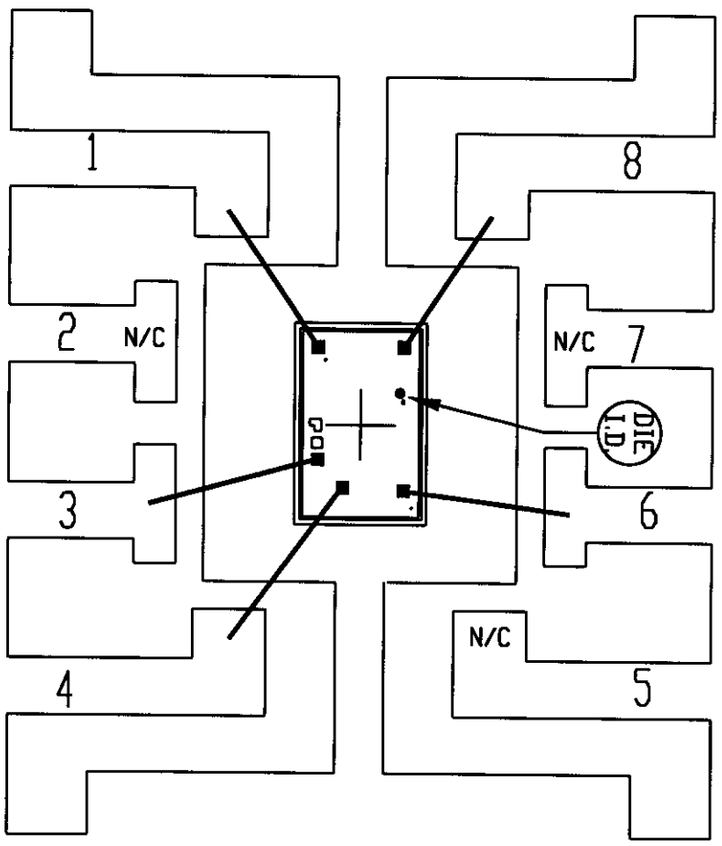
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

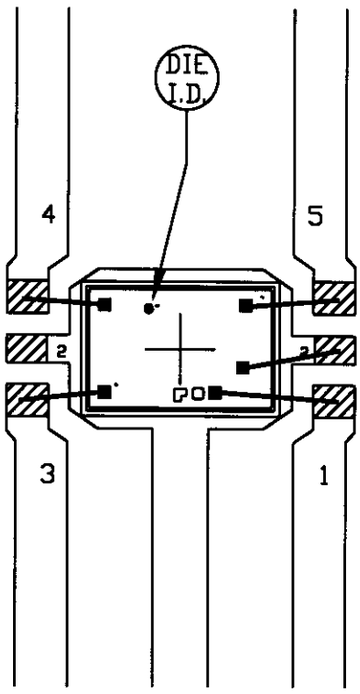
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8



PKG.CODE: S8-2		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 90 X 90	PKG.	RAJ. C	2/5/99	BUILDSHEET NUMBER: 05-3001-0147	REV.: A
	DESIGN	AS PER FAXED COPY	2/8/99		

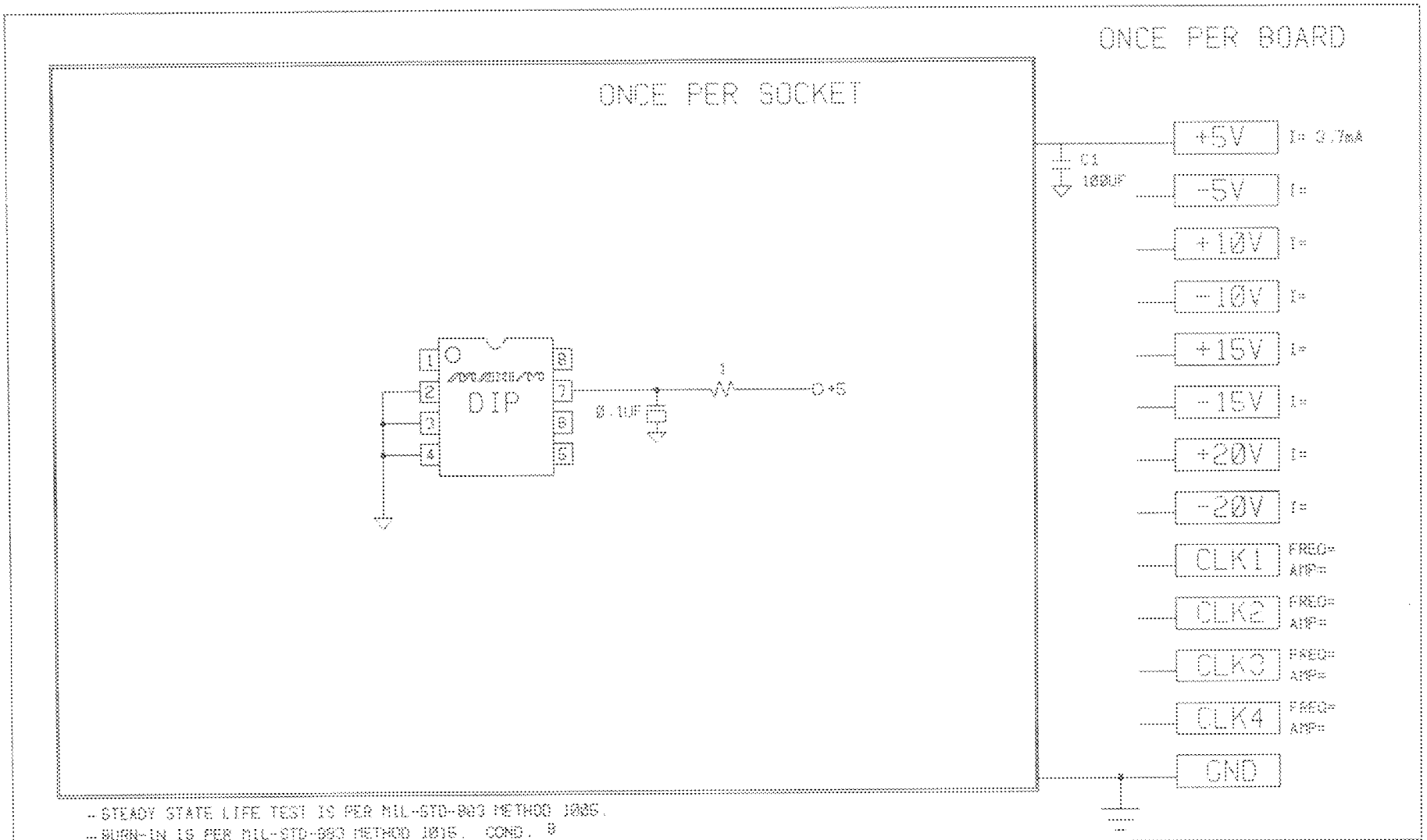


▨ - BONDING AREA

NOTE: MUST USE NON-CONDUCTING EPOXY

NOTE: CAVITY DOWN

PKG.CODE: U5-1		APPROVALS	DATE	MAXIM	
CAV./PAD SIZE: 64X45	PKG.	RAJ.S	2/9/99	BUILDSHEET NUMBER: 05-3001-0148	REV.: A
	DESIGN	P.	2/12/99		



-- STEADY STATE LIFE TEST IS PER MIL-STD-883 METHOD 1005.
-- BURN-IN IS PER MIL-STD-883 METHOD 1015. COND. B

NOTES:

1. TEMPERATURE: 125C OR EQUIVALENT
2. TIME: 160 HOURS MIN. OR EQUIVALENT
3. ALL COMPONENTS AND MATERIAL MUST STAND 150C CONTINUOUS
4. APPROVED FOR [X] COMMERCIAL
   [X] MIL/883

SPEC. NO. 06-5024 REV. B

DATE: 9/05/95

DRAWN BY: R. TARIGA

MAXIM BURN-IN SCHEMATIC

DEVICE TYPE: MAX473/495
MAX4120/4125/41J1