RELIABILITY REPORT

FOR

MAX4242ExA

PLASTIC ENCAPSULATED DEVICES

June 8, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX4242 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4242 micropower op amp operates from a single +1.8V to +5.5V supply or dual ±0.9V to ±2.75V supplies and has Beyond-the-Rails™ input and Rail-to-Rail ® output capabilities. This amplifier provides a 90kHz gain-bandwidth product while using only 10µA of supply current per amplifier.

This amplifier has an input common-mode range that extends 200mV beyond each rail, and its outputs typically swing to within 9mV of the rails with a 100kΩ load. Beyond-the-rails input and rail-to-rail output characteristics allow the full power-supply voltage to be used for signal range. The combination of low input off-set voltage, low input bias current, and high open-loop gain makes it suitable for low-power/low-voltage precision applications. The MAX4242 contains 2 amps.

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage (V_{CC} to V_{EE})	6V
All Other Pins	(V_{CC} + 0.3V) to (V_{EE} - 0.3V)
Output Short-Circuit Duration (to V_{CC} or V_{EE})	Continuous
Junction Temperature	+150°C
Storage Temp.	-65°C to +160°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
8-Lead uMaX	330mW
8-Lead SO	471mW
Derates above +70°C	
8-Lead uMax	4.1mW/°C
8-Lead SO	5.88mW/°C

II. Manufacturing Information

A. Description/Function: Dual, +1.8V/10μA, Beyond-the-Rails Op Amp

B. Process: CB2 (Complementary Bipolar Process)

C. Number of Device Transistors: 466

D. Fabrication Location: Oregon, USA

E. Assembly Location: Philippines, Malaysia, or Thailand

F. Date of Initial Production: March, 1998

III. Packaging Information

A. Package Type:	8-Lead uMax	8-Lead SO
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver Filled Exposy
E. Bondwire:	Gold (1 mil dia.)	Gold (1 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram Buildsheet:	# 05-3001-0098	# 05-3001-0098
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions: 58 x 76 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Gold

D. Backside Metallization: None

E. Minimum Metal Width: 2 microns (as drawn)

F. Minimum Metal Spacing: 2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:

Jim Pedicord	(Reliability Lab Manager)
Bryan Preeshl	(Executive Director of QA)
Kenneth Huening	(Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83 \quad \text{(Chi square value for MTTF upper limit)}}{192 \times 4389 \times 160 \times 2}$$

Thermal acceleration factor assuming a 0.8eV activation energy

$\lambda = 6.79 \times 10^{-9}$ $\lambda = 6.79$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure the reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on lots exceeding this level. The following Burn-In Schematic (Spec. # 06-5216) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The OP64 die type has been found to have all pins able to withstand a transient pulse of ±2000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX4242ExA

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	160	0
Moisture Testing				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality (generic test vehicle)	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality (generic test vehicle)	77	0
Mechanical Stress				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters (generic test vehicle)	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Small Outline package.

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

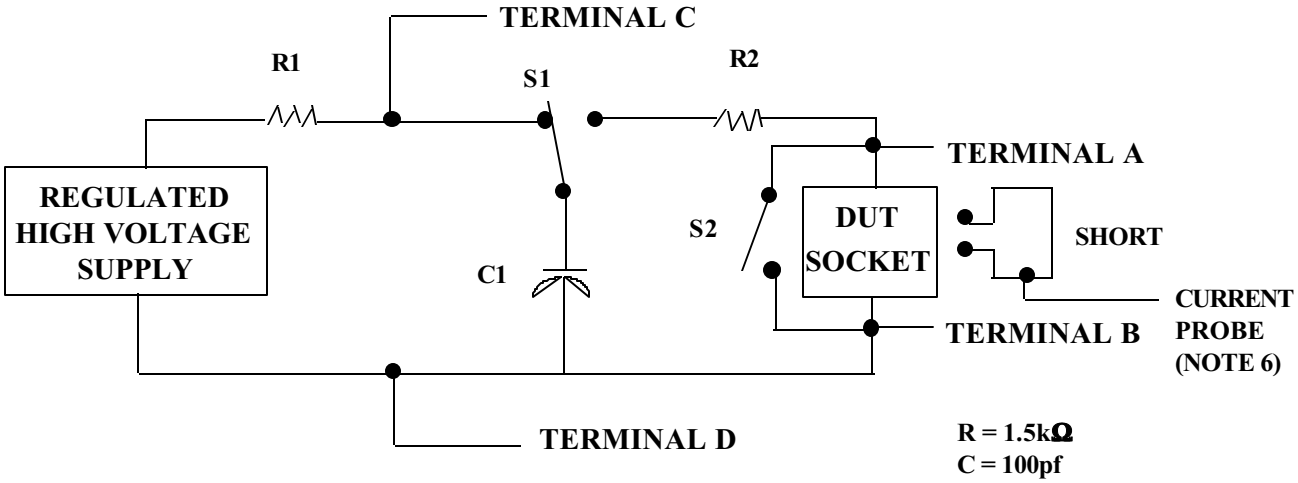
1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

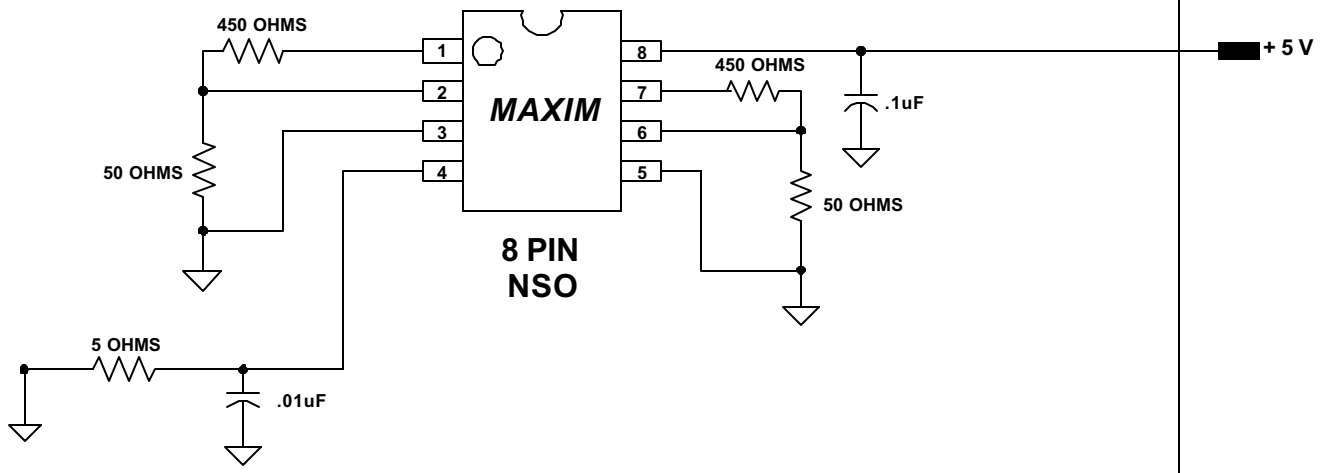
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 4016; MAX 4126 / 4128 / 4133 / 4167;
MAX 4432/4433/4413/4416/4417/4450/4491;
MAX 4353/4453/4436/4437/4092
MAX. EXPECTED CURRENT = 15mA

DRAWN BY: HAK TAN
NOTES: Max current for MAX4092
is .5mA