RELIABILITY REPORT

FOR

MAX4019Exx

PLASTIC ENCAPSULATED DEVICES

August 3, 2001

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

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Conclusion

The MAX4019 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

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I. Device Description

A. General

The MAX4019 is a precision, closed-loop, gain of +2 (or -1) buffer featuring high slew rates, high output current drive, and low differential gain and phase errors. This single-supply device operates from +3.15V to +11V, or from ±1.575V to ±5.5V dual supplies. The input voltage range extends 100mV beyond the negative supply rail and the outputs swing Rail-to-Rail ® .

The MAX4019 requires only 5.5mA of quiescent supply current while achieving a 200MHz -3dB bandwidth and a 600V/µs slew rate. In addition, the MAX4019 has a disable feature that reduces the supply current to 400µA. Input voltage noise for these parts is only 10nV/√Hz and input current noise is only 1.3pA/√Hz. This buffer family is ideal for low-power/low-voltage applications that require wide bandwidth, such as video, communications, and instrumentation systems.

B. Absolute Maximum Ratings

Item	Rating
Supply Voltage (V_{CC} to V_{EE})	12V
IN_-, IN_+, OUT_, EN_	(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Output Short-Circuit Duration to V_{CC} or V_{EE}	Continuous
Storage Temp.	-65°C to +150°C
Lead Temp. (10 sec.)	+300°C
Power Dissipation	
14 Lead SO	667mW
16 Lead QSOP	667mW
Derates above +70°C	
14 Lead SO	8.3mW/°C
16 Lead QSOP	8.3mW/°C

II. Manufacturing Information

A. Description/Function: Low-Cost, High-Speed, Single-Supply, Gain of +2 Buffer with Rail-to-Rail Output

B. Process: CB2 - Complementary Bipolar Process

C. Number of Device Transistors: 299

D. Fabrication Location: Oregon, USA

E. Assembly Location: Philippines, Malaysia, Thailand or Korea

F. Date of Initial Production: October, 1997

III. Packaging Information

A. Package Type:	**14 Lead SO**	**16 Lead QSOP**
B. Lead Frame:	Copper	Copper
C. Lead Finish:	Solder Plate	Solder Plate
D. Die Attach:	Silver-filled Epoxy	Silver-filled Epoxy
E. Bondwire:	Gold (1.3 mil dia.)	Gold (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-3001-0028	Buildsheet # 05-3001-0029
H. Flammability Rating:	Class UL94-V0	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1	Level 1

IV. Die Information

A. Dimensions: 120 x 55 mils

B. Passivation: Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)

C. Interconnect: Gold

D. Backside Metallization: None

E. Minimum Metal Width: 2 microns (as drawn)

F. Minimum Metal Spacing: 2 microns (as drawn)

G. Bondpad Dimensions: 5 mil. Sq.

H. Isolation Dielectric: SiO_2

I. Die Separation Method: Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Reliability Lab Manager)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83 \text{ (Chi square value for MTTF upper limit)}}{192 \times 4389 \times 150 \times 2}$$

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 7.24 \times 10^{-9}$ $\lambda = 7.24$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The attached Burn-In Schematic shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1L**).

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

C. E.S.D. and Latch-Up Testing

The OP08-1 die type has been found to have all pins able to withstand a transient pulse of ±3000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA and/or ±20V.

Table 1
Reliability Evaluation Test Results

MAX4019Exx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		150	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	NSO QSOP	319 77	0 0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		77	0
Mechanical Stress (Note 2)					
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters		77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots for the Small Outline package.
Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground (e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.